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Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Not recommended
for new design

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P-CHANNEL MOS FIELD EFFECT TRANSISTOR FOR SWITCHING

DESCRIPTION

The μ PA1818 is a switching device which can be driven directly by a 2.5 V power source.

This device features a low on-state resistance and excellent switching characteristics, and is suitable for applications such as power management of notebook computers and so on.

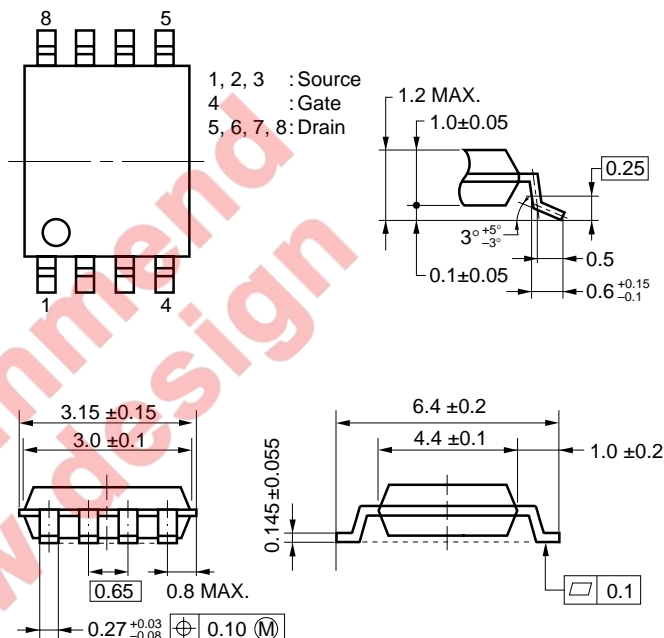
FEATURES

- 2.5 V drive available
- Low on-state resistance
 $R_{DS(on)1} = 15.2 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.5 \text{ V, } I_D = -5.0 \text{ A)}$
 $R_{DS(on)2} = 16 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.0 \text{ V, } I_D = -5.0 \text{ A)}$
 $R_{DS(on)3} = 25 \text{ m}\Omega \text{ MAX. (} V_{GS} = -2.5 \text{ V, } I_D = -5.0 \text{ A)}$
- Built-in G-S protection diode against ESD

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1818GR-9JG	Power TSSOP8

PACKAGE DRAWING (Unit: mm)



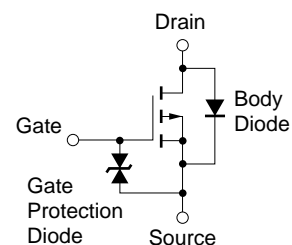
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	-20	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±12	V
Drain Current (DC) (T _A = 25°C)	I _{D(DC)}	±10	A
Drain Current (pulse) ^{Note1}	I _{D(pulse)}	±40	A
Total Power Dissipation ^{Note2}	P _T	2.0	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C

- Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%
 2. Mounted on ceramic substrate of 5000 mm² x 1.1 mm

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

EQUIVALENT CIRCUIT

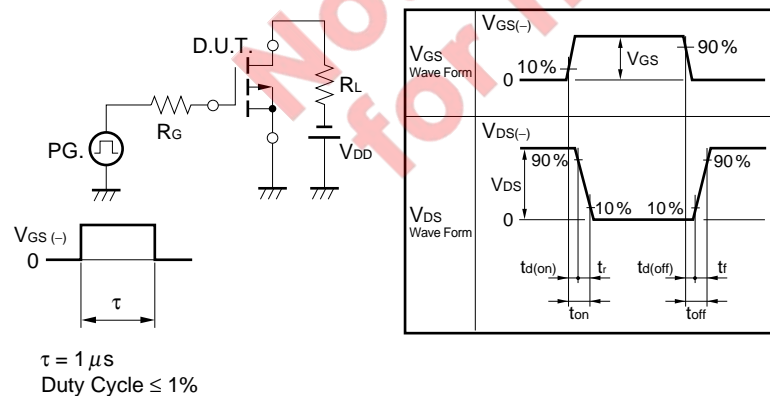


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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

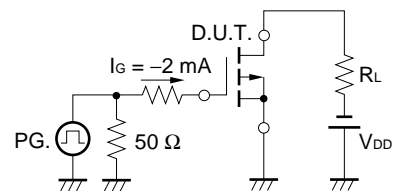
ELECTRICAL CHARACTERISTICS (TA = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$			-1.0	μA
Gate Leakage Current	I_{GSS}	$V_{GS} = \mp 12\text{ V}, V_{DS} = 0\text{ V}$			± 10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	$V_{DS} = -10\text{ V}, I_D = -1.0\text{ mA}$	-0.5	-1.1	-1.5	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS} = -10\text{ V}, I_D = -5.0\text{ A}$	12	24		S
Drain to Source On-state Resistance	$R_{DS(on)1}$	$V_{GS} = -4.5\text{ V}, I_D = -5.0\text{ A}$		12.1	15.2	mΩ
	$R_{DS(on)2}$	$V_{GS} = -4.0\text{ V}, I_D = -5.0\text{ A}$		12.7	16	mΩ
	$R_{DS(on)3}$	$V_{GS} = -2.5\text{ V}, I_D = -5.0\text{ A}$		18.8	25	mΩ
Input Capacitance	C_{iss}	$V_{DS} = -10\text{ V}$		2200		pF
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$		510		pF
Reverse Transfer Capacitance	C_{rss}	$f = 1.0\text{ MHz}$		310		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, I_D = -5.0\text{ A}$		23		ns
Rise Time	t_r	$V_{GS} = -4.0\text{ V}$		207		ns
Turn-off Delay Time	$t_{d(off)}$	$R_G = 10\ \Omega$		139		ns
Fall Time	t_f			193		ns
Total Gate Charge	Q_G	$V_{DD} = -16\text{ V}$		20		nC
Gate to Source Charge	Q_{GS}	$V_{GS} = -4.0\text{ V}$		5.0		nC
Gate to Drain Charge	Q_{GD}	$I_D = -10\text{ A}$		6.0		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	$I_F = 10\text{ A}, V_{GS} = 0\text{ V}$		0.82		V
Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}, V_{GS} = 0\text{ V}$		44		ns
Reverse Recovery Charge	Q_{rr}	$di/dt = 100\text{ A}/\mu\text{ s}$		28		nC

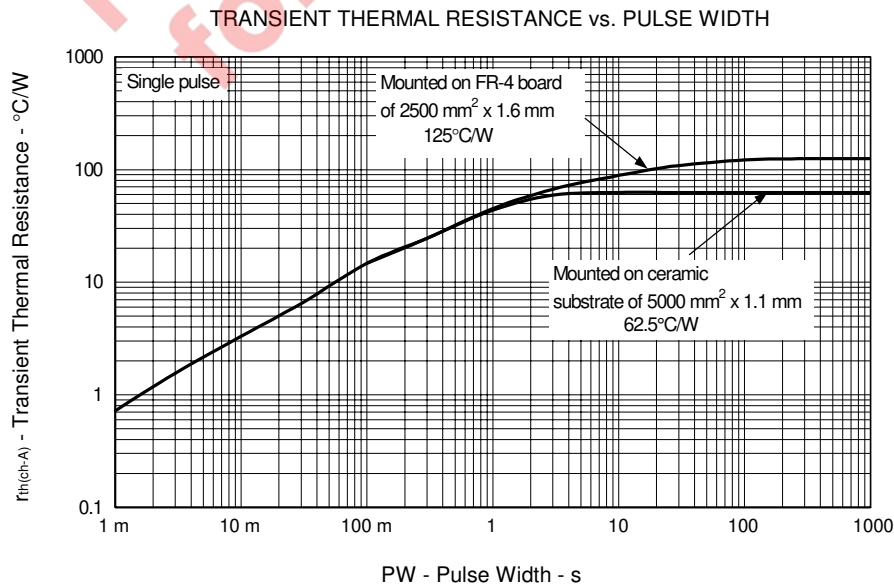
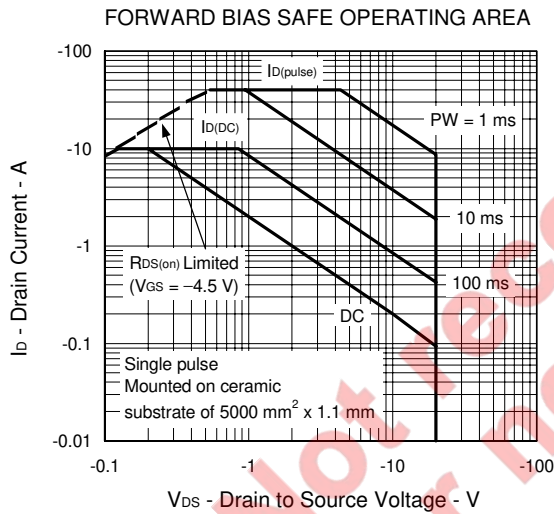
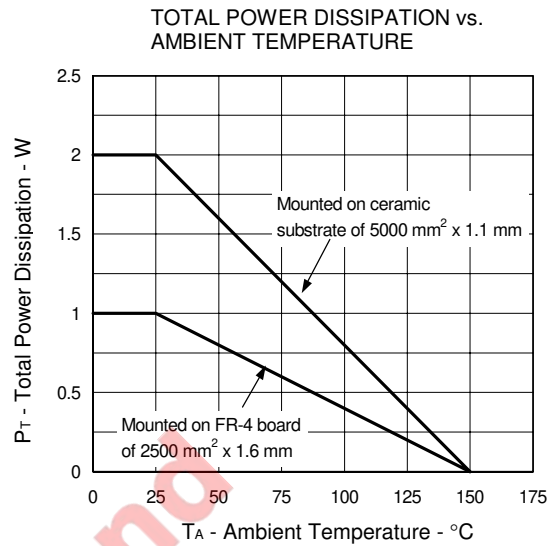
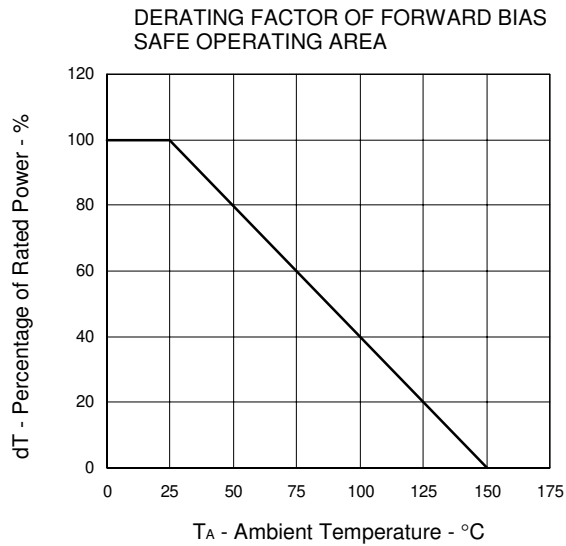
TEST CIRCUIT 1 SWITCHING TIME



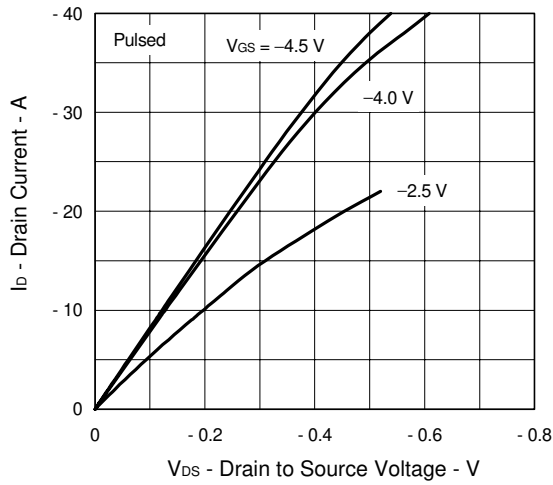
TEST CIRCUIT 2 GATE CHARGE



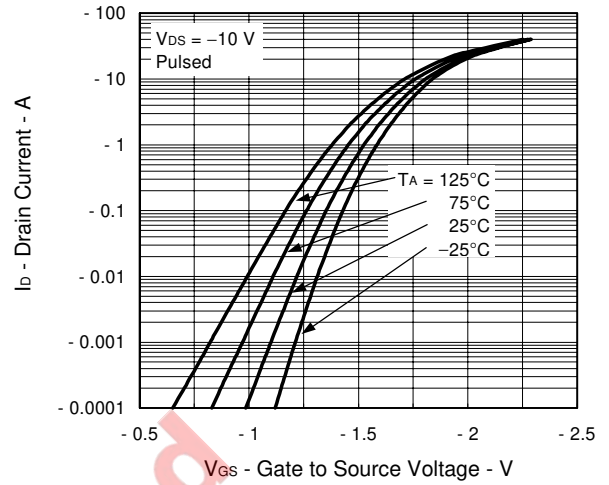
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)



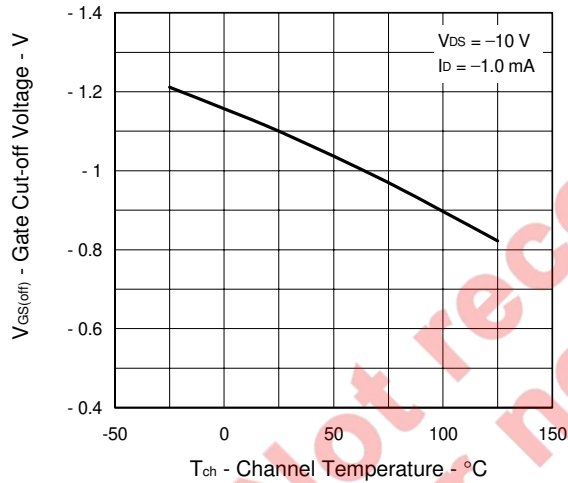
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



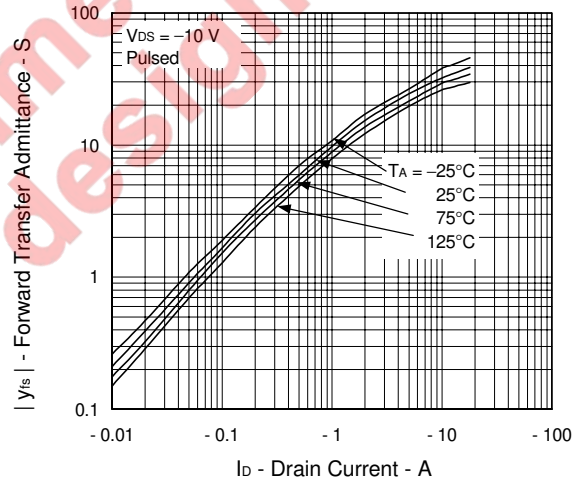
FORWARD TRANSFER CHARACTERISTICS



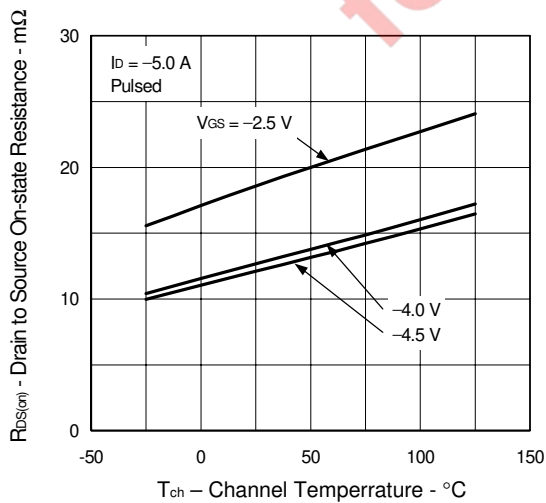
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



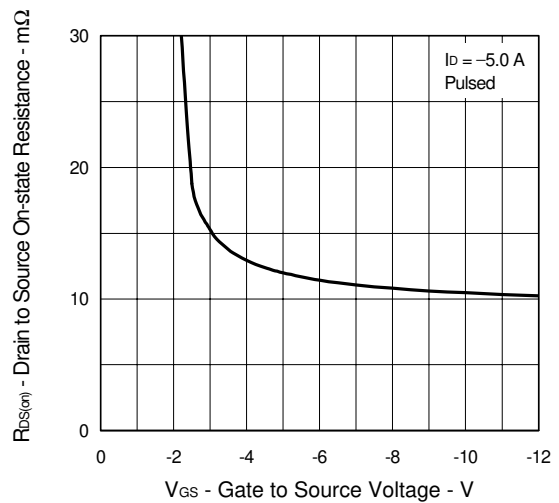
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

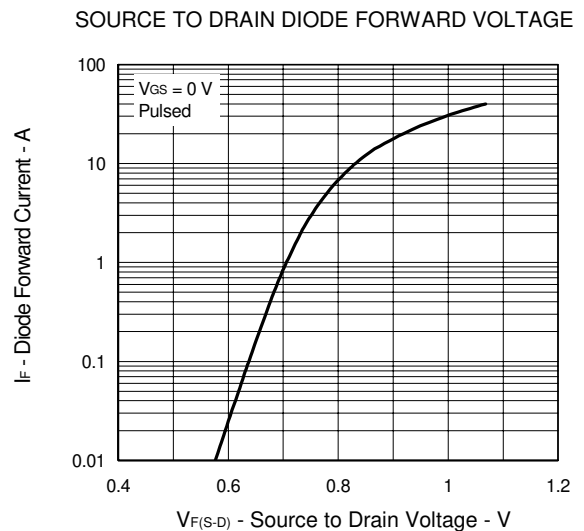
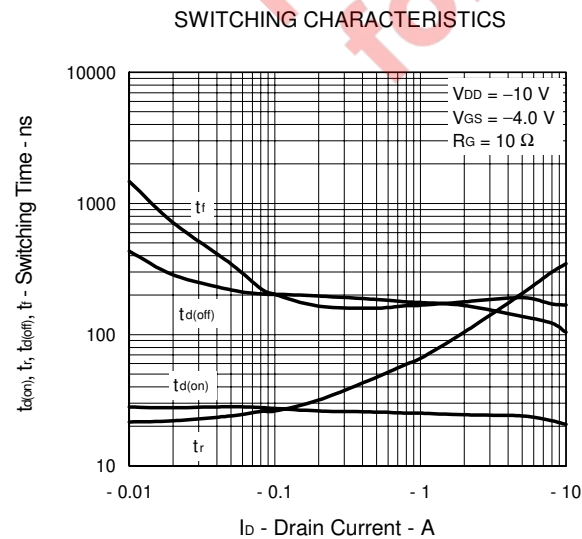
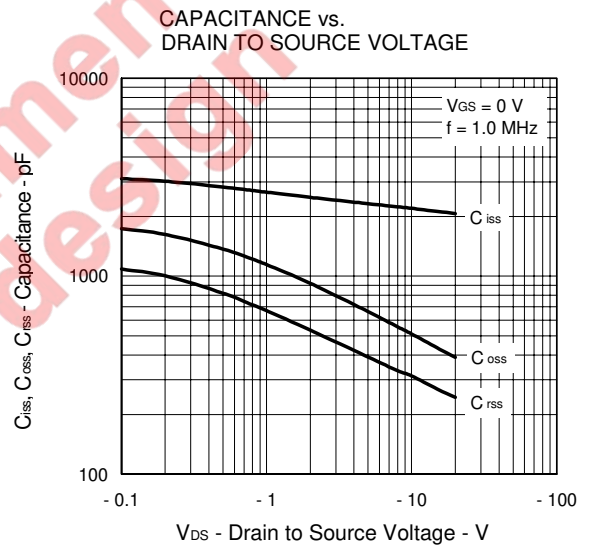
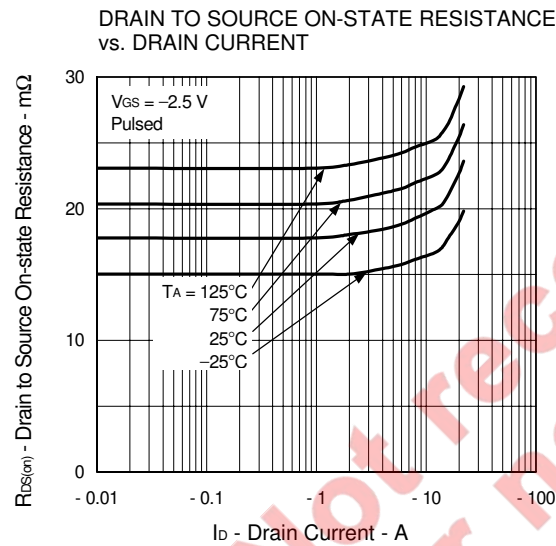
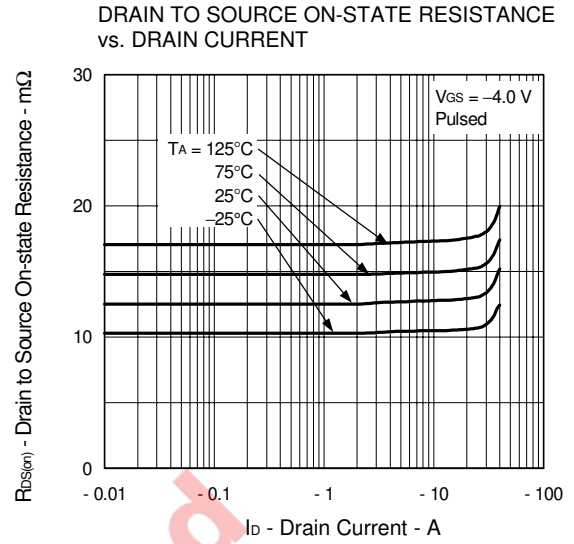
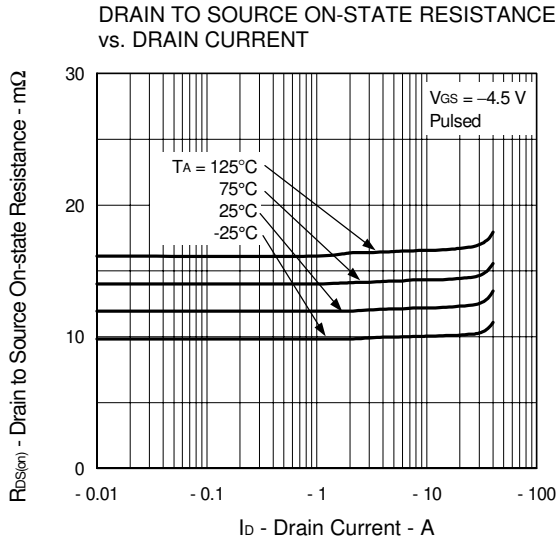


DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

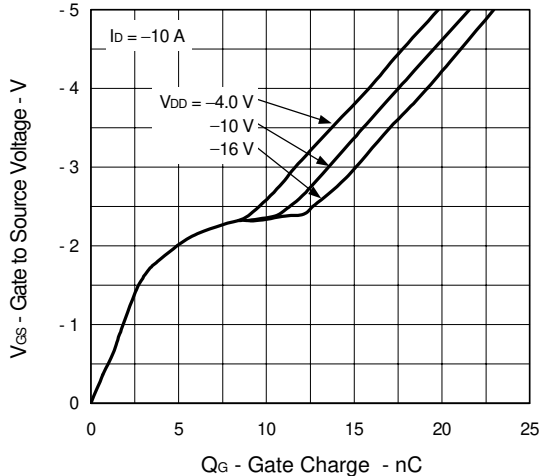


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE





DYNAMIC INPUT/OUTPUT CHARACTERISTICS



Not recommend
for new design

[MEMO]

Not recommend
for new design

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