AOZ32034AQV

Coil Driver for Wireless Charger Transmitter with Slew-Rate Control

General Description

The AOZ32034AQV is an integrated half-bridge solution with intelligent slew-rate control for wireless charger application. The device includes the high-side, low-side N-channel MOSFETs and its driver circuit. Typically, it's dedicated for the design of wireless charger transmitter circuit which is composed of full-bridge topology with resonant tank circuit to get best efficiency of power converter.

The AOZ32034AQV provides adjustable gate drive sink and source current control, by doing this control methodology, it's able to optimize EMI and driver losses to improve overall efficiency performance. Moreover, the features of AOZ32034AQV have multiple protection functions such as V_{CC} UVLO, over temperature protection to make the design more robust.

The AOZ32034AQV is available in a 4mm×4mm QFN-23L package and is rated over a -40°C to +125°C ambient temperature range.

Features

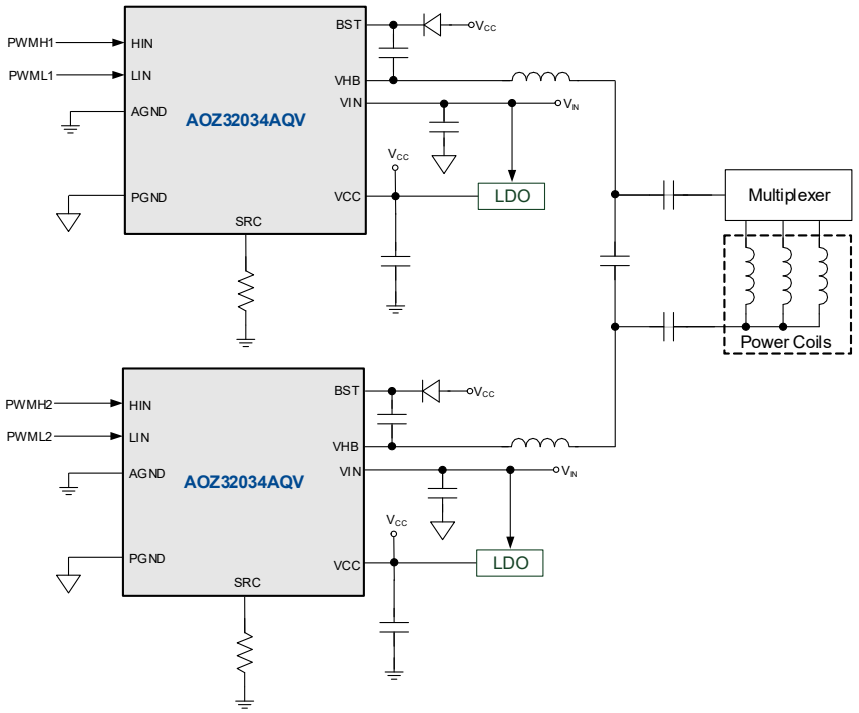
- Maximum input voltage 28V
  - Support 12V & 24V voltage rail system
- 15W~50W Coil Driver
  - For wireless charger transmitter circuit
- Slew-rate control to improve EMI performance
- Low $R_{DS(ON)}$ internal NFETs
  - 7.5mΩ for Both HS/LS
- Integrated Bootstrap Diode
- Support protections
  - OTP, UVLO
- Thermally enhanced 23-pin 4×4 QFN

Applications

- Wireless charger TX

Green Product

Typical Application (Wireless Charger TX)

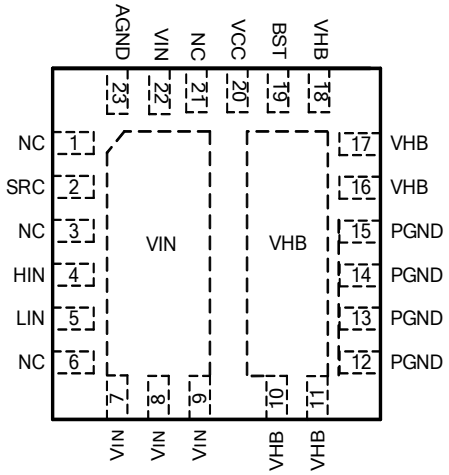


Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ32034AQV	-40°C to +125°C	23-Pin 4x4 QFN	Green

All AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit http://www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



AOZ32034AQV
23-Pin 4mm x 4mm QFN

Pin Description

Pin Number	Pin Name	Pin Function
1	NC(1)	No connect
2	SRC	Slew-Rate Control to Adjust Driver Speed of Internal MOSFET
3	NC	No connect
4	HIN	PWM Input for High-Side MOSFET
5	LIN	PWM Input for Low-Side MOSFET
6	NC	No connect
7, 8, 9, 22	VIN	Supply Input. All IN pins must be connected together
10, 11, 16, 17, 18	VHB	Switching Node for Half-Bridge. All VHB must be connected together
12, 13, 14, 15	PGND	Power Ground
19	BST	Bootstrap Capacitor Connection. Connect an external capacitor between BST and VHB for supplying high-side MOSFET
20	VCC	Supply Input for Analog Functions. Bypass VCC to AGND with a 0.1uF~10uF ceramic capacitor and as close to VCC pin as possible
21	NC	No connect
23	AGND	Analog Ground

Note:
1. NC must be floating.

Absolute Maximum Ratings[1]

Parameter	Rating
VIN to AGND	-0.3V to 30V
VHB to AGND	-0.3V to 30V
BST to AGND	-0.3V to 40V
BST to VHB	-0.3 to 6V
SRC, VCC to AGND	-0.3V to 6V
PGND to AGND	-0.3V to +1V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating	±2kV

Notes:

1. Exceeding the Absolute Maximum ratings may damage the device.
2. The device is not guaranteed to operate beyond the Maximum Operating ratings.

Recommend Operating Ratings[2]

Parameter	Rating
Supply Voltage (V_{IN})	3.8V to 28V
Supply Voltage (V_{CC})	4.75V to 5.5V
Ambient Temperature (T_A)	-40°C to +125°C
Package Thermal Resistance (Θ_{JA}) (Θ_{JC})	 40°C/W 0.6°C/W

Electrical Characteristics

T_A = -40°C to 125°C unless otherwise specified.

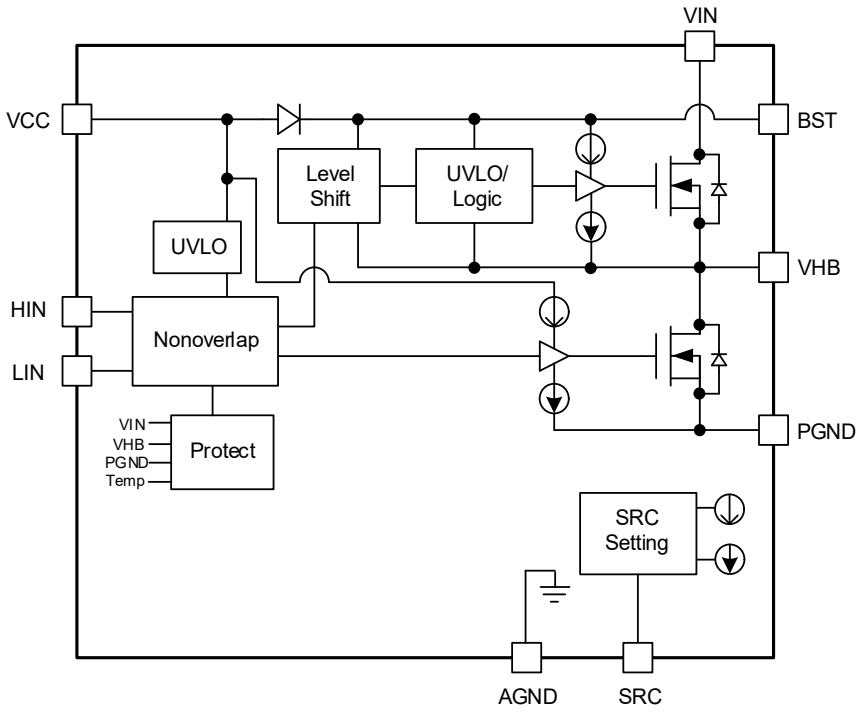
Symbol	Parameter	Conditions	Min	Typ.	Max.	Units
V_{UVLO_R}	Vcc UVLO Rising	V_{IN} =12V, Vcc increase, Monitor SRC from low to high		4.3		V
V_{UVLO_F}	Vcc UVLO Falling	V_{IN} =12V, Vcc decrease, Monitor SRC from high to low		4.2		V
$V_{BST\_UVLO\_R}$	V_{BST}-V_{HB} UVLO Rising	V_{IN} =20V, (V_{BST} -V_{HB}) increase, Monitor V_{HB} from low to high		4.3		V
$V_{BST\_UVLO\_F}$	V_{BST}-V_{HB} UVLO Falling	V_{IN} =20V, (V_{BST} -V_{HB}) decrease, Monitor V_{HB} from high to low		4.2		V
I_{VIN_QC}	I_{VIN} Quiescent Current	V_{IN} =12V, V_{CC}=5V, HIN=LIN=0V, SRC=100kΩ		20		µA
I_{VCC_QC}	I_{VCC} Quiescent Current	V_{IN} =12V, V_{CC}=5V, HIN=LIN=0V, SRC=100kΩ		180		µA
$I_{BST\text{-}VHB\_QC}$	$I_{BST\text{-}VHB}$ Quiescent Current	HIN/LIN=0V, V_{HB}=1V, (V_{BST} -V_{HB})=5V, Monitor (V_{BST} -V_{HB}) Current			40	mA
V_{HLIN_L}	HIN/LIN Logic Low Voltage	V_{IN}=12V	0.7	0.9	1.1	V
V_{HLIN_H}	HIN/LIN Logic High Voltage	V_{IN}=12V	1.2	1.4	1.6	V
R_{HLIN_IN}	HIN/LIN Input Pull Low Impedance			280		kΩ
t_{HIN_RP}	HIN Rising Propagation Delay	V_{IN}=10V, V_{CC}=5V, SRC=20kΩ, VHB to GND=100Ω, HIN=Low to High, Monitor V_{HB} Low to High	62	87	110	ns
t_{HIN_FP}	HIN Falling Propagation Delay	V_{IN}=10V, V_{CC}=5V, SRC=20kΩ, VHB to GND=100Ω, HIN=High to Low, Monitor V_{HB} High to Low	60	86	110	ns
t_{LIN_RP}	LIN Rising Propagation Delay	V_{IN}=10V, V_{CC}=5V, SRC=20kΩ,VHB to GND=100Ω, LIN=Low to High, Monitor V_{HB} High to Low	72	91	105	ns
t_{LIN_FP}	LIN Falling Propagation Delay	V_{IN}=10V, V_{CC}=5V, SRC=20kΩ,VHB to GND=100Ω, LIN=High to Low, Monitor V_{HB} Low to High	50	75	95	ns

Electrical Characteristics

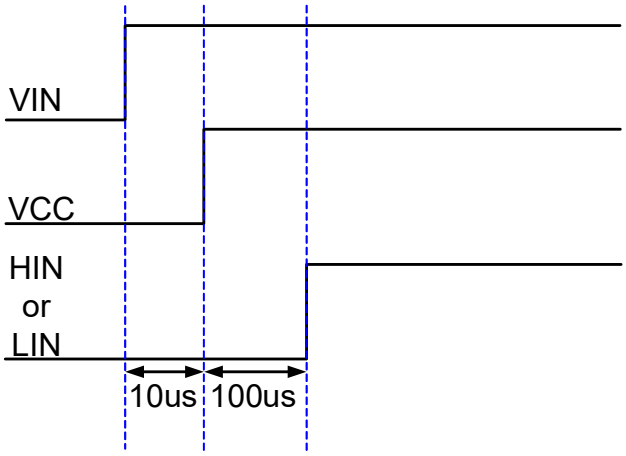
T_A = -40°C to 125°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ.	Max.	Units
T_{DM_R}	Delay Matching Rising	Difference between t_{HIN_RP} and t_{LIN_RP}		4		ns
T_{DM_F}	Delay Matching Falling	Difference between t_{HIN_FP} and t_{LIN_FP}		11		ns
V_{SRC}	SRC	V_{IN}=12V, V_{CC}=5V, SRC=20kΩ	0.97	1	1.03	V
I_{SRC_MIN}	SRC Min. Source Current	V_{IN}=12V, V_{CC}=5V, SRC=4V		0.5		µA
I_{SRC_MAX}	SRC Max. Source Current	V_{IN}=12V, V_{CC}=5V, SRC=0.8V		140		µA
SR_{HIN_R}	HIN Rising Slew Rate (SRC=20kΩ)	VIN=10V, V_{CC}=5V, V_{HB} to GND=100Ω, HIN=Low to High, Monitor V_{HB} Rising Slew Rate		0.4		V/ns
SR_{HIN_F}	HIN Falling Slew Rate (SRC=20kΩ)	VIN=10V, V_{CC}=5V, V_{HB} to GND=100Ω, HIN=High to Low, Monitor V_{HB} Falling Slew Rate		0.5		V/ns
SR_{LIN_R}	LIN Rising Slew Rate (SRC=20kΩ)	VIN=10V, V_{CC}=5V, V_{HB} to VIN=100Ω, LIN=High to Low, Monitor V_{HB} Rising Slew Rate		0.5		V/ns
SR_{LIN_F}	LIN Falling Slew Rate (SRC=20kΩ)	VIN=10V, V_{CC}=5V, V_{HB} to VIN=100Ω, LIN=Low to High Monitor V_{HB} Falling Slew Rate		0.4		V/ns
R_{H_ON}	V_{IN}-V_{HB} RON	V_{IN}=12V, V_{CC}=5V, HIN=5V, (V_{BST} -V_{HB})=5V, I_{VHB}=1A		7.5		mΩ
R_{L_ON}	V_{HB}-PGND RON	V_{IN}=12V, V_{CC}=5V, LIN=5V, PGND=0, I_{VHB}=1A		7.5		mΩ
V_{SD}	Boost Diode Forward Voltage	Forward Current = 2mA		0.42		V
T_{OTP}	OTP	V_{IN}=12V, V_{CC}=5V		150		°C

Functional Block Diagram



Start-up Sequence



Typical Performance Characteristics

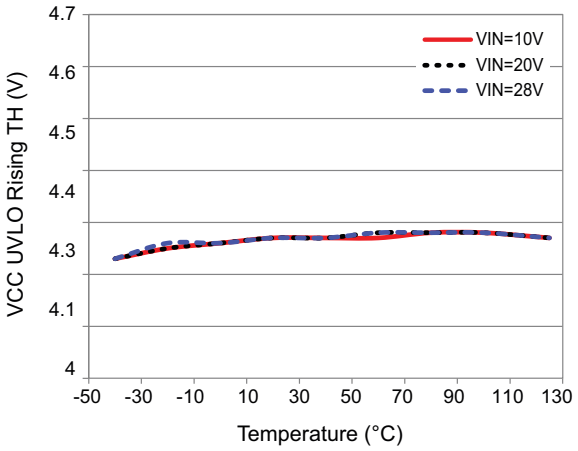


Figure 1. VCC UVLO Rising Threshold

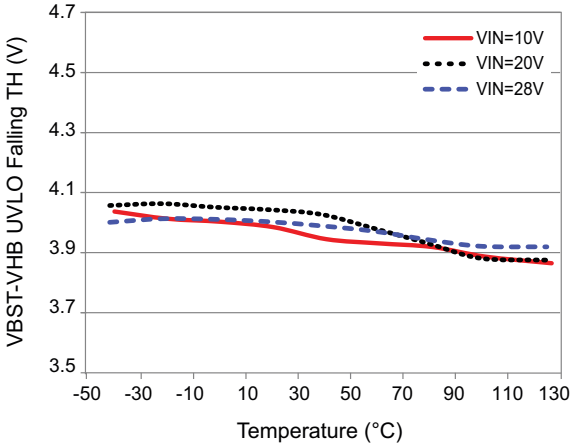


Figure 2. $V_{BST-VHB}$ UVLO Falling Threshold

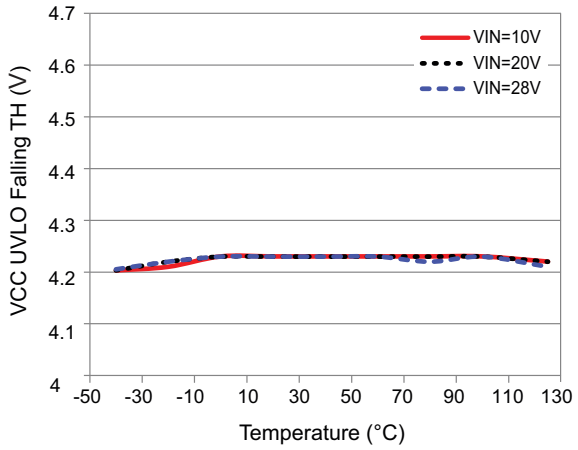


Figure 3. VCC UVLO Falling Threshold

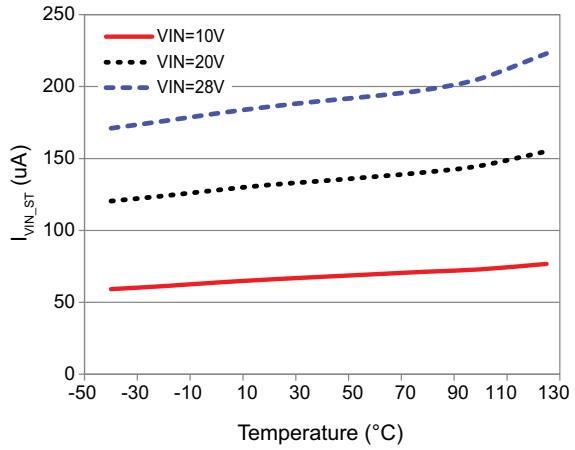


Figure 4. Input Standby Current

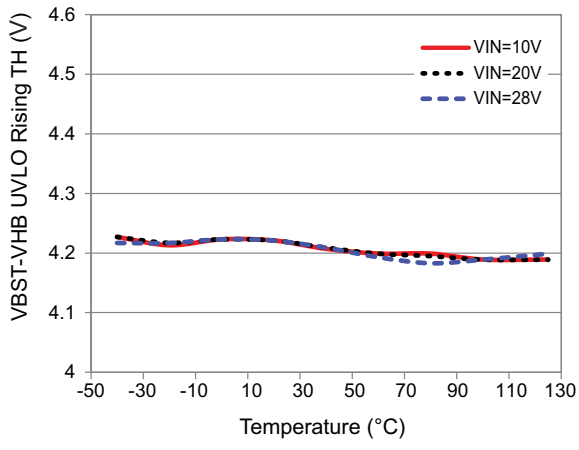


Figure 5. $V_{BST-VHB}$ UVLO Rising Threshold

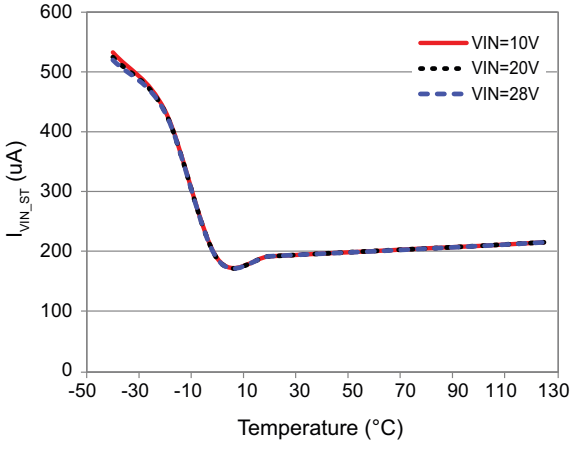


Figure 6. V_{CC} Standby Current

Typical Performance Characteristics *(Continued)*

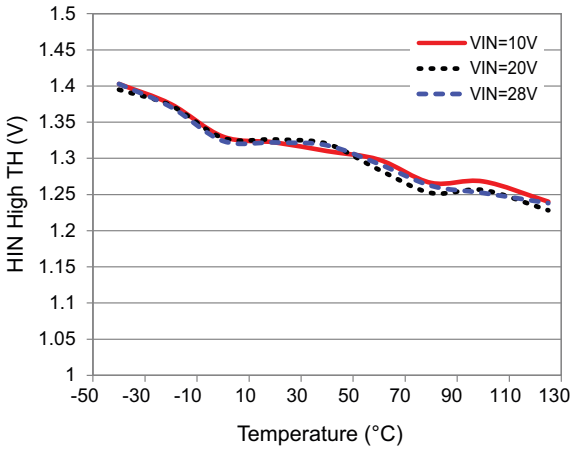


Figure 7. HIN High Threshold

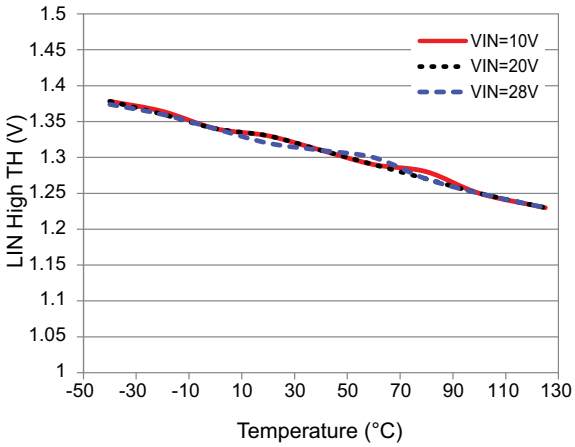


Figure 8. LIN High Threshold

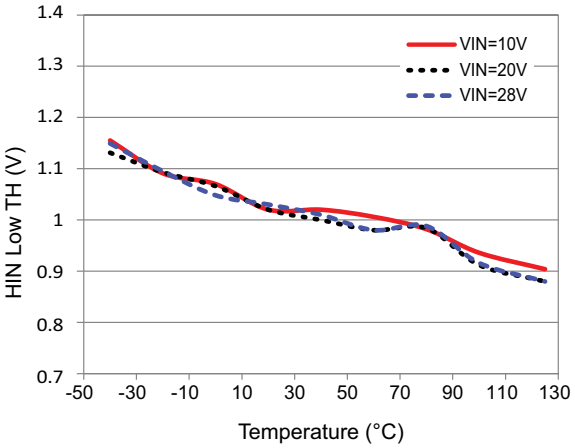


Figure 9. HIN Low Threshold

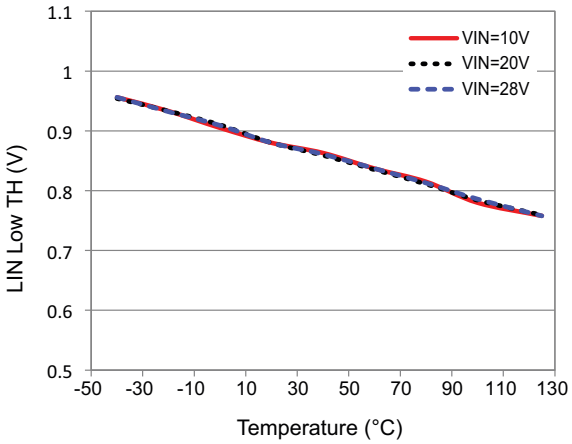


Figure 10. LIN Low Threshold

Detailed Description

The AOZ32034AQV is an integrated half-bridge solution with intelligent slew-rate control for wireless charger application. The device includes the high-side, low-side N-channel MOSFETs and its driver circuit. Typically, it's dedicated for the design of wireless charger transmitter circuit which is composed of full-bridge topology with resonant tank circuit to get best efficiency of power converter.

The AOZ32034AQV provides adjustable gate drive sink and source current control, by doing this control methodology, it's able to optimize EMI and driver losses to improve overall efficiency performance.

In addition, the AOZ32034AQV provides several fault protections, such as UVLO, OTP and non-overlapping mechanism.

The AOZ32034AQV is available in 23-pin 4mm×4mm QFN package.

Non-overlapping

For forbidding shoot-through, HIN or LIN is invalid when HIN or LIN goes high state before other one. For example, low-side gate state keeps low regardless of the state of LIN when HIN is high at first, and vice versa.

Fault Protection

In order to protect power MOSFETs, over temperature protection (OTP) is implemented. AOZ32034AQV will be shutdown when OTP is occurred until VCC is reset. The threshold of OTP is 140°C.

Adjustable Source/Sink Current

It's hard to meet all of EMI specifications in different applications. So, AOZ32034AQV provides external adjustable resistors for tuning gate drive source and sink current.

SRC is used to tune gate drive source and sink current, respectively. A resistor connects between SRC pin and GND to setting gate drive source / sink current by internal current mirror, as illustrated Figure 11. Source and sink current use maximum capability to drive when SRC pin is floating or the voltage on SRC pin is exceed 4V. The suggestion range of R_{SRC} is 10kΩ~100kΩ.

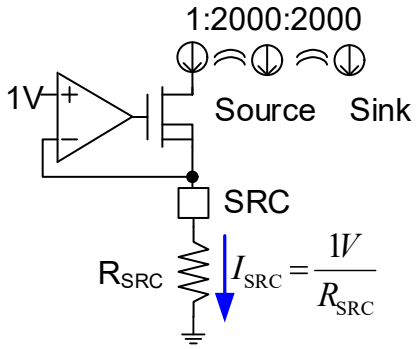


Fig. 11 Source/Sink Current Setting

In addition, source and sink current controls are implemented only during MOSFET Miller effect and VGS >1V, as illustrated Figure 12.

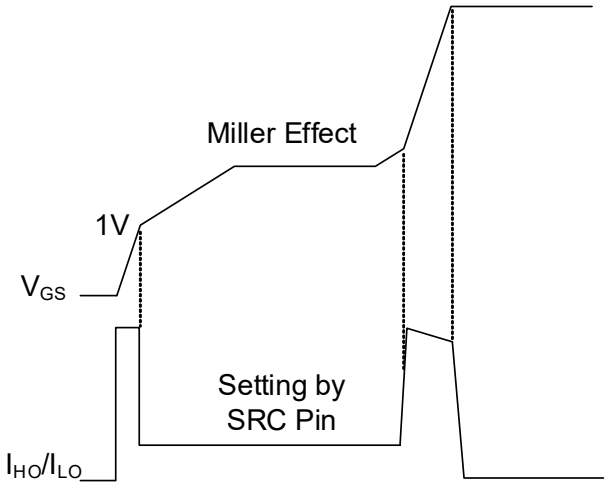


Fig. 12 Source /Sink Current Implement Waveform

Layout Considerations

Several layout tips are listed below for the best electric and thermal performance.

1. The VIN pins and pad are connected to internal high side switch drain. They are also low resistance thermal conduction path. Connected a large copper plane to VIN pins to help thermal dissipation.
2. Input capacitors should be connected to the VIN pins and the PGND pins as close as possible to reduce the switching spikes.
3. The VHB pins and pad are connected to internal low side switch drain. They are low resistance thermal conduction path and most noisy switching node. Connected a large copper plane to VHB pins to help thermal dissipation.
4. Decoupling capacitor C_{VCC} should be connected to VCC and AGND as close as possible.
5. Bootstrap capacitor C_B should be connected to BST and VHB as close as possible.
6. A ground plane is preferred. PGND and AGND must be connected to the ground plane through vias.
7. Keep sensitive signal traces such as feedback trace and digital signals far away from the VHB pins.

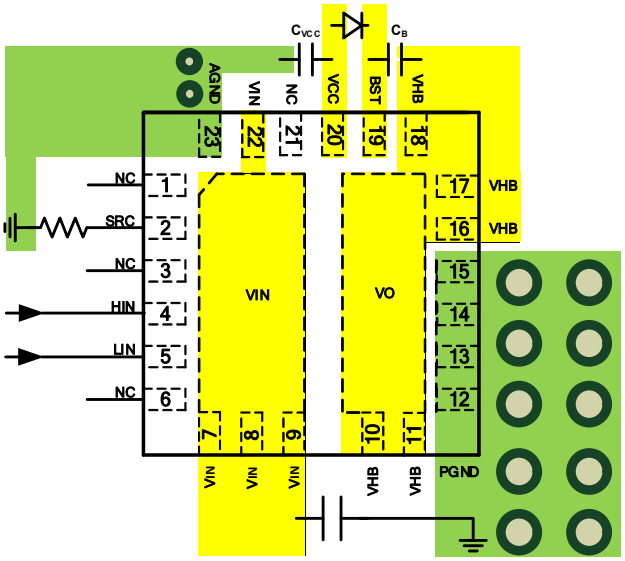
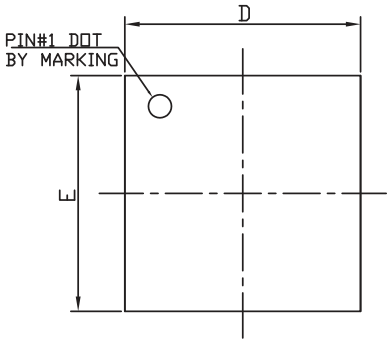
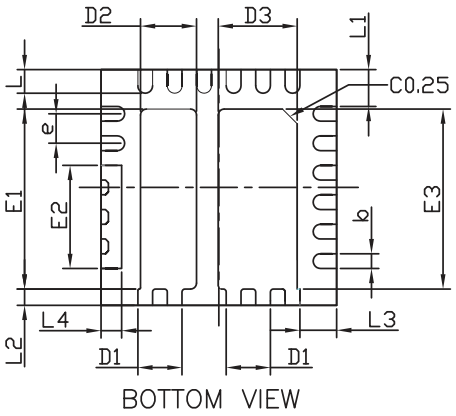


Figure 13. Layout Placement

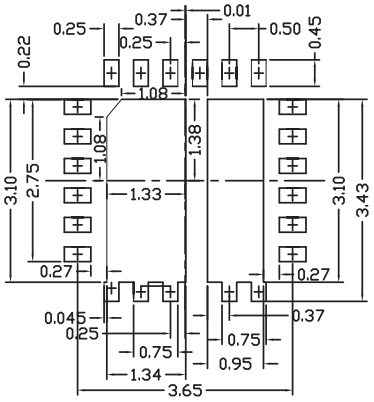
Package Dimensions, QFN4x4-23L



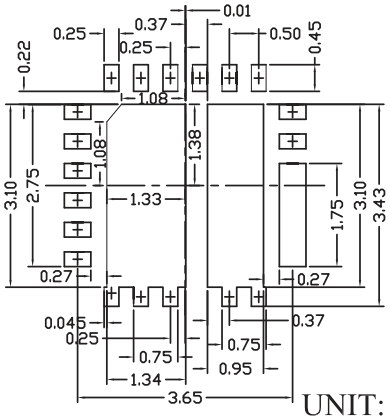


RECOMMENDED LAND PATTERN

Option 1



Option 2



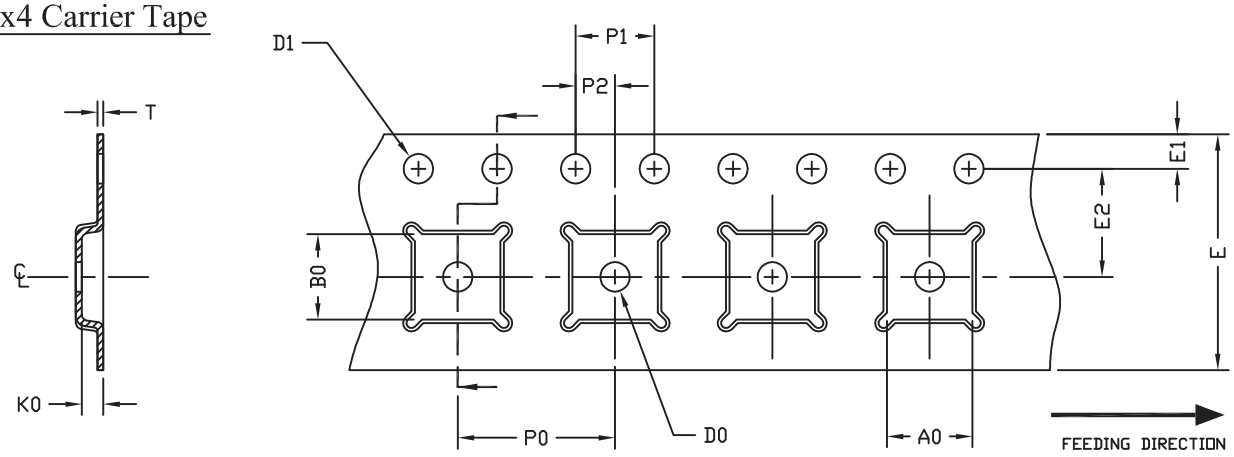
UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	---	0.05	0.000	---	0.002
A2		0.2 REF			0.008 REF	
E	3.90	4.00	4.10	0.153	0.157	0.161
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.65	1.75	1.85	0.065	0.069	0.073
E3	2.95	3.05	3.15	0.116	0.120	0.124
D	3.90	4.00	4.10	0.153	0.157	0.161
D1	0.65	0.75	0.85	0.026	0.030	0.034
D2	0.85	0.95	1.05	0.033	0.037	0.041
D3	1.24	1.34	1.44	0.049	0.053	0.057
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.57	0.62	0.67	0.022	0.024	0.026
L2	0.23	0.28	0.33	0.009	0.011	0.013
L3	0.57	0.62	0.67	0.022	0.024	0.026
L4	0.30	0.35	0.40	0.012	0.014	0.016
b	0.20	0.25	0.30	0.008	0.010	0.012
e		0.50 BSC			0.020 BSC	

NOTE
1. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
2. TOLERANCE :±0.05 UNLESS OTHERWISE SPECIFIED.
3. RADIUS ON ALL CORNER ARE 0.152 MAX., UNLESS OTHERWISE SPECIFIED.
4. PACKAGE WARPAGE: 0.012 MAX.
5. NO ANY PLASTIC FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
6. PAD PLANARITY: ±0.102
7. CRACK BETWEEN PLASTIC BODY AND LEAD IS NOT ALLOWED.

Tape and Reel Dimensions, QFN4x4-23L

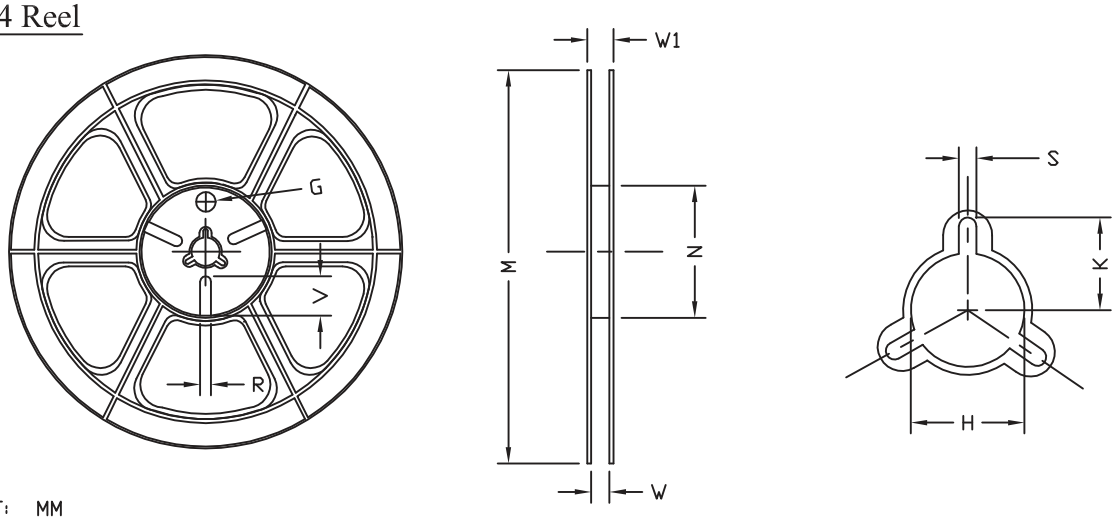
QFN4x4 Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN4x4 (12 mm)	4.35 ±0.10	4.35 ±0.10	1.10 ±0.10	1.50 MIN.	1.50 +0.1 −0.0	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

QFN4x4 Reel



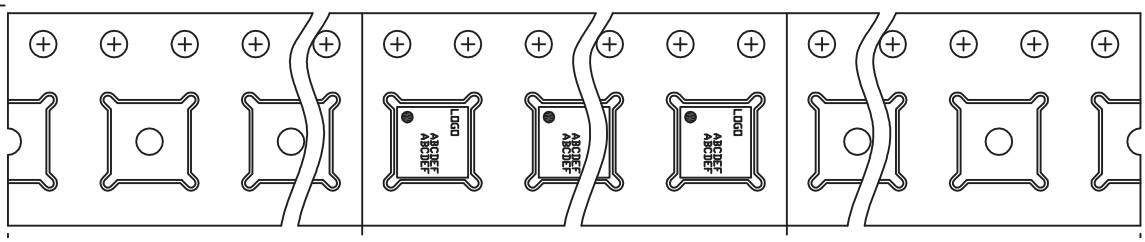
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.0 ±2.0	ø79.0 ±1.0	12.4 +2.0 −0.0	17.0 +2.6 −1.2	ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	---	---	---

QFN4x4 Tape

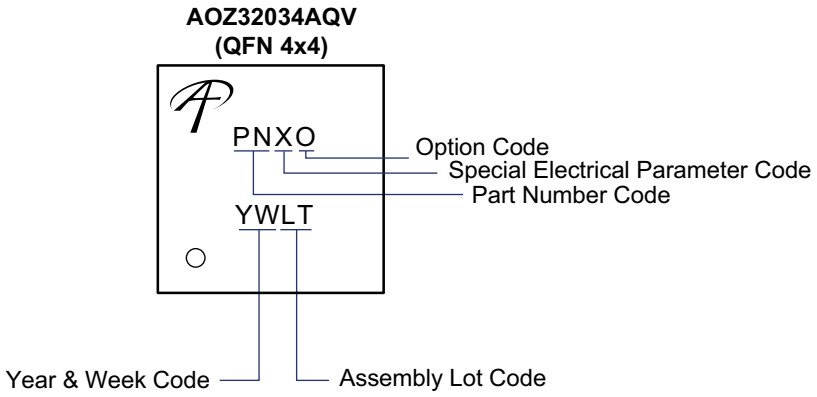
Leader / Trailer & Orientation

Normal



Unit Per Reel:

Part Marking



PART NO.	DESCRIPTION	CODE
AOZ32034AQV	Green Product	DU00

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.