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T-51-19

54/74123

DUAL RETRIGGERABLE RESETTABLE MULTIVIBRATOR

DESCRIPTION — Each half of the '123 features retriggerable capability, complementary dc level triggering and overriding Direct Clear. When a circuit is in the quasi-stable (delay) state, another trigger applied to the inputs (per the Truth Table) will cause the delay period to start again, without disturbing the outputs. By repeating this process, the output pulse period (Q HIGH, \bar{Q} LOW) can be made as long as desired. Alternatively, a delay period can be terminated at any time by a LOW signal on \bar{C}_D , which also inhibits triggering. An internal connection from \bar{C}_D to the input gate makes it possible to trigger the circuit by a positive-going signal on \bar{C}_D , as shown in the Truth Table. For timing capacitor values greater than 1000 pF, the output pulse width is defined as follows.

$$t_w = 0.28 R_x C_x (1.0 + 0.7/R_x)$$

Where t_w is in ns, R_x is in k Ω and C_x is in pF.

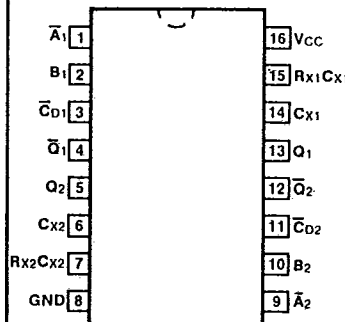
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0 V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = +5.0 V \pm 10\%$, $T_A = -55^\circ C$ to $+125^\circ C$	
Plastic DIP (P)	A	74123PC		9B
Ceramic DIP (D)	A	74123DC	54123DM	6B
Flatpak (F)	A	74123FC	54123FM	4L

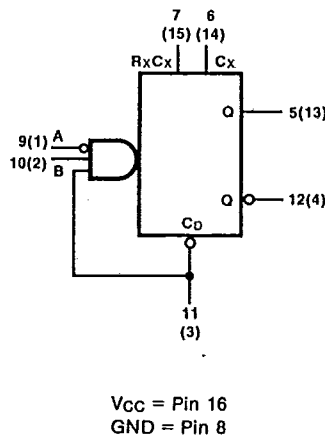
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
\bar{A}_1, \bar{A}_2	Trigger Inputs (Active Falling Edge)	1.0/1.0
B_1, B_2	Trigger Inputs (Active Rising Edge)	1.0/1.0
$\bar{C}_{D1}, \bar{C}_{D2}$	Direct Clear Inputs (Active LOW)	2.0/2.0
Q_1, Q_2	Positive Pulse Output	20/10
\bar{Q}_1, \bar{Q}_2	Negative Pulse Output	20/10

CONNECTION DIAGRAM PINOUT A



LOGIC SYMBOL



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TRIGGERING TRUTH TABLE

INPUTS			RESPONSE
A	B	\bar{C}_D	
X	X	L	No Trigger
\swarrow	L	X	No Trigger
\swarrow	H	H	Trigger
H	\swarrow	X	No Trigger
L	\swarrow	H	Trigger
L	H	\swarrow	Trigger

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

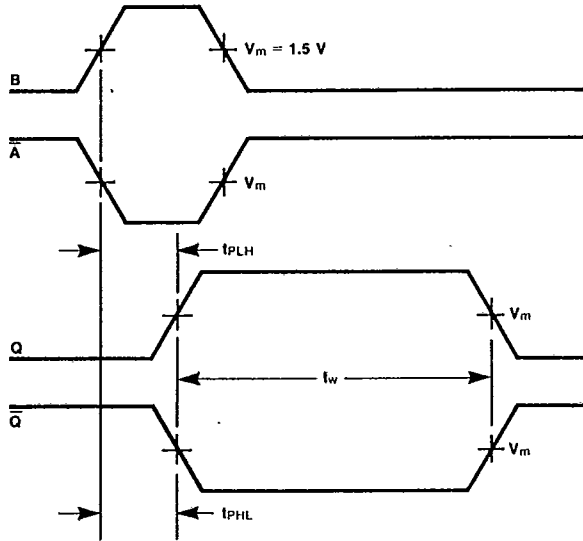
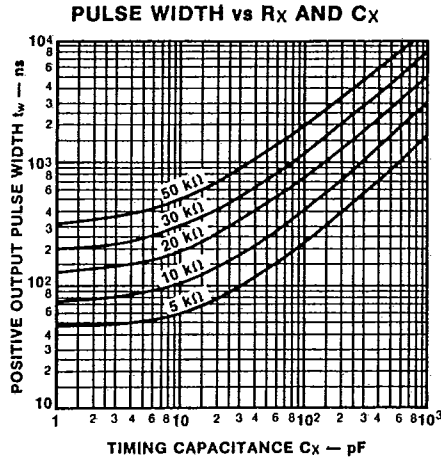


Fig. a.

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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		Min	Max		
I _{OS}	Output Short Circuit Current	-10	-40	mA	V _{CC} = Max
I _{CC}	Power Supply Current		66	mA	V _{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		C _L = 15 pF R _L = 400 Ω			
		Min	Max		
t _{PLH}	Propagation Delay B to Q		28	ns	C _x = 0 pF, R _x = 5 kΩ Fig. 3-1, Fig. a
t _{PLH}	Propagation Delay \bar{A} to Q		33	ns	
t _{PHL}	Propagation Delay B to \bar{Q}		36	ns	
t _{PHL}	Propagation Delay \bar{A} to \bar{Q}		40	ns	
t _{PLH}	Propagation Delay \bar{C}_{Dn} to \bar{Q}		40	ns	C _x = 0 pF, R _x = 5 kΩ Figs. 3-1, 3-10
t _{PHL}	Propagation Delay \bar{C}_{Dn} to Q		27	ns	
t _{w(min)}	Pulse Width with Zero Timing Capacitor		65	ns	C _x = 0 pF, R _x = 5 kΩ Fig. 3-1, Fig. a
t _w	Pulse Width with External Timing Components	2.76	3.37	μs	C _x = 1000 pF, R _x = 10 kΩ Fig. 3-1, Fig. a

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS	
		Min	Max			
t _w	Trigger Pulse Width	40		ns	Over Operating Temperature Range	
R _x	External Timing Resistor	XC	5.0	50		kΩ
		XM	5.0	25		
C _x	External Timing Capacitor	No Restrictions		pF		