NTD70N03R

Power MOSFET

72 A, 25 V, N−Channel DPAK

Features

- Planar HD3e Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low C_{ISS} to Minimize Driver Loss
- Low Gate Charge
- Pb−Free Packages are Available

ON Semiconductor®

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
25 V	5.6 mΩ	72 A

N−Channel

MARKING DIAGRAMS
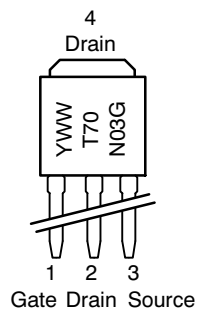
70N03 = Device Code
Y = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MAXIMUM RATINGS (T_J = 25°C Unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	25	V_{dc}
Gate−to−Source Voltage − Continuous	V_{GS}	±20	V_{dc}
Thermal Resistance − Junction−to−Case Total Power Dissipation @ T_C = 25°C Drain Current − Continuous @ T_C = 25°C, Chip − Continuous @ T_C = 25°C, Limited by Package − Continuous @ T_A = 25°C, Limited by Wires − Single Pulse (t_p = 10 μs)	$R_{\theta JC}$ P_D I_D I_D I_D I_{DM}	2.4 62.5 72.0 62.8 32 140	°C/W W A A A A
Thermal Resistance − Junction−to−Ambient (Note1) Total Power Dissipation @ T_A = 25°C Drain Current − Continuous @ T_A = 25°C	$R_{\theta JA}$ P_D I_D	80 1.87 12.0	°C/W W A
Thermal Resistance − Junction−to−Ambient (Note2) Total Power Dissipation @ T_A = 25°C Drain Current − Continuous @ T_A = 25°C	$R_{\theta JA}$ P_D I_D	110 1.36 10.0	°C/W W A
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 175	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 30 V_{dc}, V_{GS} = 10 V_{dc}, I_L = 12 A_{pk}, L = 1 mH, R_G = 25 Ω)	E_{AS}	71.7	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 s	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
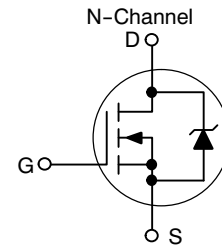1. When surface mounted to an FR4 board using 0.5 sq. in. pad size.
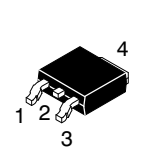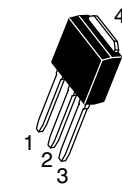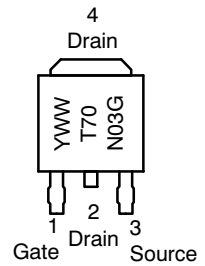2. When surface mounted to an FR4 board using minimum recommended pad size.

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Breakdown Voltage (Note 3) (V_{GS} = 0 V_{dc}, I_D = 250 μA_{dc}) Temperature Coefficient (Positive)	$V_{(br)DSS}$	25 –	28 20.5	– –	V_{dc} mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 20 V_{dc}, V_{GS} = 0 V_{dc}) (V_{DS} = 20 V_{dc}, V_{GS} = 0 V_{dc}, T_J = 150°C)	I_{DSS}	 – –	 – –	 1.5 10	μA_{dc}
Gate–Body Leakage Current (V_{GS} = ±20 V_{dc}, V_{DS} = 0 V_{dc})	I_{GSS}	–	–	±100	nA_{dc}
ON CHARACTERISTICS (Note 3)					
Gate Threshold Voltage (Note 3) (V_{DS} = V_{GS}, I_D = 250 μA_{dc}) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	1.0 –	1.5 4.0	2.0 –	V_{dc} mV/°C
Static Drain–to–Source On–Resistance (Note 3) (V_{GS} = 4.5 V_{dc}, I_D = 20 A_{dc}) (V_{GS} = 10 V_{dc}, I_D = 20 A_{dc})	$R_{DS(on)}$	 – –	 8.1 5.6	 13 8.0	$m\Omega$
Forward Transconductance (Note 3) (V_{DS} = 10 V_{dc}, I_D = 15 A_{dc})	g_{FS}	–	27	–	Mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	C_{ISS}	–	1333	–	pF
Output Capacitance	C_{OSS}	–	600	–	
Transfer Capacitance	C_{RSS}	–	218	–	
SWITCHING CHARACTERISTICS (Note 4)					
Turn–On Delay Time	$t_{d(on)}$	–	6.9	–	ns
Rise Time	t_r	–	1.3	–	
Turn–Off Delay Time	$t_{d(off)}$	–	18.4	–	
Fall Time	t_f	–	5.5	–	
Gate Charge	Q_T	–	13.2	–	nC
	Q_{GS}	–	3.3	–	
	Q_{DS}	–	6.5	–	
SOURCE–DRAIN DIODE CHARACTERISTICS					
Forward On–Voltage (I_S = 20 A_{dc}, V_{GS} = 0 V_{dc}) (Note 3) (I_S = 20 A_{dc}, V_{GS} = 0 V_{dc}, T_J = 125°C)	V_{SD}	 – –	 0.86 0.73	 1.2 –	V_{dc}
Reverse Recovery Time	t_{rr}	–	27.9	–	ns
	t_a	–	14.8	–	
	t_b	–	13.1	–	
Reverse Recovery Stored Charge	Q_{RR}	–	19	–	nC

The dynamic characteristics are measured at (V_{DS} = 20 V_{dc}, V_{GS} = 0 V, f = 1 MHz).

The switching characteristics turn-on/off times are measured at (V_{GS} = 10 V_{dc}, V_{DD} = 10 V_{dc}, I_D = 36 A_{dc}, R_G = 3 Ω).

The gate charge is measured at (V_{GS} = 5 V_{dc}, I_D = 36 A_{dc}, V_{DS} = 10 V_{dc}) (Note 3).

The reverse recovery is measured at (I_S = 36 A_{dc}, V_{GS} = 0 V_{dc}, dI_S/dt = 100 A/μs) (Note 3).

3. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.
4. Switching characteristics are independent of operating junction temperatures.

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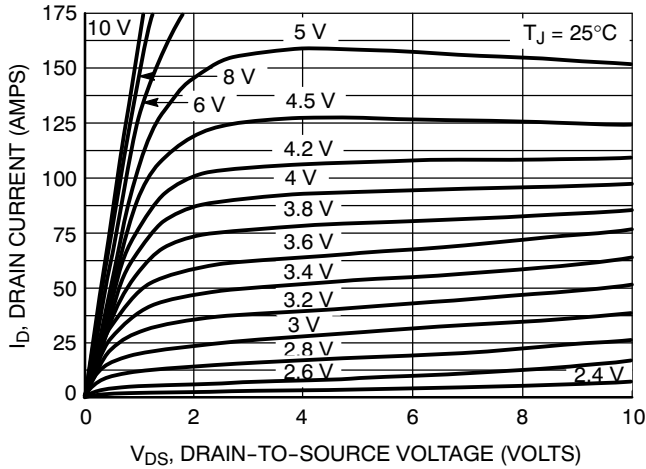## TYPICAL PERFORMANCE CURVES (T$_J$ = 25°C unless otherwise noted)

Figure 1. On–Region Characteristics

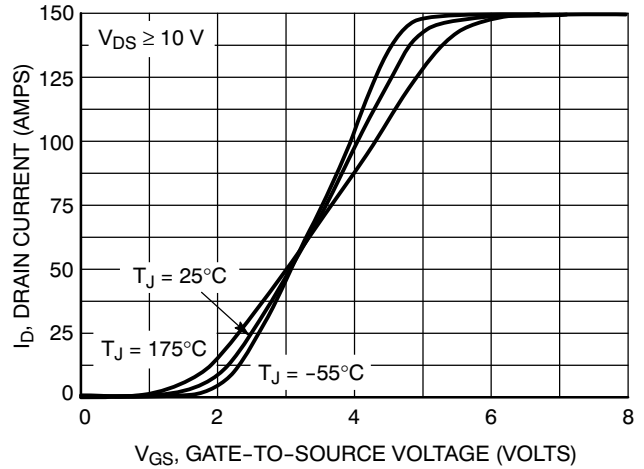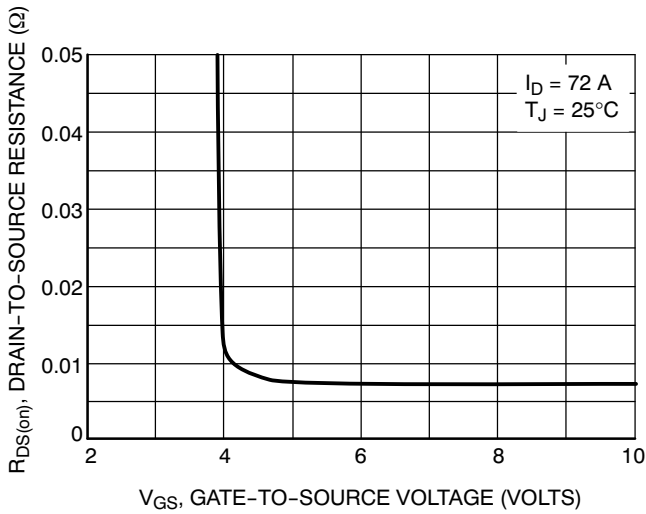**Figure 2. Transfer Characteristics**

Figure 3. On–Resistance versus Gate–to–Source Voltage
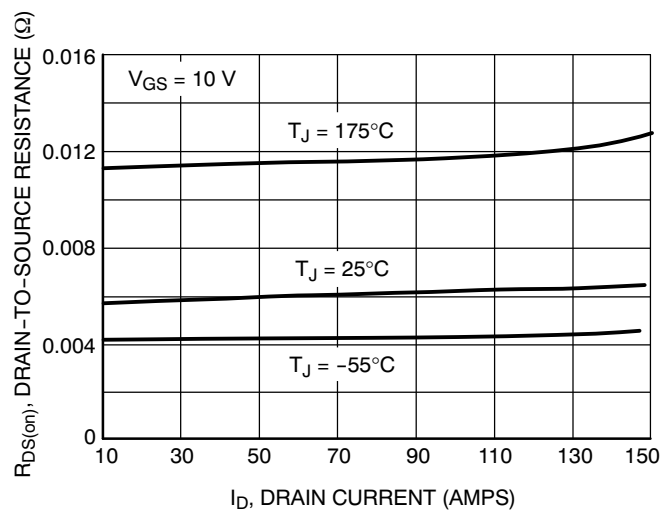
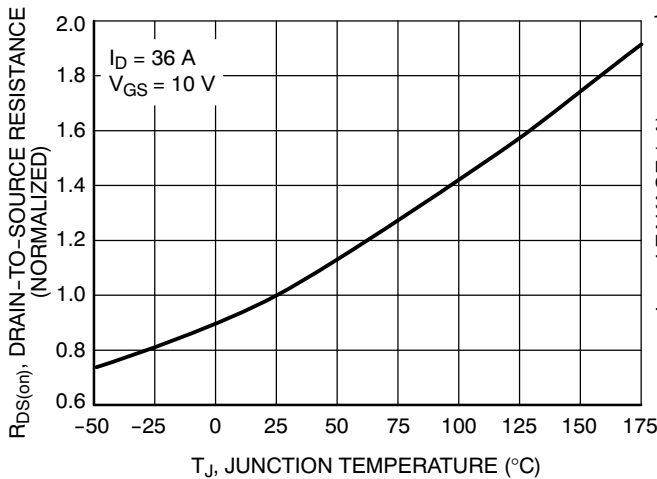**Figure 4. On–Resistance versus Drain Current and Gate Voltage**
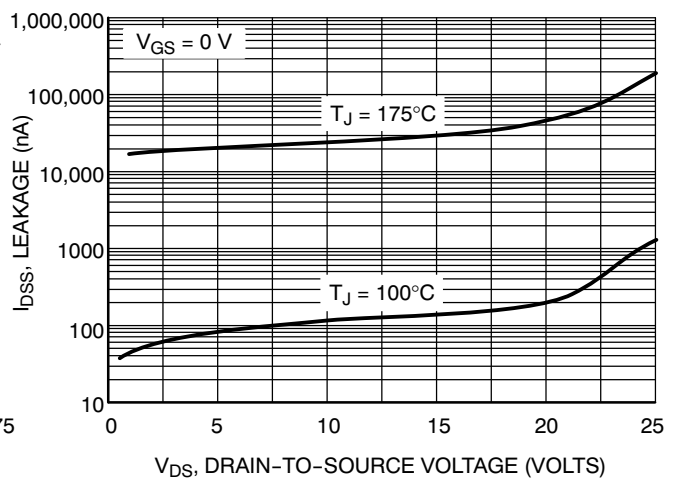
Figure 5. On–Resistance Variation with Temperature

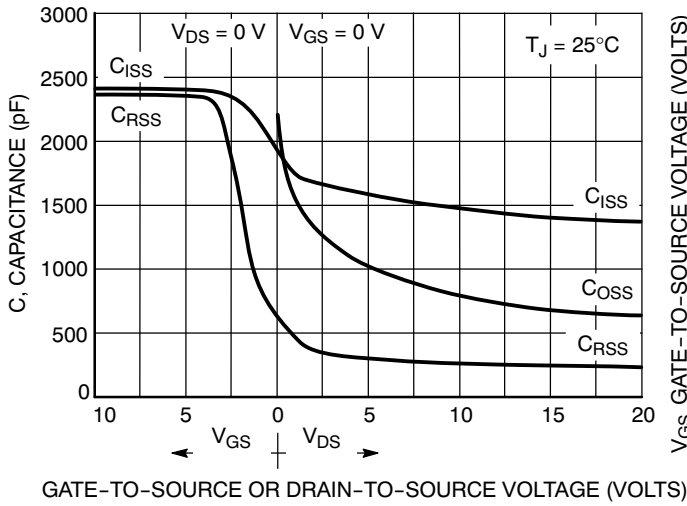**Figure 6. Drain–to–Source Leakage Current versus Voltage**
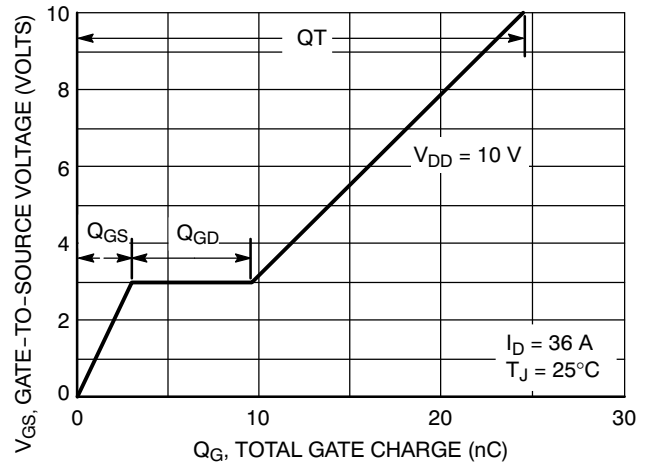
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Figure 7. Capacitance Variation

Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge
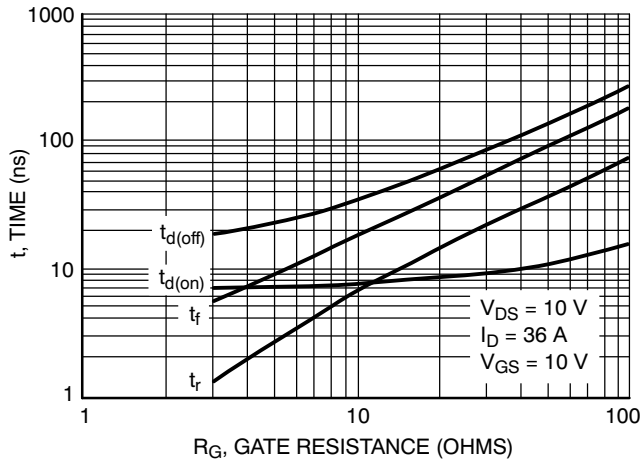
Figure 9. Resistive Switching Time Variation versus Gate Resistance
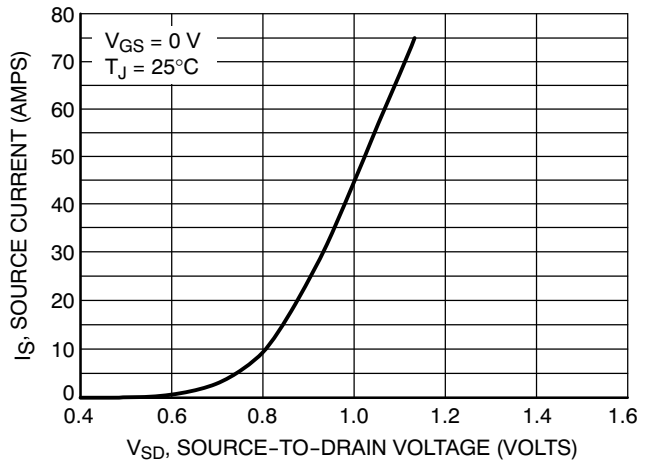
Figure 10. Diode Forward Voltage versus Current
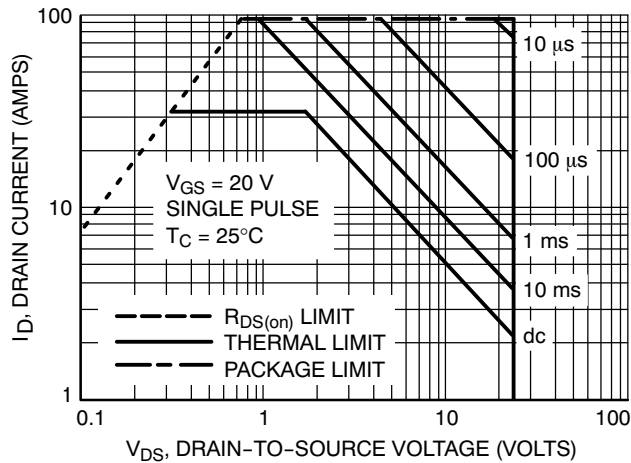
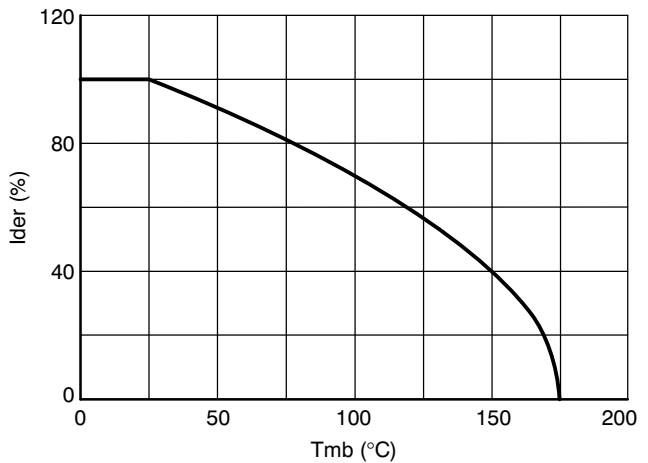Figure 11. Maximum Rated Forward Biased Safe Operating Area

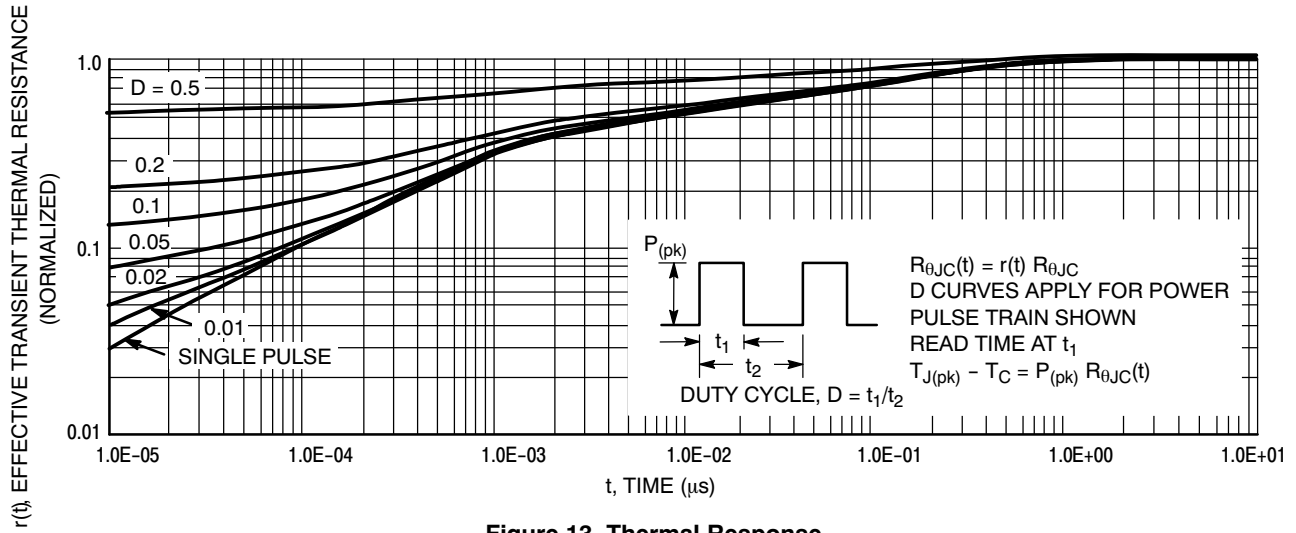Figure 12. Normalized Continuous Drain Current as a function of Mounting Base Temperature

r(t), EFFECTIVE TRANSIENT THERMAL RESISTANCE (NORMALIZED)

D = 0.5
0.2
0.1
0.05
0.02
0.01
SINGLE PULSE

$P_{(pk)}$

t_1
t_2

DUTY CYCLE, $D = t_1/t_2$

$R_{\theta JC}(t) = r(t)\ R_{\theta JC}$
D CURVES APPLY FOR POWER
PULSE TRAIN SHOWN
READ TIME AT t_1
$T_{J(pk)} - T_C = P_{(pk)}\ R_{\theta JC}(t)$

t, TIME (μs)

Figure 13. Thermal Response

ORDERING INFORMATION

Order Number	Package	Shipping†
NTD70N03R	DPAK–3	75 Units / Rail
NTD70N03RG	DPAK–3 (Pb–Free)	75 Units / Rail
NTD70N03RT4	DPAK–3	2500 / Tape & Reel
NTD70N03RT4G	DPAK–3 (Pb–Free)	2500 / Tape & Reel
NTD70N03R–1	DPAK–3 Straight Lead	75 Units / Rail
NTD70N03R–1G	DPAK–3 Straight Lead (Pb–Free)	75 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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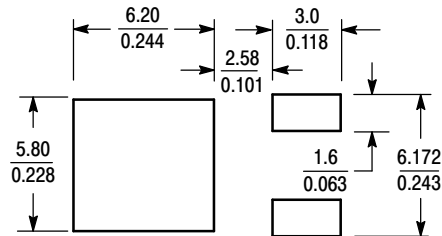## PACKAGE DIMENSIONS

DPAK
CASE 369AA–01
ISSUE A
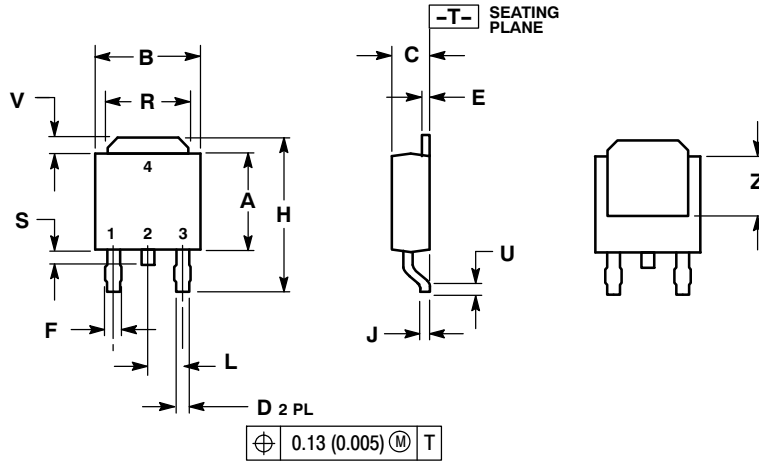
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.89
E	0.018	0.024	0.46	0.61
F	0.030	0.045	0.77	1.14
H	0.386	0.410	9.80	10.40
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.024	0.040	0.60	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:
PIN 1. GATE
    2. DRAIN
    3. SOURCE
    4. DRAIN

SOLDERING FOOTPRINT*

SCALE 3:1 $\left(\dfrac{mm}{inches}\right)$

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

DPAK
CASE 369D–01
ISSUE B
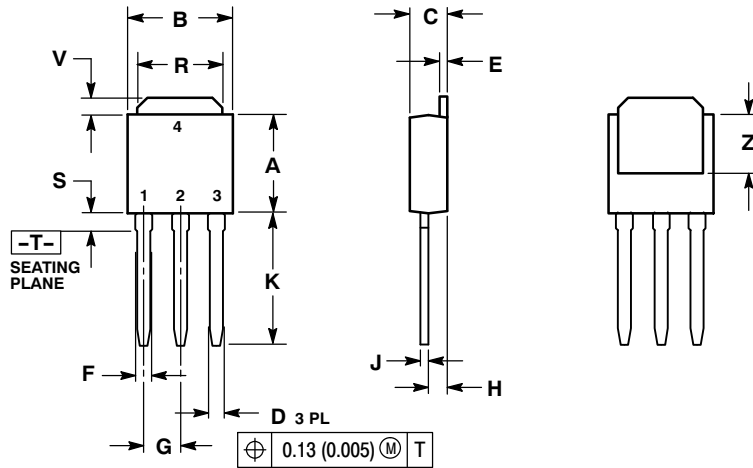
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B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN