



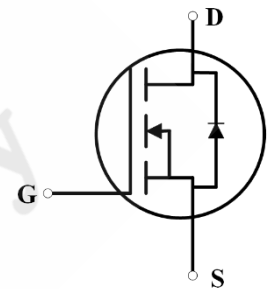
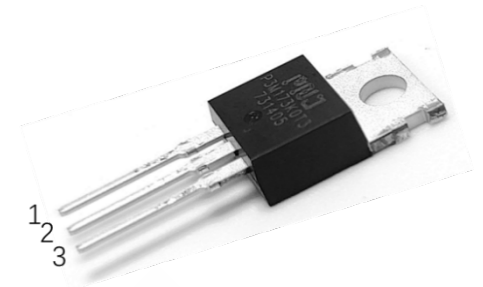
P3M06120T3 SiC MOS N-Channel Enhancement Mode

V_{RRM}	=	650	V
I_D	=	29	A
$I_D(100^\circ\text{C})$	=	21	A
$R_{DS(on)}$	=	120	mΩ

SiC MOS P3M06120T3 N-Channel Enhancement Mode

Features

- Qualified to AEC-Q101
- High Blocking Voltage with Low On-Resistance
- High-Frequency Operation
- Ultra-Small Q_{gd}
- 100% UIS tested



Benefits

- Improve System Efficiency
- Increase Power Density
- Reduce Heat Sink Requirements
- Reduction of System Cost

TO-220-3

Gate	1
Drain	2
Source	3

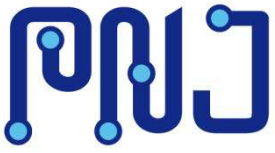
Applications

- Solar Inverters
- EV Battery Chargers
- High Voltage DC/DC Converters
- Switch Mode Power Supplies



Order Information

Part Number	Package	Marking
P3M06120T3	TO-220-3	P3M06120T3



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PNJ Preliminary



1. Maximum Ratings

At $T_J = 25^\circ\text{C}$, unless specified otherwise

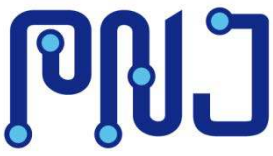
Parameter	Symbol	Value	Unit	Test Conditions
Drain - Source Voltage	V_{DSmax}	650	V	$V_{GS} = 0V$ $I_D = 100\mu A$
Gate - Source Voltage (dynamic)	V_{GSmax}	-8 / +20	V	AC ($f > 1\text{ Hz}$)
Gate - Source Voltage(static) turn-on gate voltage turn-off gate voltage	$V_{GS,on}$ $V_{GS,off}$	+15 / +18 -3	V	Static
Continuous Drain Current	I_D	29	A	$V_{GS} = 15V$ $T_C = 25^\circ\text{C}$
		21		$V_{GS} = 15V$ $T_C = 100^\circ\text{C}$
Power Dissipation	P_D	153	W	
Operating Junction	T_J	-55 To +175	$^\circ\text{C}$	
Storage Temperature	T_{stg}	-55 To +175	$^\circ\text{C}$	
Solder Temperature	T_L	260	$^\circ\text{C}$	
Mounting Torque	M_d	1 8.8	Nm lbf-in	M3 or 6-32 screw



2. Electrical Characteristics

At $T_J = 25^\circ\text{C}$, unless specified otherwise

Parameter	Symbol	Value			Unit	Test Conditions
		Min.	Typ.	Max.		
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	650	/	/	V	$V_{GS} = 0V$ $I_D = 100\mu A$
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.2	/	V	(tested after 30ms pulse at $V_{GS} = 15V$) $V_{DS} = V_{GS}$ $I_D = 5mA$ $T_J = 25^\circ\text{C}$
		/	1.65	/	V	$V_{DS} = V_{GS}$ $I_D = 5mA$ $T_J = 175^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	/	1.3	500	μA	$V_{GS} = 0V$ $V_{DS} = 650V$
Gate-Source Leakage Current	I_{GSS}	/	2	125	nA	$V_{GS} = 15V$ $V_{DS} = 0V$
Drain-Source On-State Resistance	$R_{DS(on)}$	/	120	158	m Ω	$V_{GS} = 15V$ $I_D = 10A$ $T_J = 25^\circ\text{C}$
		/	100	/		$V_{GS} = 18V$ $I_D = 10A$ $T_J = 25^\circ\text{C}$
Trans conductance	g_{fs}	/	7	/	S	$V_{DS} = 20V$ $I_{DS} = 10A$ $T_J = 25^\circ\text{C}$
		/	6.6	/		$V_{DS} = 20V$ $I_{DS} = 10A$ $T_J = 175^\circ\text{C}$



P3M06120T3 SiC MOS N-Channel Enhancement Mode

Parameter	Symbol	Value			Unit	Test Conditions
		Min.	Typ.	Max.		
Input Capacitance	C_{iss}	/	1200	/	pF	$V_{GS} = 0V$ $V_{DS} = 400V$ $f = 1MHz$ $V_{AC} = 25mV$
Output Capacitance	C_{oss}	/	85.6	/		
Reverse Transfer Capacitance	C_{rss}	/	8.6	/		
Coss Stored Energy	E_{oss}	/	14.3	/	μ	
Turn-on Energy	E_{on}	/	91	/	μ	$V_{DS} = 400V$ $V_{GS} = -3/15V$ $I_D = 10A$ $R_G = 1\Omega$
Turn-off Energy	E_{off}	/	7	/		
Turn-on Energy	E_{on}	/	80	/	μ	$V_{DS} = 400V$ $V_{GS} = -3/18V$ $I_D = 10A$ $R_G = 1\Omega$
Turn-off Energy	E_{off}	/	8	/		
Turn-On Delay Time	$t_{d(on)}$	/	15	/	ns	$V_{DS} = 400V$ $V_{GS} = -3/15V$ $I_D = 10A$ $R_G = 1\Omega$
Rise Time	t_r	/	22	/		
Turn-Off Delay Time	$t_{d(off)}$	/	20	/		
Fall Time	t_f	/	16	/		
Internal Gate Resistance	$R_{G(int)}$	/	1.3	/	Ω	$f = 1MHz$ $V_{AC} = 25mV$
Gate to Source Charge	Q_{gs}	/	9.8	/	nC	$V_{DS} = 400V$ $I_{DS} = 10A$ $V_{GS} = -3 \text{ to } 15V$ $I_G = 20mA$
Gate to Drain Charge	Q_{gd}	/	8.5	/		
Total Gate Charge	Q_g	/	31.6	/		

3. Reverse Diode Characteristics

At $T_J = 25^\circ\text{C}$, unless specified otherwise

Parameter	Symbol	Value		Unit	Test Conditions
		Typ.	Max.		
Diode Forward Voltage	V_{SD}	4.8	/	V	$V_{GS} = -3V$ $I_{SD} = 5A$ $T_J = 25^\circ\text{C}$
		4.2	/	V	$V_{GS} = -3V$ $I_{SD} = 5A$ $T_J = 175^\circ\text{C}$
Continuous Diode Forward Current	I_S	22	/	A	$V_{GS} = -3V$
Reverse Recover Time	t_{rr}	27	/	ns	$V_{GS} = -3V$ $I_{SD} = 10A$ $V_R = 400V$ $d_{if}/d_t = 2800A/\mu s$ $T_J = 25^\circ\text{C}$
Reverse Recovery Charge	Q_{rr}	195	/	nC	
Peak Reverse Recovery Current	I_{rrm}	13	/	A	
Reverse Recover Time	t_{rr}	22	/	ns	
Reverse Recovery Charge	Q_{rr}	204	/	nC	$I_{SD} = 10A$ $V_R = 400V$ $d_{if}/d_t = 3000A/\mu s$ $T_J = 25^\circ\text{C}$
Peak Reverse Recovery Current	I_{rrm}	17	/	A	

4. Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction to Case	$R_{\theta JC}$	0.98	$^\circ\text{C}/\text{W}$

5. Typical Performance

At $T_J = 25^\circ\text{C}$, unless specified otherwise

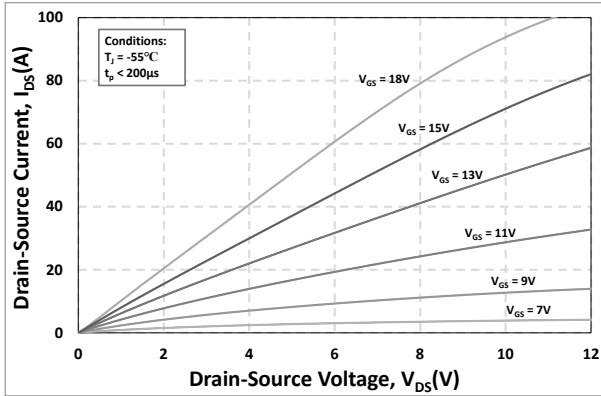


Figure 1. Output Characteristics $T_J = -55^\circ\text{C}$

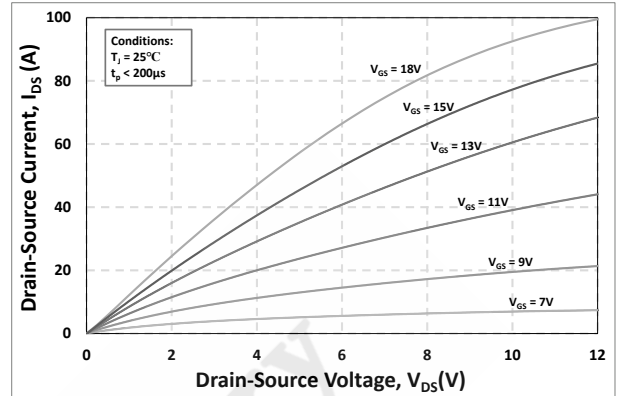


Figure 2. Output Characteristics $T_J = 25^\circ\text{C}$

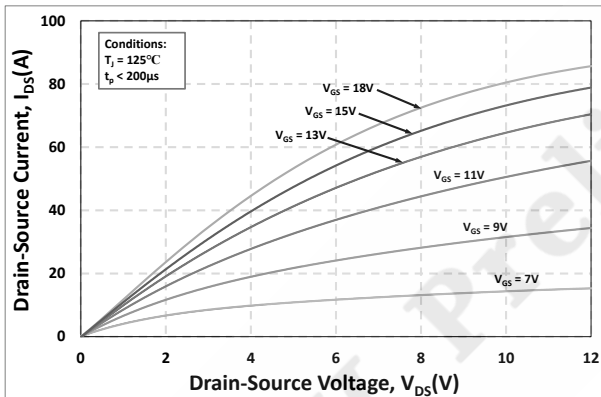


Figure 3. Output Characteristics $T_J = 125^\circ\text{C}$

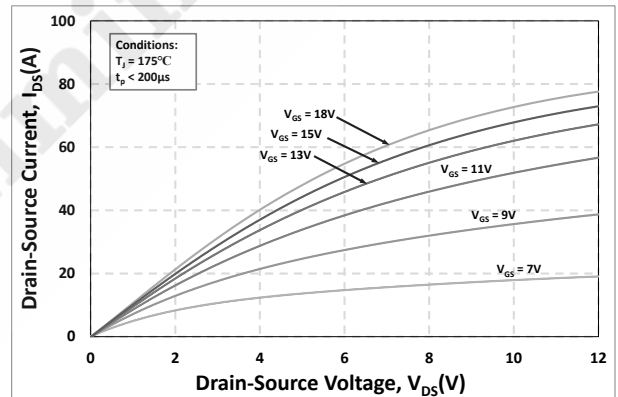


Figure 4. Output Characteristics $T_J = 175^\circ\text{C}$

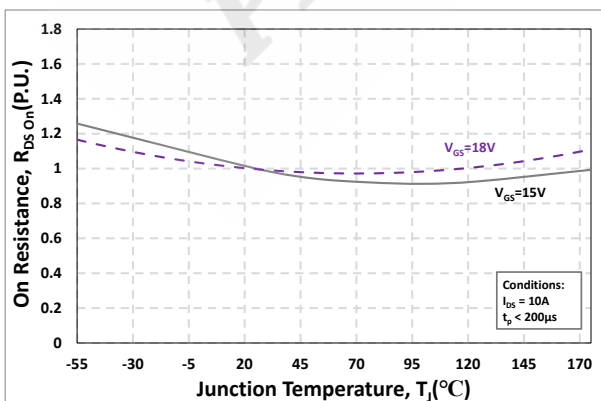


Figure 5. Normalized On-Resistance vs. Temperature

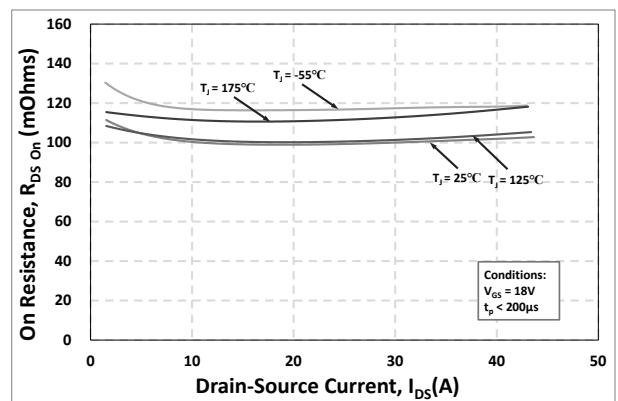


Figure 6. On-Resistance vs. Drain Current Various Temperatures

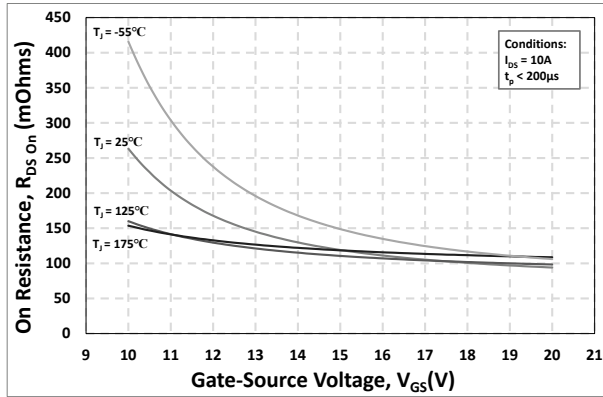


Figure 7. On-Resistance vs. Gate-Source Voltage

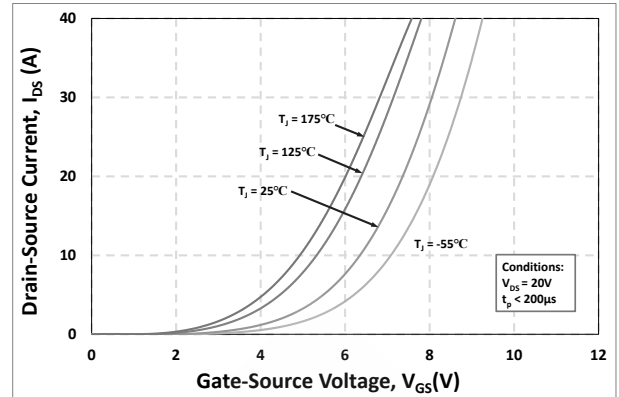


Figure 8. Transfer Characteristic for Various Junction Temperatures

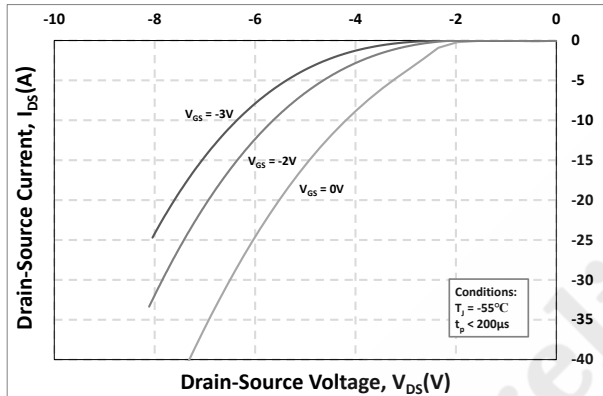


Figure 9. Body Diode Characteristic at -55°C

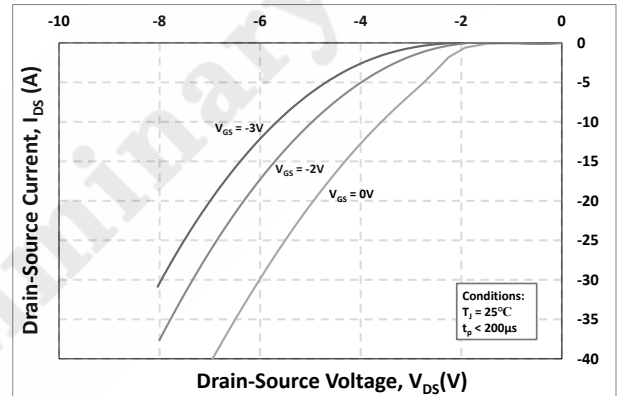


Figure 10. Body Diode Characteristic at 25°C

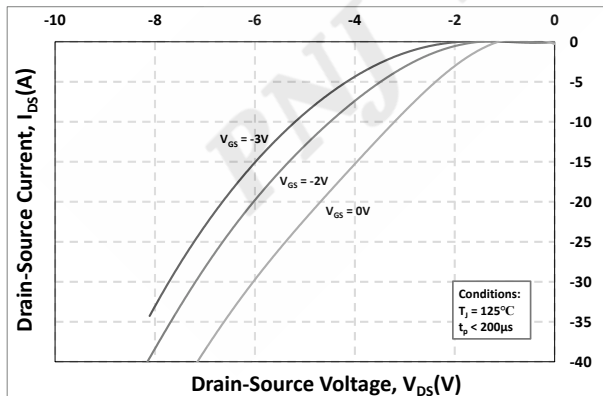


Figure 11. Body Diode Characteristic at 125°C

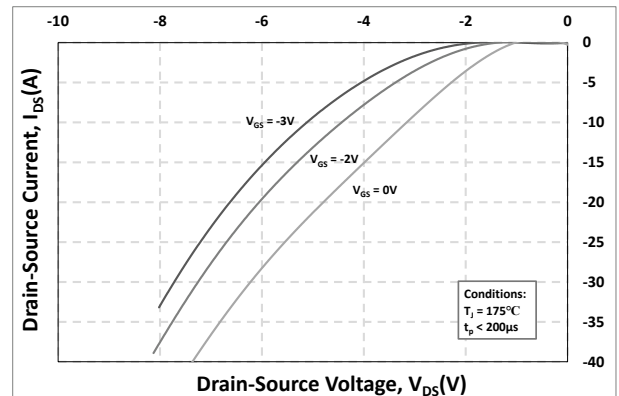


Figure 12. Body Diode Characteristic at 175°C

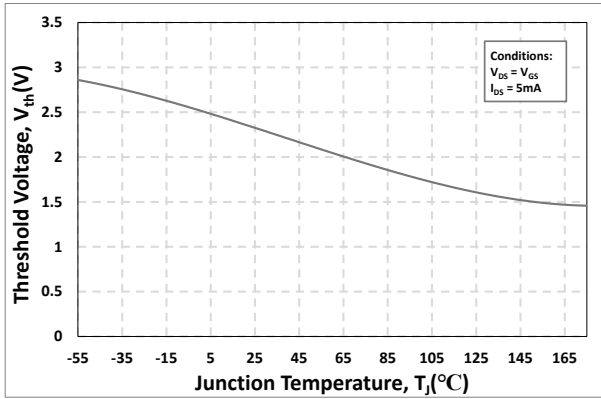


Figure 13. Threshold Voltage vs. Temperature

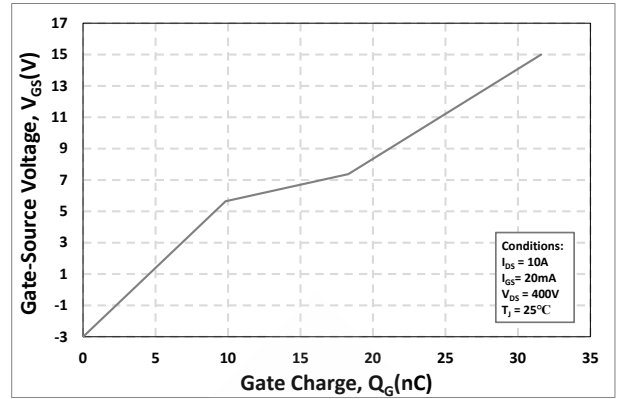


Figure 14. Gate Charge Characteristics

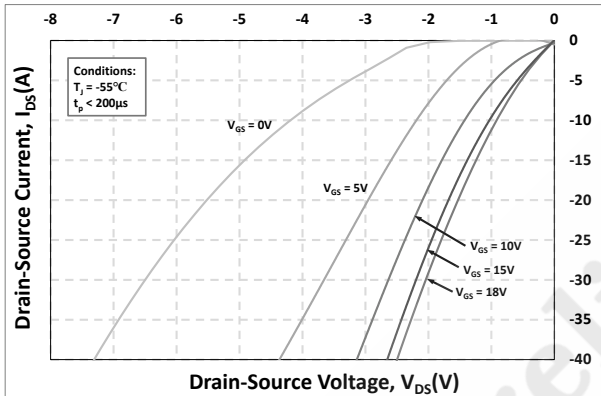


Figure 15. 3rd Quadrant Characteristic at -55°C

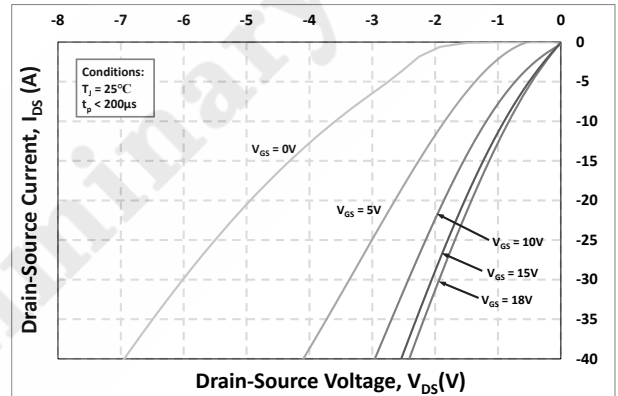


Figure 16. 3rd Quadrant Characteristic at 25°C

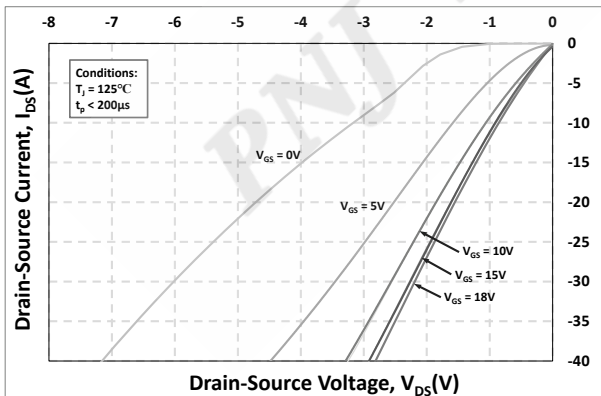


Figure 17. 3rd Quadrant Characteristic at 125°C

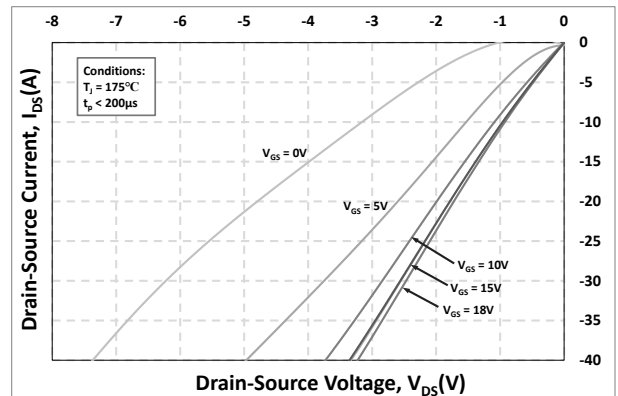
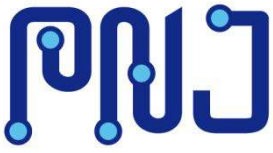


Figure 18. 3rd Quadrant Characteristic at 175°C



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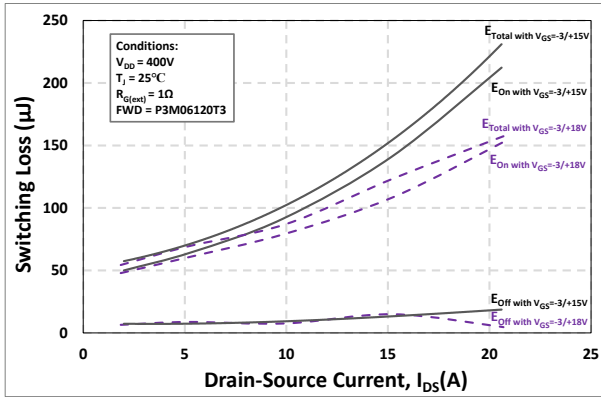


Figure 19. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 400V$)

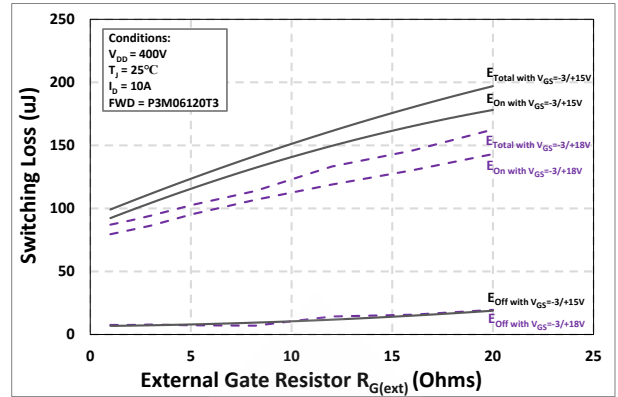


Figure 20. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

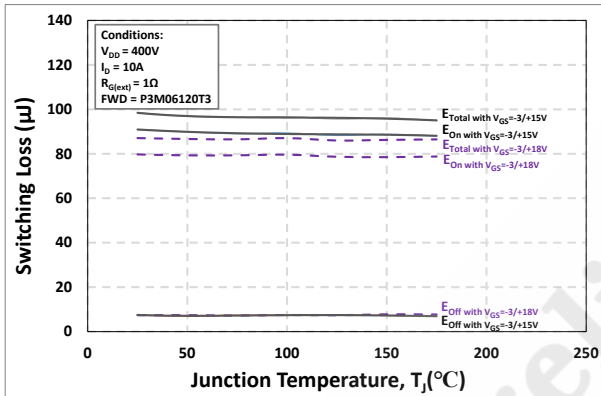


Figure 21. Clamped Inductive Switching Energy vs. Temperature

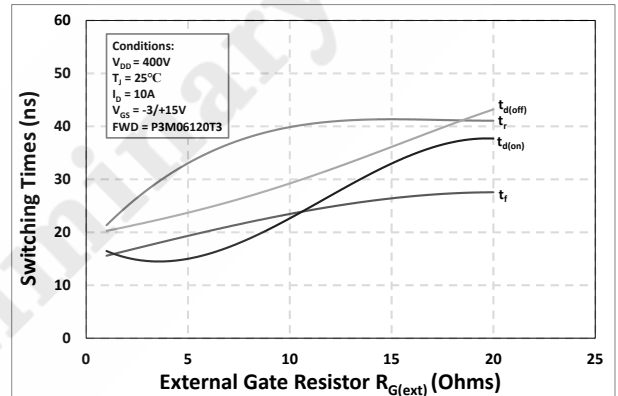


Figure 22. Switching Times vs. $R_{G(ext)}$

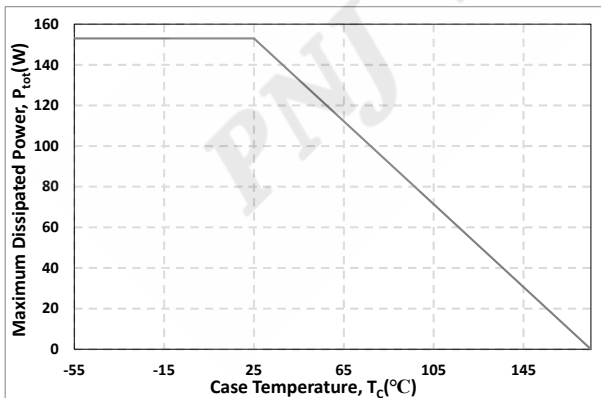


Figure 23. Maximum Power Dissipation Derating vs. Case Temperature

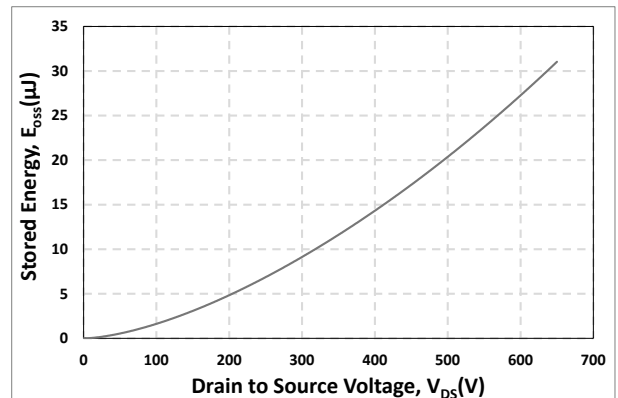


Figure 24. Output Capacitor Stored Energy

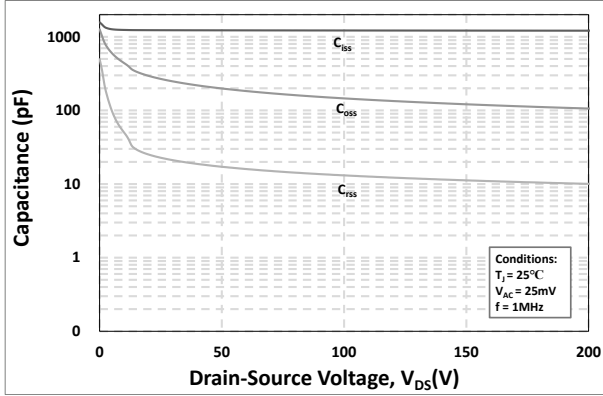


Figure 25. Capacitances vs. Drain-Source Voltage (0 - 200V)

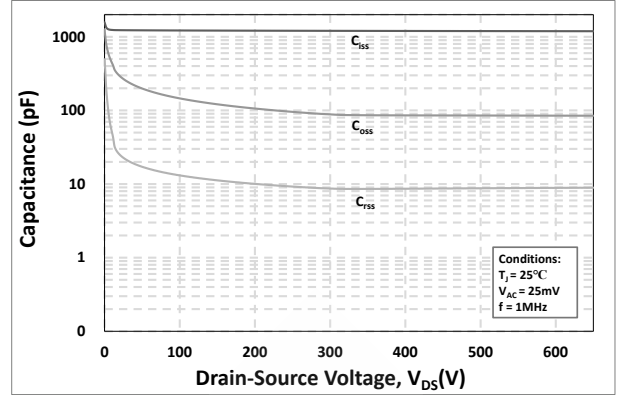


Figure 26. Capacitances vs. Drain-Source Voltage (0 - 650V)

6. Definitions

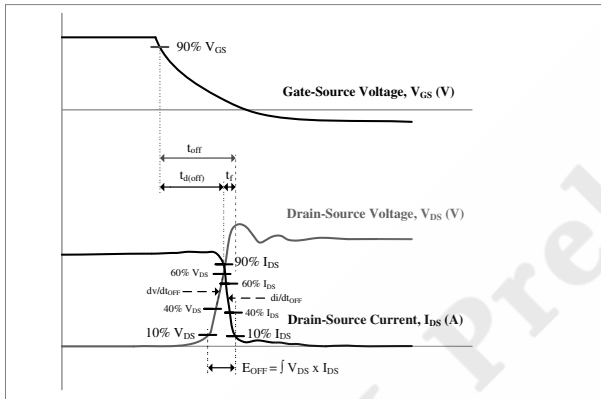


Figure 27. Turn-off Transient Definitions

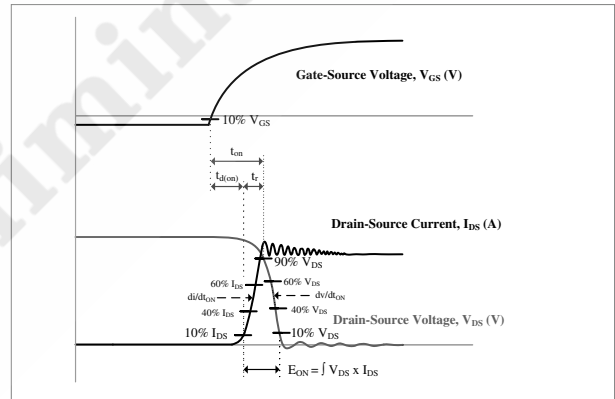


Figure 28. Turn-on Transient Definitions

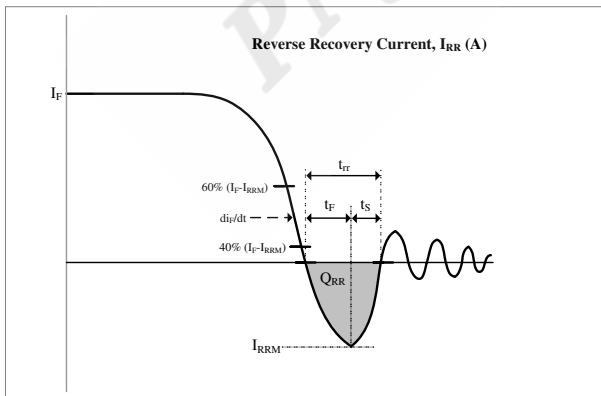


Figure 29. Reverse Recovery Definitions

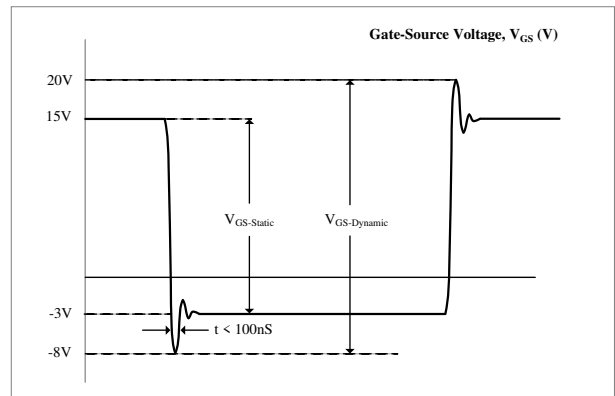
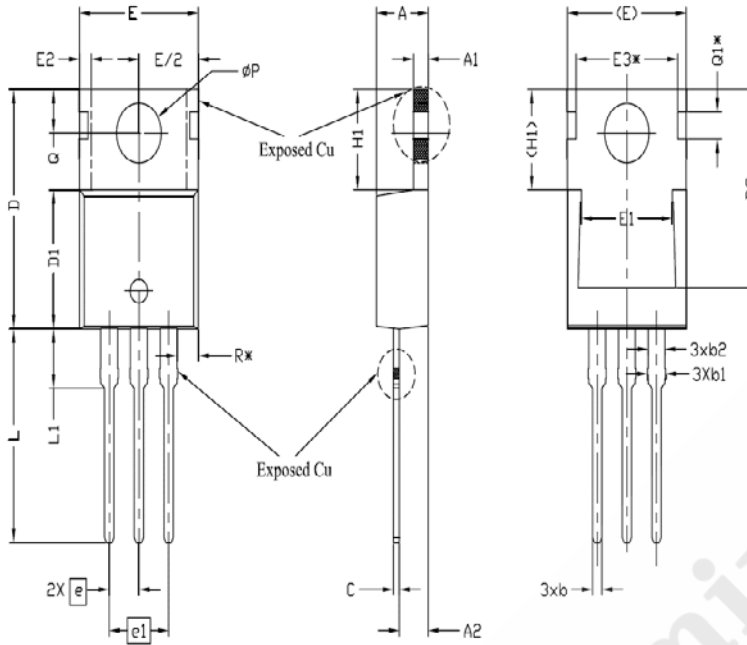


Figure 30. vGS Transient Definitions

7. Package Outlines



SYMBOL	DIMENSIONS			NOTES
	MIN.	NOM.	MAX.	
A	4.24	4.44	4.64	
A1	1.15	1.27	1.40	
A2	2.30	2.48	2.70	
b	0.70	0.80	0.90	
b1	1.20	1.55	1.75	
b2	1.20	1.45	1.70	
c	0.40	0.50	0.60	
D	14.70	15.37	16.00	4
D1	8.82	8.92	9.02	
D2	12.43	12.73	12.83	5
E	9.96	10.16	10.36	4,5
E1	6.86	7.77	8.89	5
E2	-	-	0.76	6
E3*	8.70REF.			
e	2.54BSC			
e1	5.08BSC			
H1	6.30	6.45	6.60	5,6
L	13.47	13.72	13.97	
L1	3.60	3.80	4.00	
ØP	3.75	3.84	3.93	
Q	2.60	2.80	3.00	
Q1*	1.73REF.			
R*	1.82REF.			

Drawing and Dimensions

PNJ Preliminary



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