Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR®

December 2013

FAN5353
3 MHz, 3 A Synchronous Buck Regulator

Features

- 3 MHz Fixed-Frequency Operation
- Best-in-Class Load Transient
- 3 A Output Current Capability
- 2.7 V to 5.5 V Input Voltage Range
- Adjustable Output Voltage: 0.8 V to 90% of V_{IN}
- Power Good Output
- Internal Soft-Start
- Input Under-Voltage Lockout (UVLO)
- Thermal Shutdown and Overload Protection
- 12-Lead, 3 x 3.5 mm MLP

Applications

- Set-Top Box
- Hard Disk Drive
- Communications Cards
- DSP Power

Description

The FAN5353 is a step-down switching voltage regulator that delivers an adjustable output from an input voltage supply of 2.7 V to 5.5 V. Using a proprietary architecture with synchronous rectification, the FAN5353 is capable of delivering 3 A at over 85% efficiency. The regulator operates at a nominal fixed frequency of 3 MHz, which reduces the value of the external components to 470 nH for the output inductor and 10 µF for the output capacitor. Additional output capacitance can be added without affecting stability if tighter regulation during transients is required. The regulator includes an open-drain power good (PGOOD) signal that pulls low when the output is not in regulation.

In shutdown mode, the supply current drops below 1 µA, reducing power consumption.

FAN5353 is available in a 12-lead 3x3.5 mm MLP package.

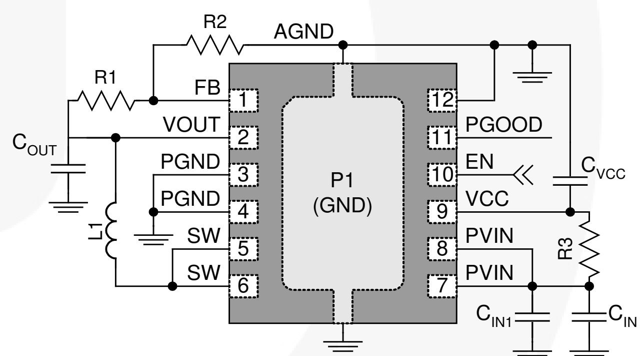

Figure 1. Typical Application

Ordering Information

Part Number	Temp. Range	Package	Packing Method
FAN5353MPX	-40 to 85°C	MLP-12, 3 x 3.5 mm	Tape and Reel

Table 1. Recommended External Components for 3 A Maximum Load Current

Component	Description	Vendor	Parameter	Typ.	Units
L1	470 nH nominal	Vishay — IHLP1616ABER47M01 Coiltronics — SD12-R47-R TDK — VLC5020T-R47N, MURATA — LQH55PNR47NT0	L	0.47	μH
			DCR	20	mΩ
C_{OUT}	2 pieces 10 μF, 6.3 V, X5R, 0805	GRM21BR60J106M (Murata) C2012X5R0J106M (TDK)	C	10.0	μF
C_{IN}	10 μF, 6.3 V, X5R, 0805				
C_{IN1}	10 nF, 25 V, X7R, 0402	GRM155R71E103K (Murata) C1005X7R1E103K (TDK)	C	10	nF
C_{VCC}	4.7 μF, 6.3 V, X5R, 0603	GRM188R60J475K (Murata) C1608X5R0J475K (TDK)	C	4.7	μF
R3(1)	Resistor: 1 Ω 0402	any	R	1	Ω

Note:
1. R3 is optional and improves IC power supply noise rejection. *See Layout recommendations for more information*.

Pin Configuration

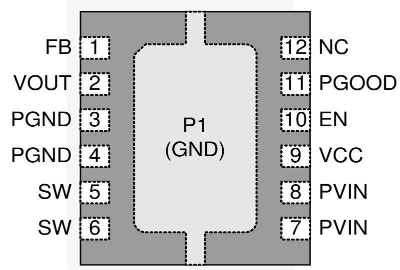

Figure 2. 12-Pin, 3 x 3.5 mm MLP (Top View)

Pin Definitions

Pin #	Name	Description
1	FB	**FB**. Connect to resistor divider. The IC regulates this pin to 0.8 V.
2	VOUT	**VOUT**. Sense pin for VOUT. Connect to COUT.
3, 4	PGND	**Power Ground**. Low-side MOSFET is referenced to this pin. CIN and COUT should be returned with a minimal path to these pins.
5, 6	SW	**Switching Node**. Connect to inductor**.**
P1	GND	**Ground**. All signals are referenced to this pin.
7, 8	PVIN	**Power Input Voltage**. Connect to input power source. Connect to CIN with minimal path.
9	VCC	**IC Bias Supply**. Connect to input power source. Use a separate bypass capacitor CVCC from this pin to the P1 GND terminal between pins 1 and 12.
10	EN	**Enable**. The device is in shutdown mode when this pin is LOW. Do not leave this pin floating.
11	PGOOD	**Power Good**. This open-drain pin pulls LOW if the output falls out of regulation or is in soft-start.
12	NC	This pin has no function and should be tied to GND.

Note:
2. P1 is the bottom heat-sink pad. Ground plane should flow through pins 3, 4, 12, and P1 and can be extended through pin 11 if PGOOD's function is not required to improve IC cooling.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	Voltage on SW, PVIN, VCC Pins	IC Not Switching	-0.3	7.0	V
		IC Switching	-0.3	6.5	
	Voltage on Other Pins		-0.3	V_{CC} + 0.3[3]	V
V_{INOV_SLEW}	Maximum Slew Rate of V_{IN} Above 6.5 V when PWM is Switching			15	V/ms
R_{PGOOD}	Pull-Up Resistance from PGOOD to VCC		1		kΩ
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114	2		kV
		Charged Device Model per JESD22-C101	2		
T_J	Junction Temperature		–40	+150	°C
T_{STG}	Storage Temperature		–65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Note:
3. Lesser of 7 V or V_{CC}+0.3 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}, V_{IN}	Supply Voltage Range	2.7		5.5	V
V_{OUT}	Output Voltage Range	0.8		90% Duty Cycle	V
I_{OUT}	Output Current	0		3	A
L	Inductor		0.47		µH
C_{IN}	Input Capacitor		10		µF
C_{OUT}	Output Capacitor		20		µF
T_A	Operating Ambient Temperature	-40		+85	°C
T_J	Operating Junction Temperature	-40		+125	°C

Thermal Properties

Symbol	Parameter	Min.	Typ.	Max.	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance[4]		46		°C/W

Note:
4. Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 1s2p boards in accordance to JESD51- JEDEC standard. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperate T_A.

Electrical Characteristics

Minimum and maximum values are at V_{IN} = 2.7 V to 5.5 V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C, V_{IN} =5 V.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Supplies						
I_Q	Quiescent Current	I_{LOAD} = 0, V_{OUT}=1.2 V		14		mA
I_{SD}	Shutdown Supply Current	EN = GND		0.1	3.0	µA
V_{UVLO}	Under-Voltage Lockout Threshold	V_{IN} Rising		2.83	2.95	V
		V_{IN} Falling	2.10	2.30	2.40	V
V_{UVHYST}	Under-Voltage Lockout Hysteresis			530		mV
Logic Pins						
V_{IH}	HIGH-Level Input Voltage		1.05			V
V_{IL}	LOW-Level Input Voltage				0.4	V
V_{LHYST}	Logic Input Hysteresis Voltage			100		mV
I_{IN}	Input Bias Current	Input tied to GND or V_{IN}		0.01	1.00	µA
I_{OUTL}	PGOOD Pull-Down Current	V_{PGOOD} = 0.4 V			1	mA
I_{OUTH}	PGOOD HIGH Leakage Current	V_{PGOOD} = V_{IN}		0.01	1.00	µA
VOUT Regulation						
V_{REF}	Output Reference DC Accuracy Measured at FB Pin	T_A = 25°C	0.792	0.800	0.808	V
			0.788	0.800	0.812	V
V_{REG}	V_{OUT} DC Accuracy	At VOUT pin W.R.T. Calculated Value, I_{LOAD} = 500 mA	1.6%		+1.6	%
$\frac{\Delta V_{OUT}}{\Delta I_{LOAD}}$	Load Regulation	$I_{OUT(DC)}$ = 0 to 3 A		–0.03		%/A
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	2.7 V ≤ V_{IN} ≤ 5.5 V, $I_{OUT(DC)}$ = 1.5 A		0.01		%/V
	Transient Response	I_{LOAD} step 0.1 A to 1.5 A, $t_r = t_f$ = 100 ns, V_{OUT}=1.2 V		±20		mV
Power Switch and Protection						
$R_{DS(ON)P}$	P-channel MOSFET On Resistance			60		mΩ
$R_{DS(ON)N}$	N-channel MOSFET On Resistance			40		mΩ
I_{LIMPK}	P-MOS Peak Current Limit		3.75	4.55	5.50	A
T_{LIMIT}	Thermal Shutdown			150		°C
T_{HYST}	Thermal Shutdown Hysteresis			20		°C
V_{SDWN}	Input OVP Shutdown	Rising Threshold		6.2		V
		Falling Threshold	5.50	5.85		V
Frequency Control						
f_{SW}	Oscillator Frequency		2.7	3.0	3.3	MHz
Soft-Start						
t_{SS}	Regulator Enable to Regulated V_{OUT}	R_{LOAD} ≥ 5 Ω, to V_{OUT} = 1.2 V		210	250	µs
		R_{LOAD} ≥ 5 Ω, to V_{OUT} = 1.8 V		340	420	µs
V_{SLEW}	Soft-Start V_{OUT} Slew Rate			10		V/ms

Typical Characteristics

Unless otherwise specified, V_{IN} = 5 V, V_{OUT} = 1.2 V, circuit of Figure 1, and components per Table 1.

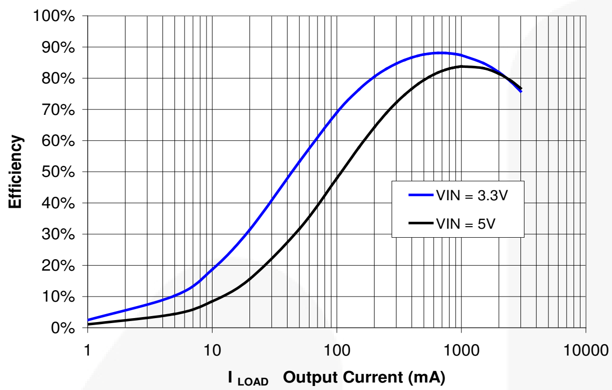

Figure 3. Efficiency vs. I_{LOAD} at V_{OUT} = 1.2 V

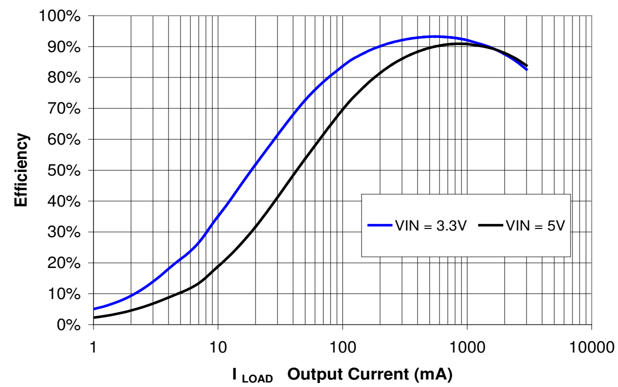

Figure 4. Efficiency vs. I_{LOAD} at V_{OUT} = 1.8 V

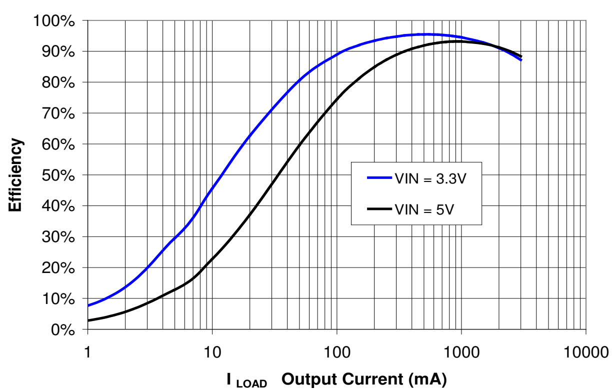

Figure 5. Efficiency vs. I_{LOAD} at V_{OUT} = 2.5 V

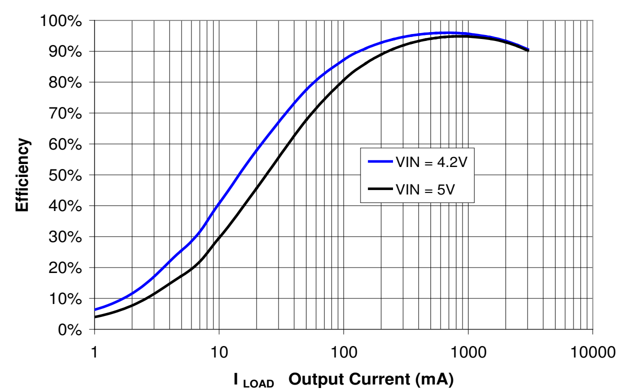

Figure 6. Efficiency vs. I_{LOAD} at V_{OUT} = 3.3 V

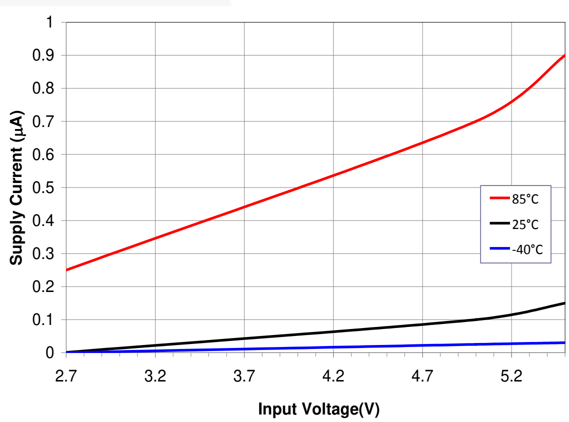

Figure 7. Shutdown Supply Current vs. V_{IN}, EN to 0 V

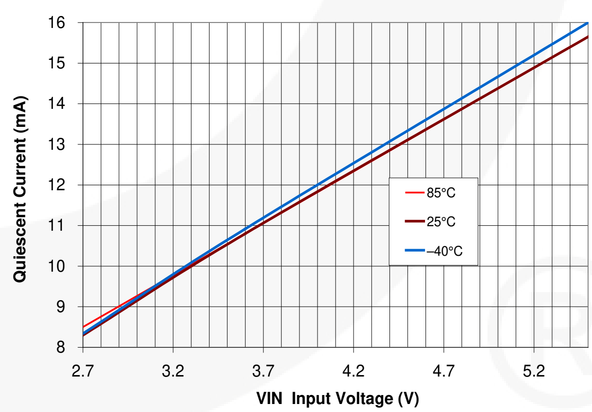

Figure 8. Quiescent Current vs. V_{IN}, No Load

Typical Characteristics

Unless otherwise specified, V_{IN} = 5 V, V_{OUT} = 1.2 V, circuit of Figure 1, and components per Table 1.

Figure 9. Load Transient Response: 100 mA to 1.5 A to 100 mA, t_r=t_f=100 ns, Horizontal Scale = 5 µs/div.

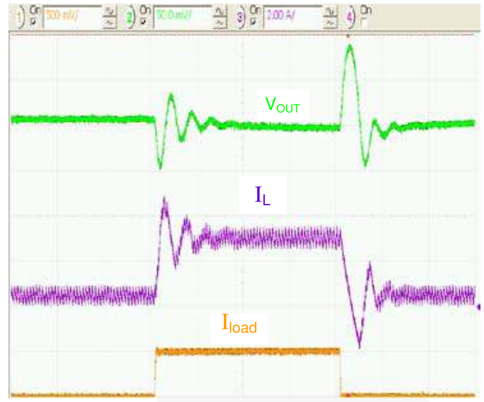

Figure 10. Load Transient Response: 500 mA to 3 A to 500 mA, t_r=t_f=100 ns, Horizontal Scale = 5 µs/div.

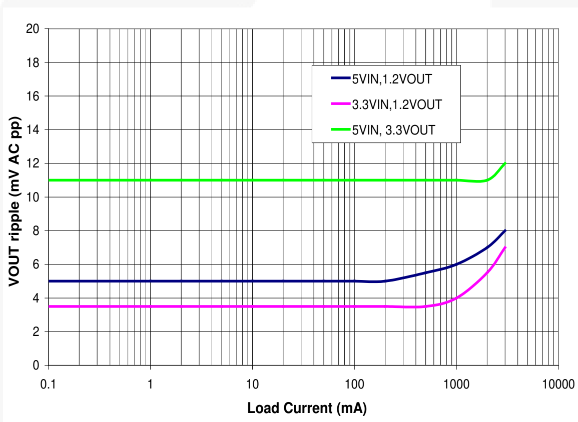

Figure 11. Output Voltage Ripple vs. Load Current

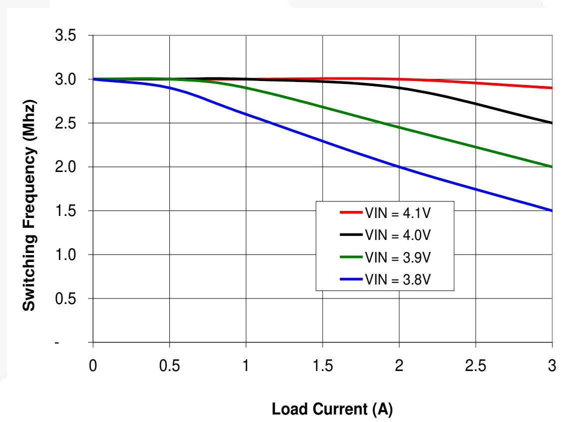

Figure 12. Effect of t_{OFF} Minimum on Reducing the Switching Frequency at Large Duty Cycles, V_{OUT} = 3.3 V

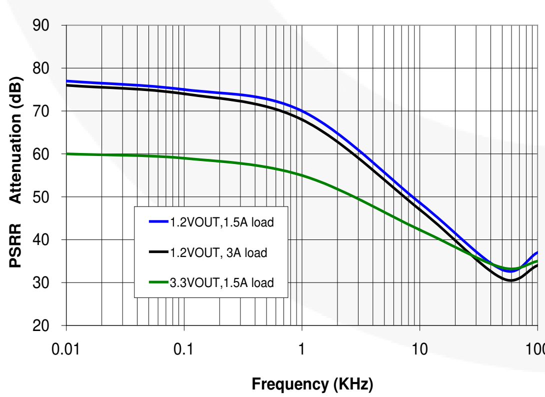

Figure 13. Power Supply Rejection Ratio

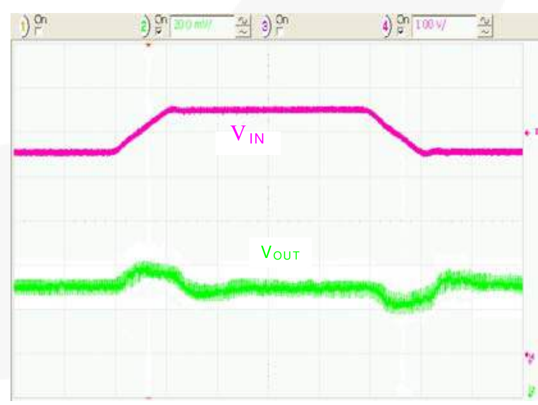

Figure 14. Line Transient Response with 1 A load, 10 µs/div.

Typical Characteristics

Unless otherwise specified, V_{IN} = 5 V, V_{OUT} = 1.2 V, circuit of Figure 1, and components per Table 1.

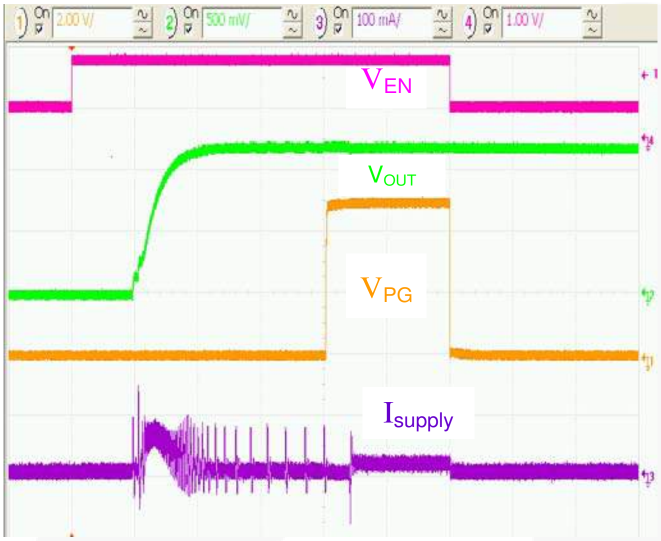

Figure 15. Soft-Start: EN Voltage Raised After V_{IN} =5.0 V, I_{LOAD} = 0, Horizontal Scale = 100 µs/div.

Figure 16. Soft-Start: EN Pin Tied to VCC, I_{LOAD} = 0, Horizontal Scale = 1 ms/div.

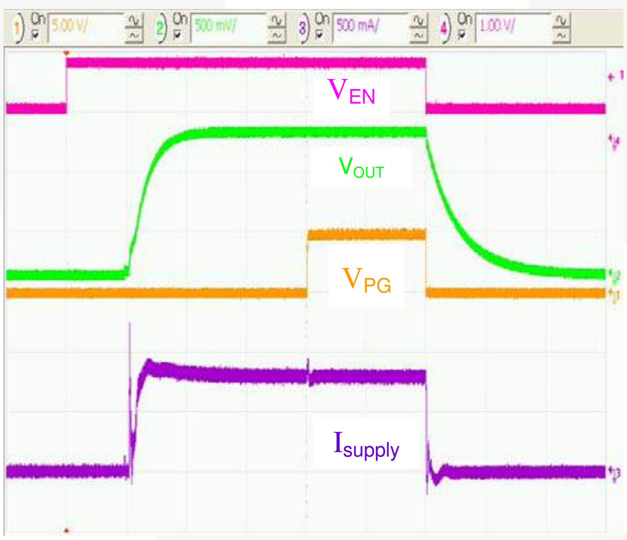

Figure 17. Soft-Start: EN Pin Raised after V_{IN} = 5.0 V, R_{LOAD} = 400 mΩ. C_{OUT} = 100 µF, Horizontal Scale = 100µs/div.

Figure 18. Soft-Start: EN Pin Tied to VCC, R_{LOAD} = 400 mΩ, C_{OUT} = 100 µF, Horizontal Scale = 1 ms/div.

Typical Characteristics

Unless otherwise specified, V_{IN} = 5 V, V_{OUT} = 1.2 V, circuit of Figure 1, and components per Table 1.

Figure 19. VOUT to GND Short Circuit, 200 µs/div.

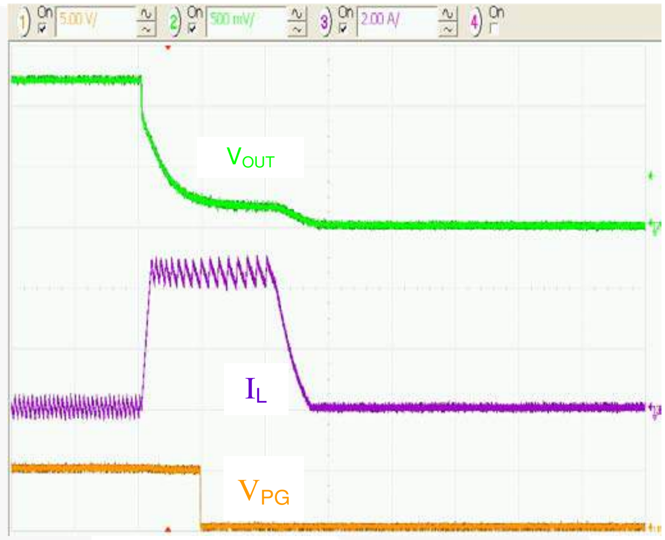

Figure 20. VOUT to GND Short Circuit, 5 µs/div.

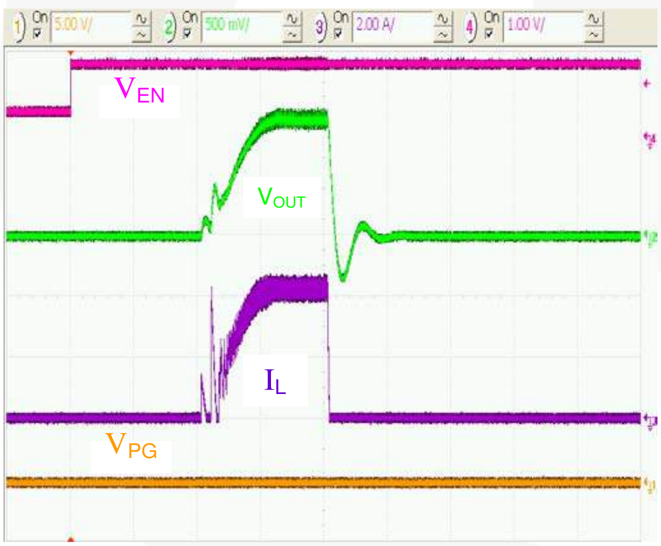

Figure 21. Over-Current at Startup: R_{LOAD} = 200 mΩ., 50 µs/div.

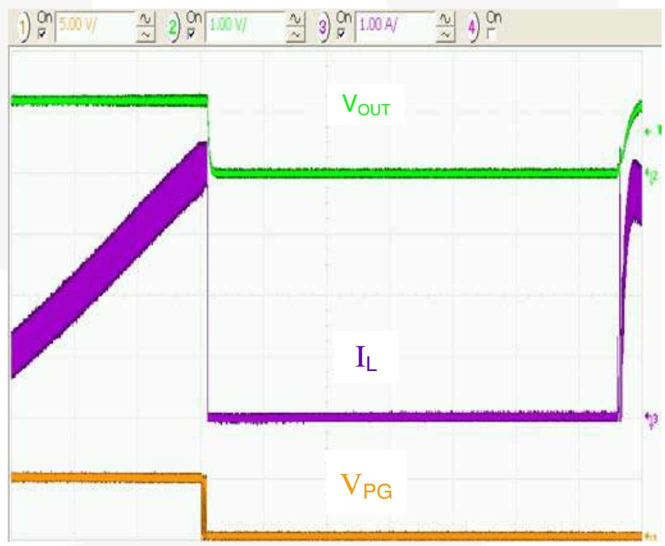

Figure 22. Progressive Overload, 200 µs/div.

Operation Description

The FAN5353 is a step-down switching voltage regulator that delivers an adjustable output from an input voltage supply of 2.7 V to 5.5 V. Using a proprietary architecture with synchronous rectification, the FAN5353 is capable of delivering 3 A at over 80% efficiency. The regulator operates at a nominal frequency of 3 MHz at full load, which reduces the value of the external components to 470 nH for the output inductor and 20 µF for the output capacitor.

Control Scheme

The FAN5353 uses a proprietary non-linear, fixed-frequency PWM modulator to deliver a fast load transient response, while maintaining a constant switching frequency over a wide range of operating conditions. The regulator performance is independent of the output capacitor ESR, allowing for the use of ceramic output capacitors. Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency loop holds the switching frequency constant over a large range of input voltages and load currents.

Setting the Output Voltage

The output voltage is set by the R1, R2, and V_{REF} (0.8 V):

$$\frac{R1}{R2} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \qquad (1)$$

R1 must be set at or below 100 kΩ. Therefore:

$$R2 = \frac{R1 \bullet 0.8}{(V_{OUT} - 0.8)} \qquad (2)$$

For example, for V_{OUT} = 1.2 V, R1 = 100 kΩ, R2 = 200 kΩ.

Enable and Soft Start

When the EN pin is LOW, the IC is shut down, all internal circuits are off, and the part draws very little current. Raising EN above its threshold voltage activates the part and starts the soft-start cycle. During soft-start, the modulator’s internal reference is ramped slowly to minimize any large surge currents on the input and prevents any overshoot of the output voltage.

If large values of output capacitance are used, the regulator may fail to start. If V_{OUT} fails to achieve regulation within 320 µs from the beginning of soft-start, the regulator shuts down and waits 1200 µs before attempting a restart. If the regulator is at its current limit for more than about 60 µs, the regulator shuts down before restarting 1200 µs later. This limits the C_{OUT} capacitance when a heavy load is applied during the startup. For a typical FAN5353 starting with a resistive load:

$$COUT_{MAX}(\mu F) \approx 400 - 100 * I_{LOAD}(A)$$

where $I_{LOAD} = \frac{V_{OUT}}{R_{LOAD}}$ (3)

Synchronous rectification is inhibited during soft-start, allowing the IC to start into a pre-charged load.

PGOOD Pin

The PGOOD pin is an open drain output that indicates the IC is in regulation when its state is open. PGOOD requires an external pull-up resistor. PGOOD pulls LOW under the following conditions:

1. The IC has operated in cycle-by-cycle current limit for eight or more consecutive PWM cycles.
2. The circuit is disabled; either after a fault occurs, or when EN is LOW.
3. The IC is performing a soft-start.

Under-Voltage Lockout

When EN is HIGH, the under-voltage lockout keeps the part from operating until the input supply voltage rises high enough to properly operate. This ensures no misbehavior of the regulator during startup or shutdown.

Input Over-Voltage Protection (OVP)

When V_{IN} exceeds V_{SDWN} (about 6.2 V) the IC stops switching, to protect the circuitry from internal spikes above 6.5 V. An internal 40 µs filter prevents the circuit from shutting down due to noise spikes. For the circuit to fully protect the internal circuitry, the V_{IN} slew rate above 6.2 V must be limited to no more than 15 V/ms when the IC is switching.

The IC protects itself if V_{IN} overshoots to 7 V during initial power-up as long as the V_{IN} transition from 0 to 7 V occurs in less than 10 µs (10% to 90%).

Current Limiting

A heavy load or short circuit on the output causes the current in the inductor to increase until a maximum current threshold is reached in the high-side switch. Upon reaching this point, the high-side switch turns off, preventing high currents from causing damage. 16 consecutive PWM cycles in current limit cause the regulator to shut down and stay off for about 1200µs before attempting a restart.

In the event of a short circuit, the soft-start circuit attempts to restart and produces an over-current fault after about 50 µs, which results in a duty cycle of less than 10%, providing current into a short circuit.

Thermal Shutdown

When the die temperature increases, due to a high load condition and/or a high ambient temperature, the output switching is disabled until the temperature on the die has fallen sufficiently. The junction temperature at which the thermal shutdown activates is nominally 150°C with a 20°C hysteresis.

Minimum Off-Time Effect on Switching Frequency

$t_{ON(MIN)}$ and $t_{OFF(MIN)}$ are both 45 ns. This imposes constraints on the maximum $\frac{VOUT}{VIN}$ that the FAN5353 can provide, while still maintaining a fixed switching frequency in PWM mode. While regulation is unaffected, the switching frequency drops when the regulator cannot provide sufficient duty cycle at 3 MHz to maintain regulation.

The calculation for switching frequency is given as:

$$f_{SW} = \min\left(\frac{1}{t_{SW(MAX)}}, \frac{1}{333.3ns}\right) \quad (4)$$

where:

$$t_{SW(MAX)} = 45ns \bullet \left(1 + \frac{V_{OUT} + I_{OUT} \bullet R_{OFF}}{V_{IN} - I_{OUT} \bullet R_{ON} - V_{OUT}}\right)$$

$$R_{OFF} = R_{DSON\_N} + DCR_L$$

$$R_{ON} = R_{DSON\_P} + DCR_L$$

Applications Information

Selecting the Inductor

The output inductor must meet both the required inductance and the energy handling capability of the application. The inductor value affects the average current limit, the output voltage ripple, and the efficiency.

The ripple current (ΔI) of the regulator is:

$$\Delta I \approx \frac{V_{OUT}}{V_{IN}} \bullet \left(\frac{V_{IN} - V_{OUT}}{L \bullet f_{SW}}\right) \quad (5)$$

The maximum average load current, $I_{MAX(LOAD)}$ is related to the peak current limit, $I_{LIM(PK)}$by the ripple current as:

$$I_{MAX(LOAD)} = I_{LIM(PK)} - \frac{\Delta I}{2} \quad (6)$$

The FAN5353 is optimized for operation with L=470 nH, but is stable with inductances up to 1.2 µH (nominal). The inductor should be rated to maintain at least 80% of its value at $I_{LIM(PK)}$. Failure to do so lowers the amount of DC current the IC can deliver.

Efficiency is affected by the inductor DCR and inductance value. Decreasing the inductor value for a given physical size typically decreases the DCR; but since ΔI increases, the RMS current increases, as do core and skin effect losses.

$$I_{RMS} = \sqrt{I_{OUT(DC)}^{\,2} + \frac{\Delta I^2}{12}} \quad (7)$$

The increased RMS current produces higher losses through the $R_{DS(ON)}$ of the IC MOSFETs as well as the inductor ESR.

Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

Table 2 shows the effects of inductance higher or lower than the recommended 470 nH on regulator performance.

Table 2. Effects of Increasing the Inductor Value (from 470nH recommended value) on Regulator Performance

$I_{MAX(LOAD)}$	ΔV_{OUT} (EQ. 8)	Transient Response
Increase	Decrease	Degraded

Inductor Current Rating

The FAN5353's current limit circuit can allow a peak current of 5.5 A to flow through L1 under worst-case conditions. If it is possible for the load to draw that much continuous current, the inductor should be capable of sustaining that current or failing in a safe manner.

For space-constrained applications, a lower current rating for L1 can be used. The FAN5353 may still protect these inductors in the event of a short circuit, but may not be able to protect the inductor from failure if the load is able to draw higher currents than the DC rating of the inductor.

Output Capacitor

Table 1 suggests 0805 capacitors, but 0603 capacitors may be used if space is at a premium. Due to voltage effects, the 0603 capacitors have a lower in-circuit capacitance than the 0805 package, which can degrade transient response and output ripple.

Increasing C_{OUT} has no effect on loop stability and can therefore be increased to reduce output voltage ripple or to improve transient response. Output voltage ripple, ΔV_{OUT}, is:

$$\Delta V_{OUT} = \Delta I \bullet \left(\frac{1}{8 \bullet C_{OUT} \bullet f_{SW}} + ESR\right) \quad (8)$$

where C_{OUT} is the effective output capacitance. The capacitance of C_{OUT} decreases at higher output voltages, which results in higher ΔV_{OUT} .

If C_{OUT} is greater than 100 µF, the regulator may fail to start under load.

If an inductor value greater than 1.0 µH is used, at least 30 µF of C_{OUT} should be used to ensure stability.

ESL Effects

The ESL (Equivalent Series Inductance) of the output capacitor network should be kept low to minimize the square wave component of output ripple that results from the division ratio C_{OUT}'s ESL and the output inductor (L_{OUT}). The square wave component due to ESL can be estimated as:

$$\Delta V_{OUT(SQ)} \approx V_{IN} \bullet \frac{ESL_{COUT}}{L1} \quad (9)$$

A good practice to minimize this ripple is to use multiple output capacitors to achieve the desired C_{OUT} value. For example, to obtain C_{OUT} = 20 µF, a single 22 µF 0805 would produce twice the square wave ripple of 2 x 10 µF 0805.

To minimize ESL, try to use capacitors with the lowest ratio of length to width. 0805s have lower ESL than 1206s. If low output ripple is a chief concern, some vendors produce 0508 or 0612 capacitors with ultra-low ESL. Placing additional small value capacitors near the load also reduces the high-frequency ripple components.

Input Capacitor

The 10µF ceramic input capacitor should be placed as close as possible between the VIN pin and PGND to minimize the parasitic inductance. If a long wire is used to bring power to the IC, additional "bulk" capacitance (electrolytic or tantalum) should be placed between C_{IN} and the power source lead to reduce under-damped ringing that can occur between the inductance of the power source leads and C_{IN}.

The effective C_{IN} capacitance value decreases as V_{IN} increases due to DC bias effects. This has no significant impact on regulator performance.

Layout Recommendations

The layout recommendations below highlight various top-copper planes by using different colors. It includes COUT3 to demonstrate how to add C_{OUT} capacitance to reduce ripple and transient excursions. The inductor in this example is the TDK VLC5020T-R47N.

VCC and VIN should be connected together by a thin trace some distance from the IC, or through a resistor (shown as R3 below), to isolate the switching spikes on PVIN from the IC bias supply on VCC. If PCB area is at a premium, the connection between PVIN and VCC can be made on another PCB layer through vias. The via impedance provides some filtering for the high-frequency spikes generated on PVIN.

PGND and AGND connect through the thermal pad of the IC. Extending the PGND and AGND planes improves IC cooling. The IC analog ground (AGND) is bonded to P1 between pins 1 and 12. Large AC ground currents should return to pins 3 and 4 (PGND) either through the copper under P1 between pins 6 and 7 or through a direct trace from pins 3 and 4 (as shown for COUT1-COUT3).

EN and PGOOD connect through vias to the system control logic.

CIN1 is an optional device used to provide a lower impedance path for high-frequency switching edges/spikes, which helps to reduce SW node and VIN ringing. CIN should be placed as close as possible between PGND and VIN, as shown below.

PGND connection back to inner planes should be accomplished as series of vias distributed among the COUT return track and CIN return plane between pins 6 and 7.

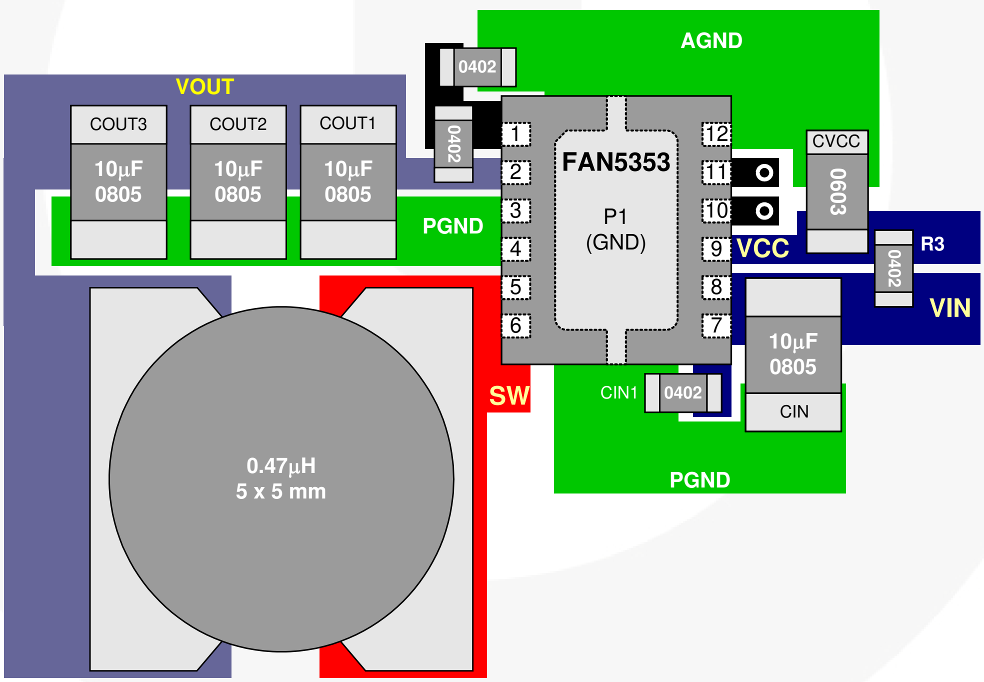

Figure 23. 3 A Layout Recommendation

Physical Dimensions

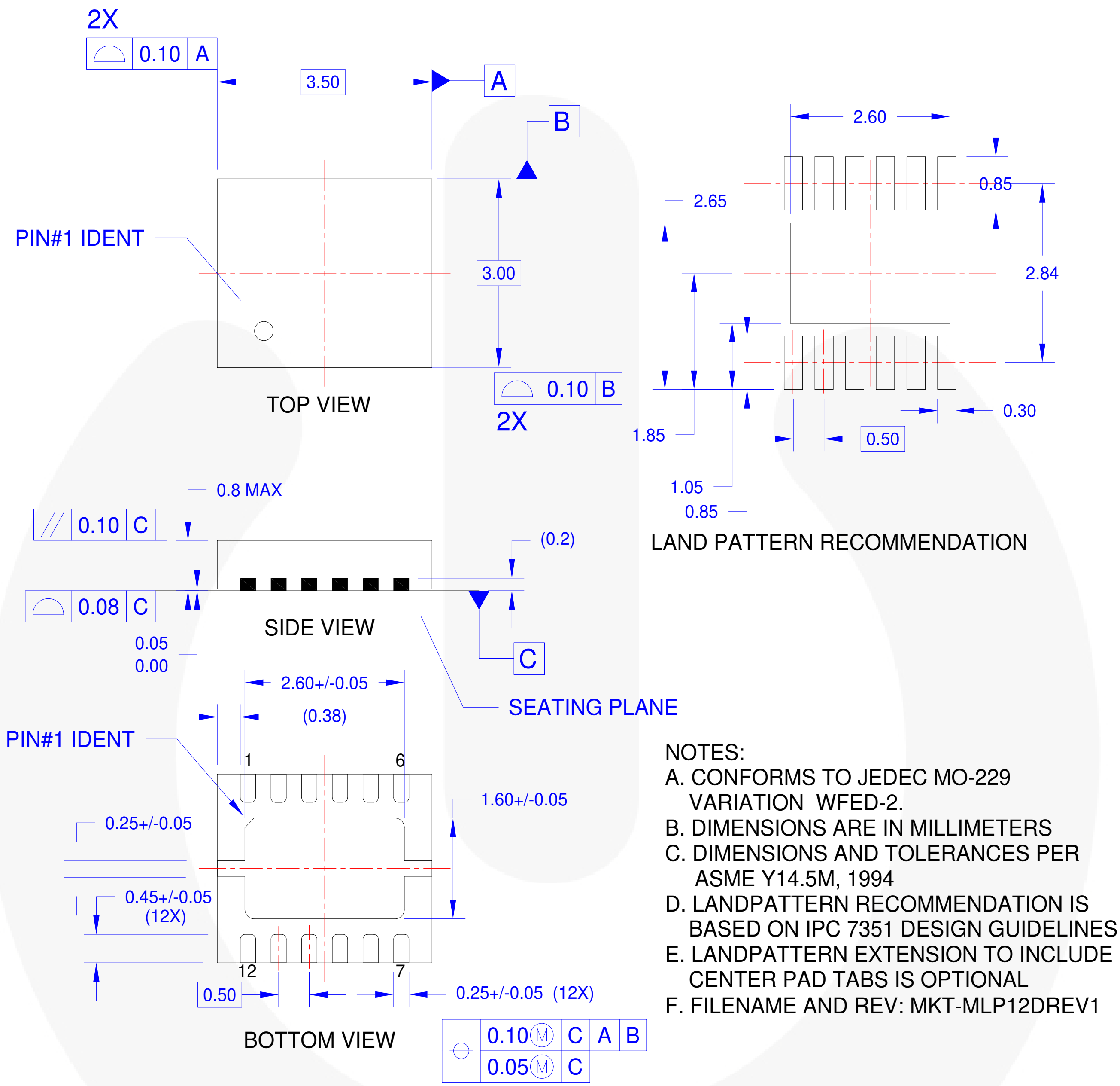

Figure 24. 12-Lead, 3x3.5 mm Molded Leadless Package (MLP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/dwg/ML/MLP12D.pdf.

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™
AX-CAP®*
BitSiC™
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficientMax™
ESBC™
F®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FPS™
F-PFS™
FRFET®
Global Power Resource℠
GreenBridge™
Green FPS™
Green FPS™ e-Series™
G*max*™
GTO™
IntelliMAX™
ISOPLANAR™
Making Small Speakers Sound Louder and Better™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
mWSaver®
OptoHiT™
OPTOLOGIC®
OPTOPLANAR®
®
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
Solutions for Your Success™
SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
SYSTEM GENERAL®*
TinyBoost®
TinyBuck®
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC™
TriFault Detect™
TRUECURRENT®*
μSerDes™
μSerDes™
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
VoltagePlus™
XS™

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I66

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative