AN2451
Application note

ST7540 FSK powerline transceiver design guide for AMR

Introduction

The ST7540 reference design has been developed as a useful tool to demonstrate how a small, high-performance powerline node can be built using the ST7540 FSK transceiver.

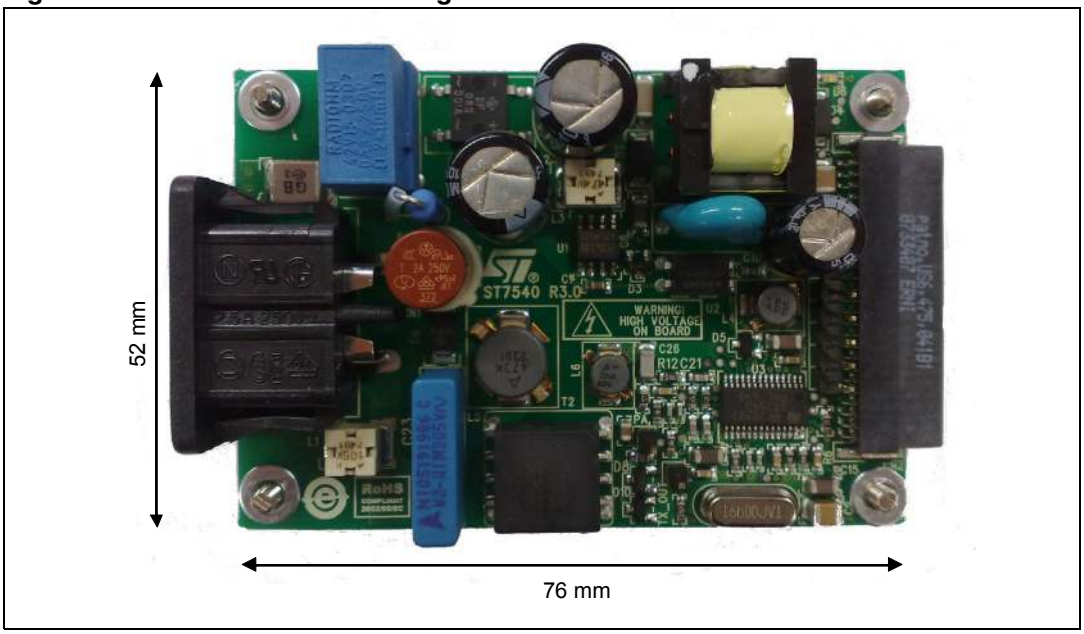
With this reference design, it is possible to evaluate the ST7540 features, in particular, its transmitting and receiving performances through actual communication on the power line.

The ST7540 reference design may be considered to be composed of three main sections:

- Power supply section, specifically tailored to match powerline coupling requirements and to operate within a wide range of the input mains voltage
- Modem and crystal oscillator section
- Line coupling interface section

The coupling interface is designed to allow the ST7540 FSK transceiver to transmit and receive on the mains using 72 kHz carrier frequencies, within the European CENELEC standard A-band specified for automatic meter reading.

Figure 1. ST7540 reference design board with outline dimensions



As it can be seen from the picture above, a special effort has been made to obtain a very compact reference design board, while keeping the focus on transmission and receiving performances.

Note: The information provided in this application note refers to EVALST7540-2 reference design board.

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1 Electrical characteristics

Table 1. Electrical characteristics of the ST7540 reference design

Parameter	Test conditions	Value			Unit
		Min	Typ	Max	
Operating conditions					
Ambient operating temperature	If ST7540 junction temperature exceeds 180 °C device shuts down			85	°C
Transceiver section transmitting specifications (Tx mode)					
Selected channel frequency	FSK carrier		72		kHz
Transmitting output voltage level at mains output	R7 = 47kΩ, R8 = 15kΩ – See Table 2		2	2.25	V rms
Transmitting output current limit	R6=1.1kΩ – See Figure 2		500		mA rms
2^{nd} harmonic distortion at mains output	Loaded with CISPR 16-1 network			-55	dB_C
3^{rd} harmonic distortion at mains output	Loaded with CISPR 16-1 network			-61	
50Hz attenuation			100		dB
Receiving specifications (Rx mode)					
Minimum detectable Rx signal	BER<10^{-3}, negligible noise		48		dBµV rms
Auxiliary supply					
5 V regulated voltage	ST7540 internally generated	-5%	5.05	+5%	V
5 V current capability				50	mA
3.3 V regulated voltage	ST7540 internally generated	-5%	3.3	+5%	V
3.3 V current capability				50	mA
Power supply section					
AC mains voltage range		85		265	V
Mains frequency			50-60		Hz
Output voltage	Green led ON	-10%	12.3	+10%	V
Output voltage ripple	Iout = 500 mA, Vin=85 Vac			1	%
Peak output current				500	mA
Output power				5.6	W
Efficiency at Pout=3.5W			70		%
Nominal transformer isolation*	Primary to secondary/ secondary to auxiliary		4		kV

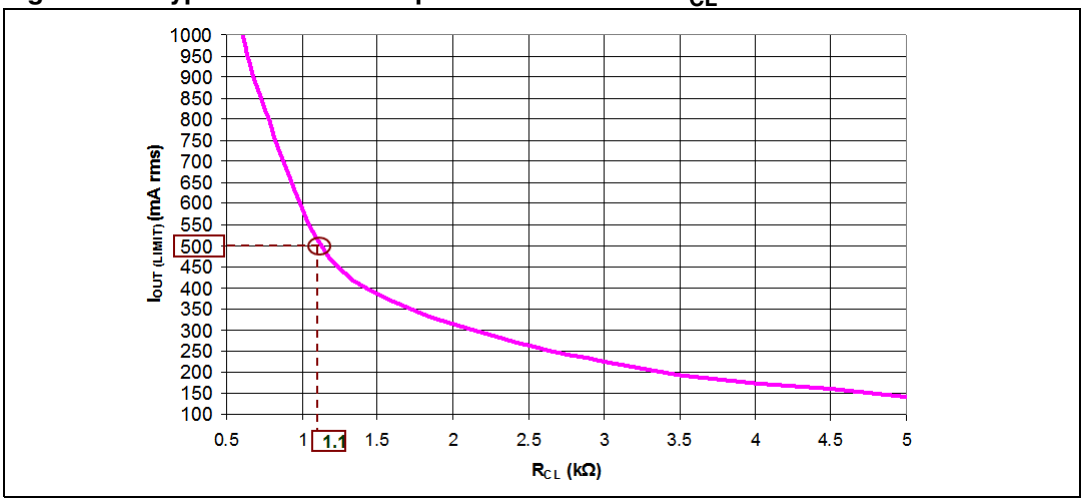
Table 1. Electrical characteristics of the ST7540 reference design (continued)

Parameter	Test conditions	Value			Unit
		Min	Typ	Max	
Number of holdup cycles			0		
Input power		100			mW
Switching frequency	Transceiver section in Tx mode	-10%	65	+10%	kHz
Switching frequency	Transceiver section in Rx mode	-10%	21	+10%	kHz

Table 2. Output voltage level setting through V_{sense} partitioning - typical values

V(PA_OUT) [V_{P-P}]	V(PA_OUT) [V_{RMS}]	V(PA_OUT) [$dBuV_{RMS}$]	R_7 [kΩ]	R_8 [kΩ]
2.830	1.000	120	16	15
3.170	1.120	121	20	15
3.560	1.260	122	24	15
3.990	1.410	123	27	15
4.470	1.580	124	33	15
5.030	1.780	125	39	15
5.660	2.000	126	47	15
6.340	2.240	127	51	15
7.100	2.510	128	56	15
7.980	2.820	129	68	15

Figure 2. Typical curve for output current limit vs. R_{CL} value



2 Safety precautions

The board must be used only by expert technicians. Due to the high voltage (220 V ac) present on the parts which are not isolated, special care should be taken with regard to people's safety.

There is no protection against high voltage accidental human contact.

After disconnection of the board from the mains, none of the live parts should be touched immediately because of the energized capacitors.

It is mandatory to use a mains insulation transformer to perform any tests on the high voltage sections (see circuit sections highlighted in *Figure 7* and *Figure 8*) in which test instruments like Spectrum Analyzers or Oscilloscopes are used.

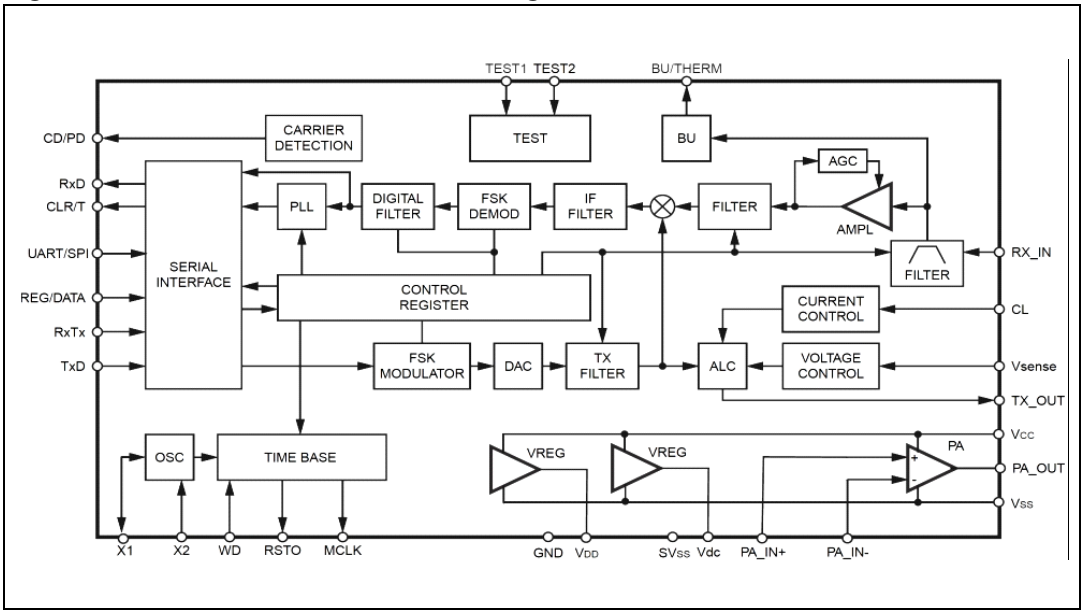
Do not connect any oscilloscope probes to high voltage sections in order to avoid damaging instruments and demonstration tools.

Warning: ST assumes no responsibility for any consequences which may result from the improper use of this tool.

3 ST7540 FSK powerline transceiver description

ST7540 transceiver uses frequency shift keying (FSK) modulation to perform a half-duplex communication on a powerline network. It operates from a 7.5 to 13.5 V single supply voltage (Vcc) and integrates a power amplifier (PA), which is able to drive low line impedance, and two linear regulators providing 5 V and 3.3 V.

Figure 3. ST7540 Transceiver block diagram



The ST7540 can communicate using eight different communication channels (60, 66, 72, 76, 82.05, 86, 110, 132.5 kHz), four baud rates (600, 1200, 2400, 4800) and two deviations (1 and 0.5). Additional functions are included, such as watchdog, automatic control on PA output voltage and current, carrier/preamble detection and band-in-use signaling, transmission time-out, and thermal shutdown.

The transceiver, which is dedicated only to physical communication, operates with a microcontroller whose aim is to manage the communication protocol stack. A reset output (RSTO) and a programmable clock (MCLK) can be provided to the microcontroller by the ST7540 in order to simplify the external logic and circuitry.

The host controller can exchange data with the transceiver through a serial interface, programmable to operate either in UART (CLR/T data clock not used) or in SPI mode. Communication on the power line can be either synchronous or asynchronous to the data clock that is provided by the transceiver at the programmed baud rate.

When in transmission mode (i.e. RxTx line at low level), the ST7540 samples the digital signal on the TxD line at the programmed baud rate and modulates it in a FSK sinusoidal output on the Tx_OUT line. This signal is then externally fed into the power amplifier to add current capability. The power amplifier can also introduce gain and active filtering to the signal, just using few external passive components. The resulting signal on the PA_OUT line is coupled to the power line.

When in receiving mode (i.e. RxTx line at high level), an incoming FSK signal on the Rx_IN line is demodulated and the digital output is available for the microcontroller on the RxD pin.

The device also recovers the synchronism of the received signal using an internal PLL. The recovered clock is present on CLR/T output.

The ST7540 operating parameters can be set by means of an internal control register, accessible only through the SPI host interface.

4 Evaluation tools description

The complete evaluation system for the ST7540 powerline communication consists of:

- a PC using the "ST7540 power line modem demo kit" software tool
- one EVALCOMMBOARD hosting the ST7 microcontroller
- one ST7540 reference design board (EVALST7540-2).

The correct procedure for connecting the EVALST7540-2 and the EVALCOMMBOARD is as follows:

1. Connect the EVALST7540-2 and the EVALCOMMBOARD
2. Connect the ac mains cable to the EVALST7540-2 and the USB cable to the EVALCOMMBOARD
3. Connect the EVALST7540-2 to the ac mains supply
4. Connect the EVALCOMMBOARD to the PC via the USB cable.

Warning: Follow the connection procedure to avoid damaging the boards.

Figure 4. Complete evaluation system including a PC, an EVALCOMMBOARD and the EVALST7540-2 board

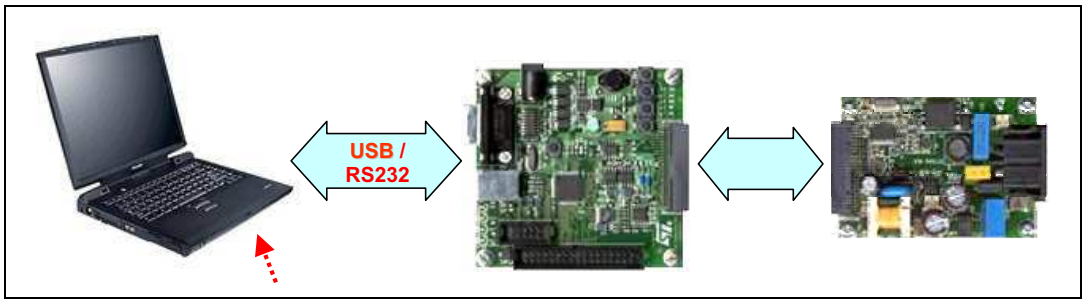
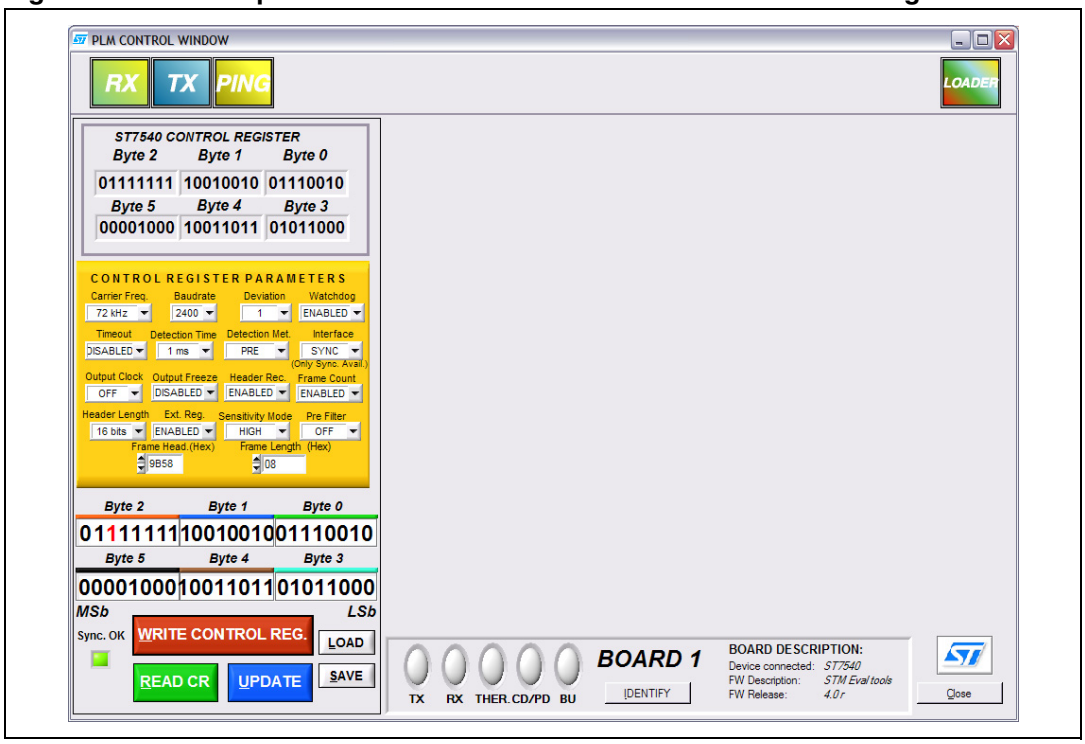


Figure 5. ST7540 powerline modem demonstration kit with control register window



The complete chain, controlled by the ST7540 powerline modem demonstration kit, can set up real communication at bit level, simply by sending or receiving a user-defined bit stream.

It is possible to establish a half-duplex communication with two of these communication nodes (two chains) connected to each other. In order to better evaluate communication between two nodes, the ST7540 powerline modem demonstration kit has some particular features, including:

- Frame synchronization: a byte synchronization header can be added to the to the exchanged data to set up a simple protocol, intended to test the capability of the system to correctly receive the exact transmitted bit sequence. This can be done in two ways: via the ST7540 control register settings (the internal configuration register of the modem has a frame header field, in which an 8- or 16-bit header can be set) or via the Rx panel of the ST7540 powerline modem demonstration kit (setting a synchronization at SW level). A bit synchronization can be introduced as a simpler feature by enabling the preamble detection method in the control register panel and then inserting at least one “0101” or one “1010” sequence at the beginning of the transmitted bit stream.
- Ping session: a master-slave communication with automatic statistics calculation can be very useful to test a point-to-point or a point-to-multipoint powerline communication network, thus providing a method to evaluate reachability of each node in the network. For further details about the ST7540 powerline modem demonstration kit, please refer to the user manual UM0239 “ST7540 power line modem demo kit graphical user interface”.

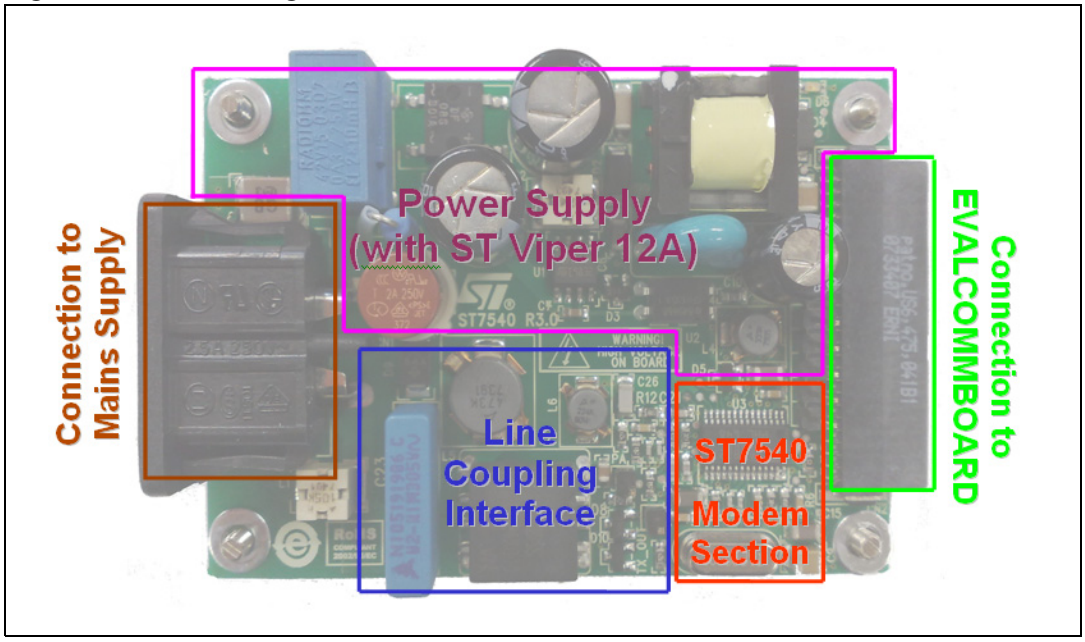
5 Board description

The ST7540 reference design is composed of the following sections:

- Power supply section, based on ST's VIPer12A-E IC
- ST7540 modem and crystal oscillator section
- Line coupling interface section, with three subsections:
  - Transmission active filter
  - Transmission passive filter
  - Receiving passive filter.

The board also has two connectors, which allow the user to plug the mains supply on one side of it and the I.B.U. communication board on the other side.

Figure 6. Positioning of the various sections of the board



The schematics of the whole reference design appear in *Figure 7* and *8*. *Figure 7* shows the modem and the coupling Interface circuits, while *Figure 8* represents the power supply circuit. In both the schematics, high voltage regions are highlighted.

Table 3 lists the components used to develop the reference design board. All parts have been selected to give optimal performances.

The layout of the printed circuit is given in *Appendix A* - *Figure 49*, *Figure 50* and *Figure 51*.

Figure 7. Modem and coupling interface schematic

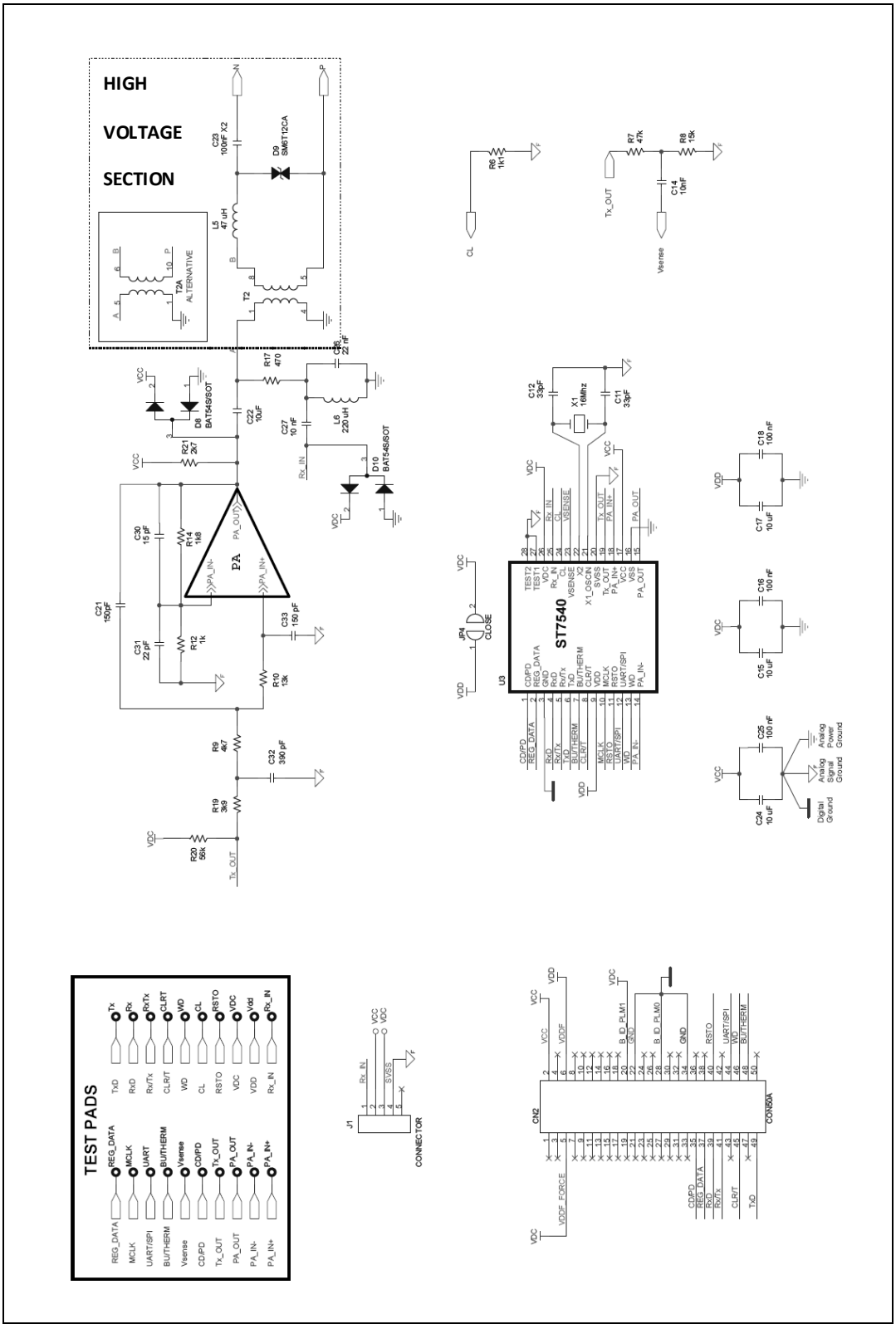


Figure 8. Power supply schematic

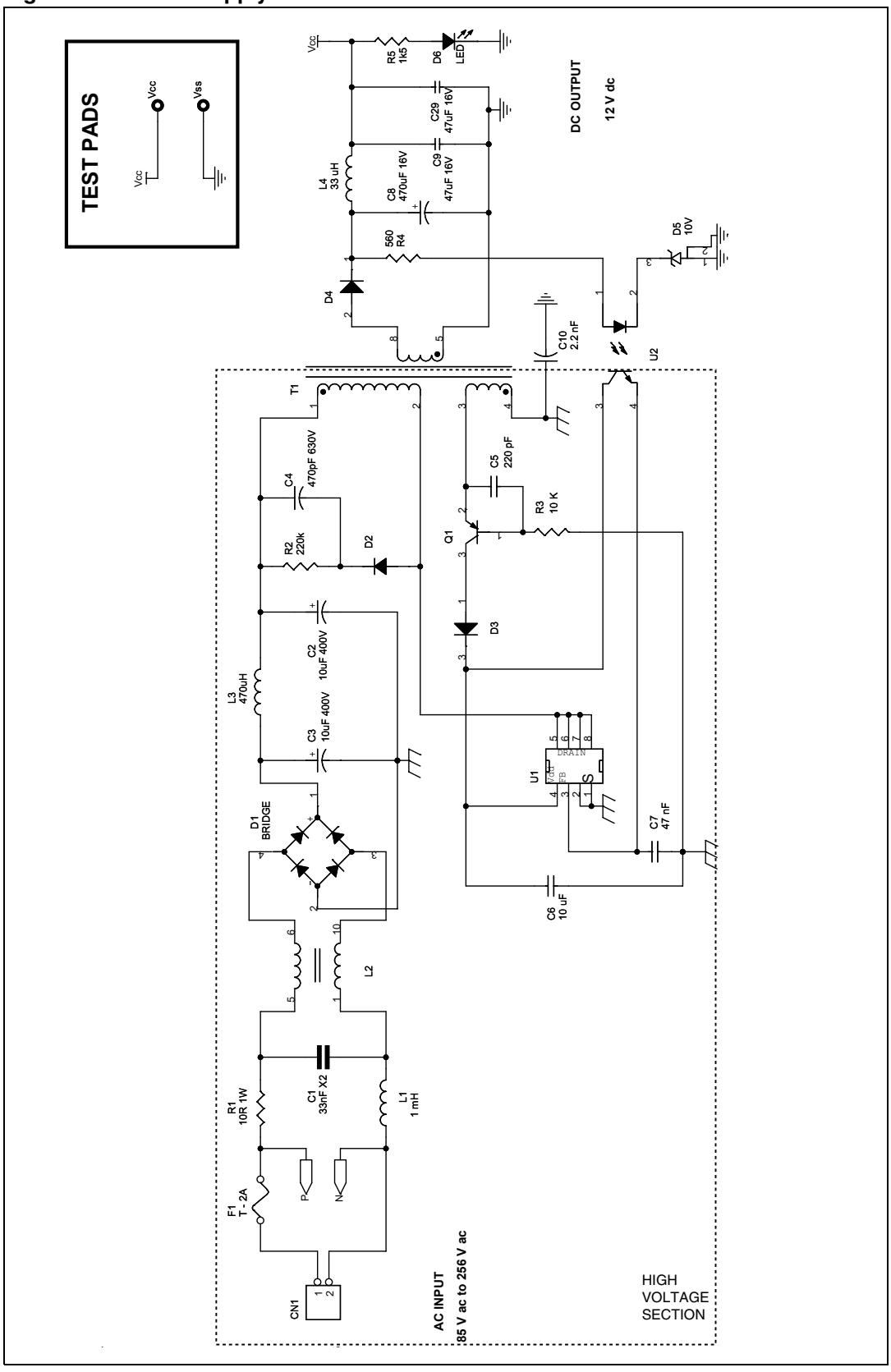


Table 3. Bill of materials

Item	Qty	Part	Value	Description
1	1	CN1	HEADER 2	Mains supply connector
2	1	CN2	CON50A	50 pins SMT right angle female p=1.27mm
3	1	C1	33nF X2	Murata GA355XR7-GB333K
4	2	C2,C3	10uF / 400V	Yageo SE-K / Nichicon VK 20%
5	1	C4	470pF / 1kV	TDK C4520X7R-3A471K
6	1	C5	220pF / 50V	TDK C0603C0G-1E220J
7	4	C6,C15,C17,C24	10uF / 16V	TDK C3216X7R-1C106MT
8	1	C7	47nF / 25V	Murata GRM188R7-1E473K
9	1	C8	470uF / 16V	Rubycon 3M0319 / Yageo SE-K 20%
10	2	C9,C29	47uF / 16V	Murata GRM32ER6-1C476K
11	1	C10	2.2nF Y1	TDK CD12-E2GA222MYNS / Murata DE1E3-KX222M
12	2	C11,C12	33pF	TDK C1005C0G-1H330J
13	2	C14,C27	10nF	Murata GRM188R7-1H103K
14	4	C16,C18,C19,C25	100nF	TDK C1608X7R-1H104K
15	2	C21,C33	150pF	Murata GRM1885C-1H151J
16	1	C22	10uF	Murata GRM21BR6-1A106K / TDK C2012X5R-0J106K
17	1	C23	100nF X2	EPCOS B32922-A2104K
18	1	C26	22nF	Murata GRM21B5C-1H223J / TDK C3216C0G1H223J
19	1	C30	15pF	Murata GRM1555C-1H150J
20	1	C31	22pF	Murata GRM1555C-1H220J
21	1	C32	390pF	Murata GRM1885C-1H391J
22	1	D1	DF06S	600 V - 1.5 A bridge rectifier
23	1	D2	STTH1L06A	SMA ultra-fast Schottky diode
24	1	D3	BAS16 / BAS21	SOT23
25	1	D4	STPS1H100	SMA Schottky diode
26	1	D5	BZX84C10	SOT23 10V zener diode
27	1	D6	LED	Green LED
28	2	D8, D10	BAT54S	SOT23 low drop Schottky diode
29	1	D9	SM6T12CA	12V bidirectional transil diode
30	1	F1	2A - T	Time-lag fuse
31	1	JP4	CLOSE	
32	1	J1	CONNECTOR	

Table 3. Bill of materials (continued)

Item	Qty	Part	Value	Description
33	1	L1	1mH	Epcos B82442-H1105K
34	1	L2	2x10mH 0.3A	Radiohm 42V15
35	1	L3	470uH	Epcos B82442-A1474K
36	1	L4	33uH	Epcos B82462-A4333K
37	1	L5	47uH	Epcos B82464-A4473K / WE 744-775-147
38	1	L6	220uH	Epcos B82462-A4224K / WE 744-774-222
39	1	Q1	BC857BL	SOT23
40	1	R1	10R 1W	Metal oxide type - radial
41	1	R2	220K	0603 1%
42	1	R3	10K	0603 1%
43	1	R4	560	0603 1%
44	1	R5	1K5	0603 1%
45	1	R6	1K1	0603 1%
46	1	R7	47K	0603 1%
47	1	R8	15K	0603 1%
48	1	R9	4K7	0603 1%
49	1	R10	12K	0603 1%
50	1	R12	1K	0603 1%
51	1	R14	1K8	0603 1%
52	1	R17	470	0603 1%
53	1	R19	3K9	0603 1%
54	1	R20	56K	0603 1%
55	1	R21	2K7	0603 1%
56	1	T1	SMPS transformer	TDK SRW12.6EF-E07H013 / WE S06-100-057
57	1	T2	Line transformer	VAC T60403-K5024-X044 / Radiohm 69H14-2101
58	1	U1	VIPER12AS	SMPS controller / switch
59	1	U2	SFH610-A	Opto-switch
60	1	U3	ST7540	Powerline transceiver
61	1	X1	16 MHz	

Table 4. ST parts on the ST7540 reference design board

Value	Description
ST7540	Powerline transceiver
VIPER12AS	SMPS controller / switch
STTH1L06A	Ultrafast diode
STPS1H100	Schottky diode
SM6T12CA	12V bidirectional transil diode

5.1 Coupling interface

The mains coupling interface is composed of three different filters: the Tx active filter, the Tx passive filter and the Rx passive filter.

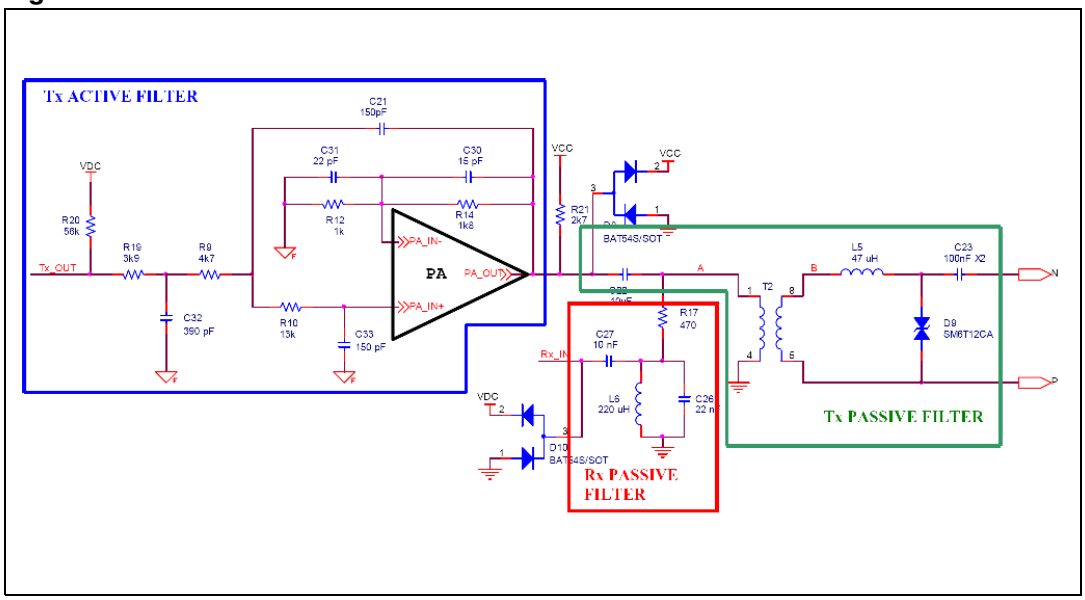
All three filters are described in the sections *Section 5.1.1*, *5.1.2*, and *5.1.3*. In each section, calculations and measured frequency responses are given.

The filters are quite sensitive to the components' value tolerance. Actual components used in the ST7540 reference design have the following tolerances:

- +/- 10% for coils and for the X2 capacitor
- +/- 1% for SMD resistors
- +/- 5% for SMD ceramic capacitors.

To evaluate sensitivity of the filters to the tolerances listed above, the following sections include simulated responses of the filters with Montecarlo statistical analysis. Statistical simulation helps understanding the relationship between components' value tolerance and variations on the responses of the filters. In simulation curves, the ideal response is drawn in blue, while red curves indicate statistical variations generated through simulation.

Figure 9. Schematic of Rx and Tx filters



5.1.1 Tx active filter

The Tx active filter is based on the ST7540 internal power amplifier (PA), whose input and output pins are available externally to allow a filtering network to be tailored around the amplifier.

For the ST7540 reference design board, a 3-pole low-pass filter has been developed by cascading a simple R-C low-pass stage and a Sallen-Key 2-pole cell with 9dB gain. The R19-C32 low-pass stage is aimed at introducing attenuation starting from approximately an octave above the transmission channel frequency.

The transfer function of the 2nd order Sallen-Key cell is:

Equation 1

$$A(s) = \frac{A_0}{\frac{s^2}{\omega_C^2} + \frac{s}{\omega_C \bullet Q} + 1}$$

where $A_0 = \left(1 + \frac{R_{14}}{R_{12}}\right)$, $\omega_C = \frac{1}{\sqrt{R_9 \bullet R_{10} \bullet C_{33} \bullet C_{21}}}$ and $Q = \frac{\sqrt{R_9 \bullet R_{10} \bullet C_{33} \bullet C_{21}}}{R_9 C_{33} + R_{10} C_{21} + R_9 C_{21}(1 - A_0)}$

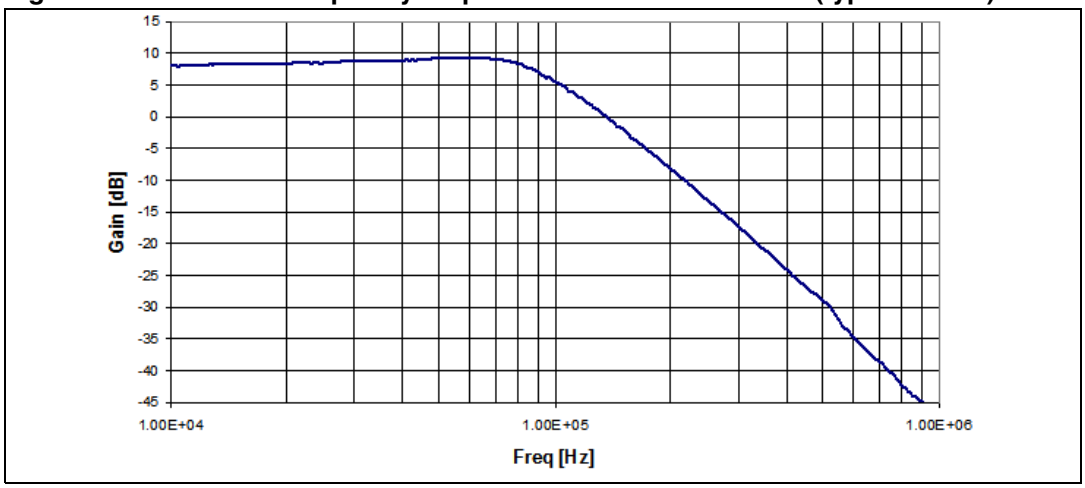
The corner frequency may be calculated as:

Equation 2

$$f_c = \frac{1}{2\pi \bullet \sqrt{R_9 \bullet R_{10} \bullet C_{33} \bullet C_{21}}} = 135.7\text{kHz}$$

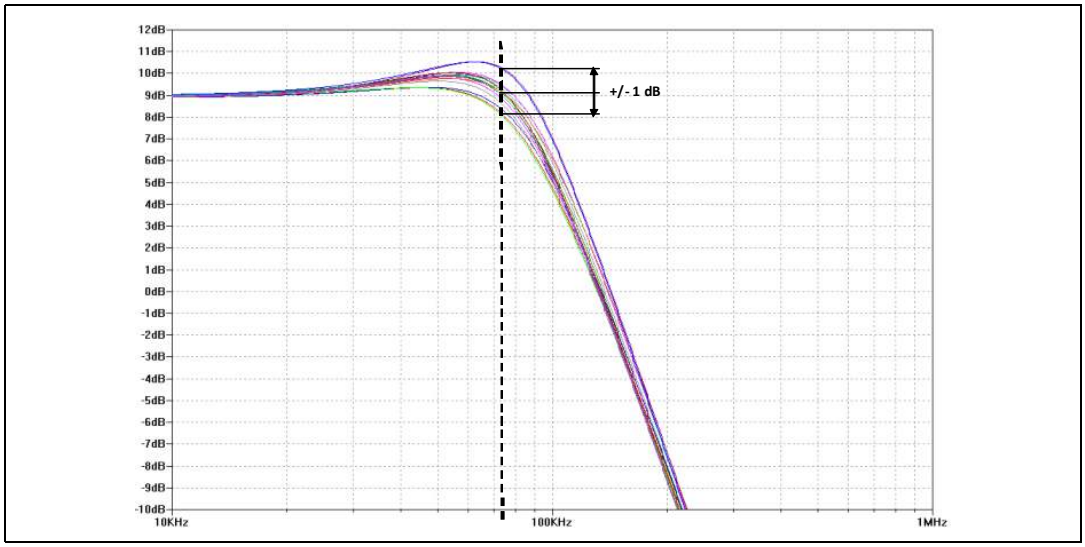
Figure 10 represents the measured transfer function of the Tx active filter. It shows good rejection on both the 2nd and 3rd harmonic frequencies for the 72 kHz signal.

Figure 10. Measured frequency response of the Tx active filter (typical curve)



Simulation of the Tx active filter response against components' tolerance, depicted in *Figure 11*, shows +/- 1 dB variation in gain module at 72 kHz.

Figure 11. Simulated frequency response of the Tx active filter with components tolerance effect



5.1.2 Tx passive filter

Coupling to the power line requires some passive components in addition to the active filtering stage. In particular, Tx passive filter section is made of the decoupling capacitor C22, line transformer T2, inductor L5 and X2 safety capacitor C23.

L5 has been accurately chosen to have a high saturation current (>1 A) and a very low equivalent series resistance (<0.2 Ω), to limit distortion and insertion losses even with heavy line load. Center frequency for the series resonance is calculated as:

Equation 3

$$f_c = \frac{1}{2\pi\sqrt{L_5 \bullet C_{23}}}$$

provided that the dc-decoupling capacitor C22 is much greater than C23 (in this case, 100 times greater) and that parasitic components of the transformer have negligible effects on the filtering action.

Particular attention has been paid in choosing the line transformer. The required characteristics are listed in *Table 5*.

In order to have a good power transfer and to minimize the insertion losses, it is recommended to choose a transformer with a primary (shunt) inductance greater than 1mH and a series resistance lower than 0.5 Ω.

Another important parameter is the leakage inductance. If it has a relevant value (10 to 50 uH), this can be used to design the coupling filter without inserting series inductance (L5, L6). The drawback, however, is the poor accuracy of this parameter, which can lead to a shift of the filter response and to bad coupling. Consequently, a low leakage inductance value (<1 µH) has been chosen, fixing the series inductance through a discrete component with greater accuracy.

The last specified parameter, the 4 kV insulation voltage requirement, is described and coded in the EN50065-4-2 CENELEC document.

Table 5. Line coupling transformer specifications

Parameter	Value
Turn ratio	1:1
Magnetizing inductance	>1 mH
Leakage inductance	<1 µH
DC resistance	<0.5 Ω
DC saturation current	>2 mA
Interwinding capacitance	< 50 pF
Withstanding voltage	4 kV

Figure 12 shows the measured response of the Tx active and passive filters, loaded with the CISPR network. The figure highlights a further filtering effect added by the passive L-C series resonant combined with the CISPR reactive load.

Figure 12. Measured frequency response of the Tx active + passive filters connected to the CISPR network (typical curve)

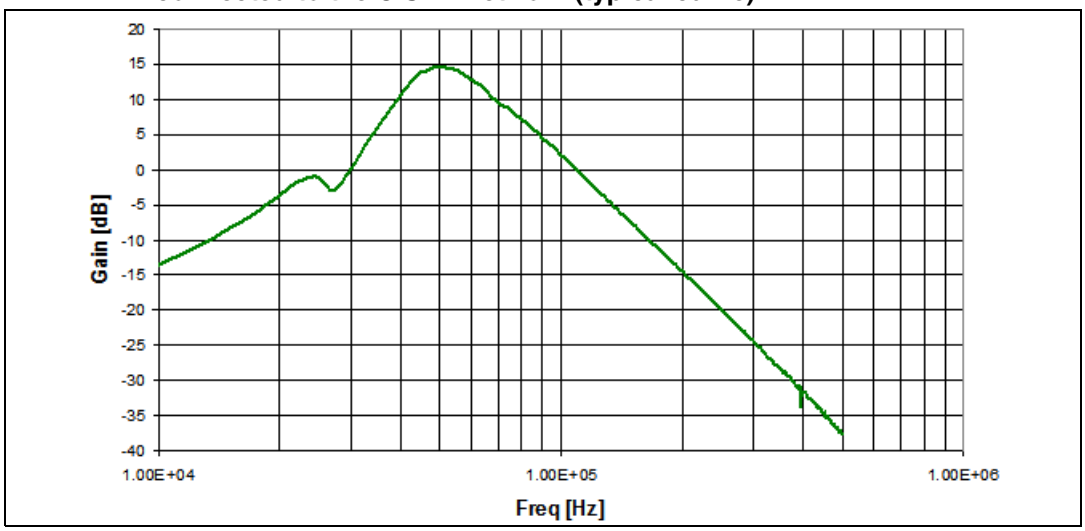
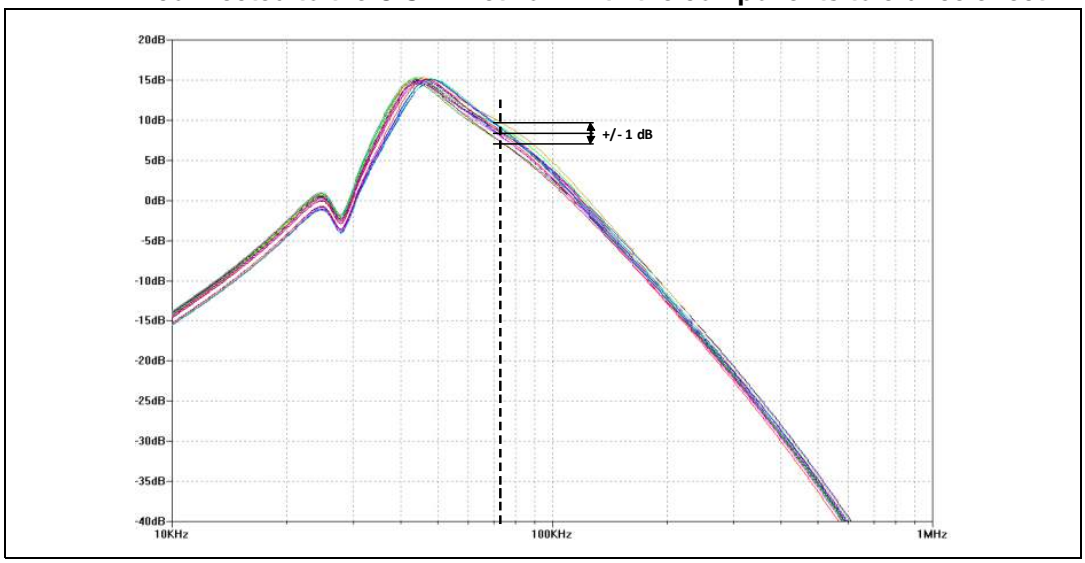


Figure 13. Simulated frequency response of the Tx active + passive filters connected to the CISPR network with the components tolerance effect



5.1.3 Rx passive filter

The Rx filter is made up of a resistor in series with a parallel L-C resonant. The transfer function of the filter can be written as:

Equation 4

$$R(s) = \frac{\frac{s \bullet L_6 + R_L}{R_{17} L_6 C_{26}}}{s^2 + \frac{R_{17} R_L C_{26} + L_6}{R_{17} L_6 C_{26}} \bullet s + \frac{R_{17} + R_L}{R_{17} L_6 C_{26}}}$$

where R_L is the DC series resistance of the inductor (in our case, about 2 Ω). The center frequency and the quality factor of the filter can be expressed as:

Equation 5

$$fc = \frac{1}{2\pi} \bullet \omega_C = \frac{1}{2\pi}\sqrt{\frac{R_{17}+R_L}{R_{17}L_6C_{26}}} \cong \frac{1}{2\pi\sqrt{L_6C_{26}}}, Q = \frac{R_{17}L_6C_{26}}{R_{17}R_LC_{26}+L_6} \bullet \omega_C$$

The simplification made on *fc* formula is possible because $R_{17}>R_L$. Consequently, the quality factor and filter selectivity depend not only on R_{17}, but also on R_L. A higher R_L produces a lower steepness of the resonance, while a higher R_{17} gives a higher selectivity. Actual values of the components give a Q equal to 4.3.

The R_L value impacts in a clearer way on insertion losses. To evaluate the relationship between R_L and the losses on the received signal, the following simplified expression of $|R(s)|$ at $f=f_c$ may be used:

Equation 6

$$\left|R(j \bullet 2\pi f_c)\right| \cong Q \bullet \frac{\omega_C \bullet L_6}{R_{17}} = \frac{1}{1 + R_L \bullet R_{17} \bullet \frac{C_{26}}{L_6}}$$

With actual values of the components, we get a loss of about 1 dB. The same calculation gives unitary transfer if R_L is set to zero.

Looking at the first way to express the module of the transfer function, it is possible to notice that a higher value of Q can help keeping the losses small. Nevertheless, a high value of Q would bring a higher sensitivity of the filter to the components tolerance.

Figure 14 shows the measured frequency response of the Rx passive filter. The filter has an actual -3 dB bandwidth equal to 17 kHz and an attenuation of about 1 dB at center frequency, just as expected.

Figure 14. Measured frequency response of the Rx passive filter (typical curve)

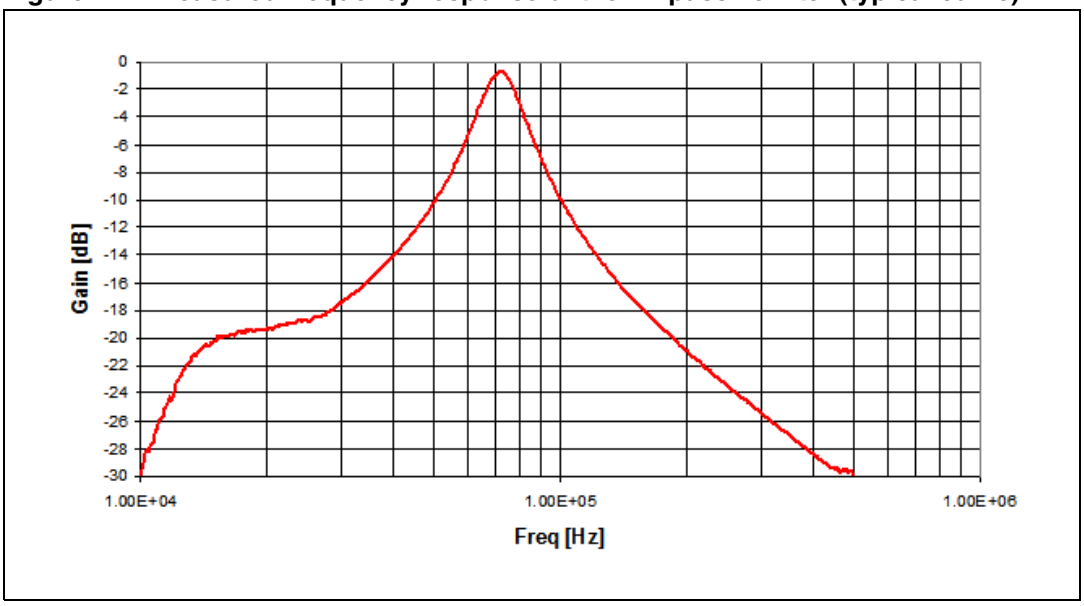
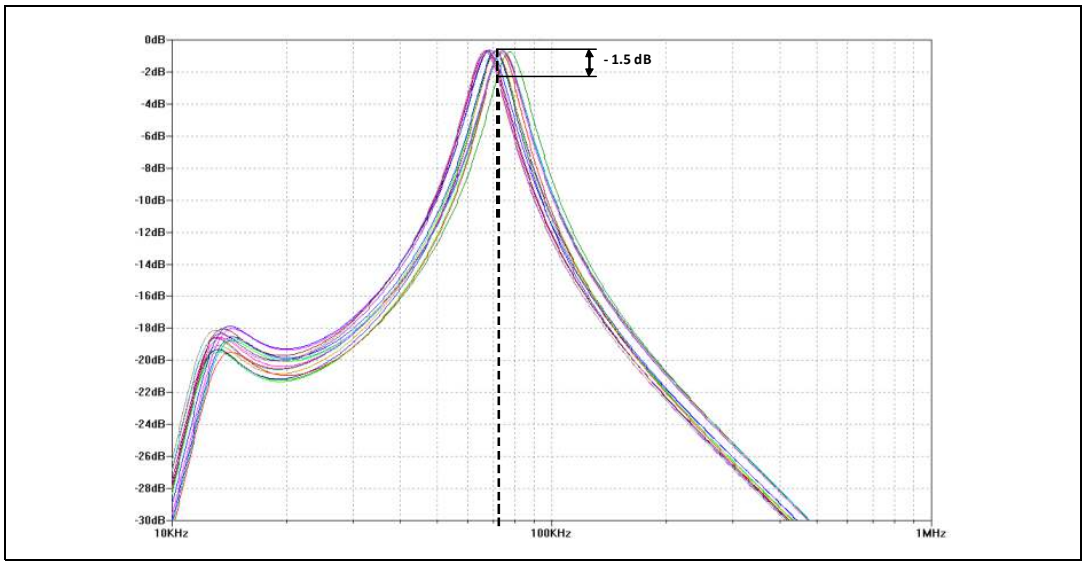


Figure 15 represents a simulation of the response of the Rx passive filter with the components tolerance effect. A worst case loss of nearly 1.5 dB can be observed at 72 kHz due to a shift on center frequency.

Figure 15. Simulated frequency response of the Rx passive filter with components tolerance effect



5.1.4 Input impedance

The input impedance of a powerline communication node is another critical point. *Figure 16* and *Figure 17* show the input impedance magnitude vs. frequency curves in both Tx and Rx mode. In both figures channel impedance point and the minimum impedance point are indicated.

The impedance magnitude values prove that the ST7540 reference design board is compliant with the EN50065-7 document, which sets the following minimum impedance constraints for this kind of equipment:

- Tx mode:
  - free in the range 3 to 95 kHz
  - 3 Ω from 95 to 148.5 kHz
- Rx mode:
  - 10 Ω from 3 to 9 kHz
  - 50 Ω between 9 and 95 kHz only inside signal bandwidth (free for frequencies outside signal bandwidth)
  - 5 Ω from 95 to 148.5 kHz

Figure 16. Measured input impedance magnitude of coupling interface in Tx mode (typical curve)

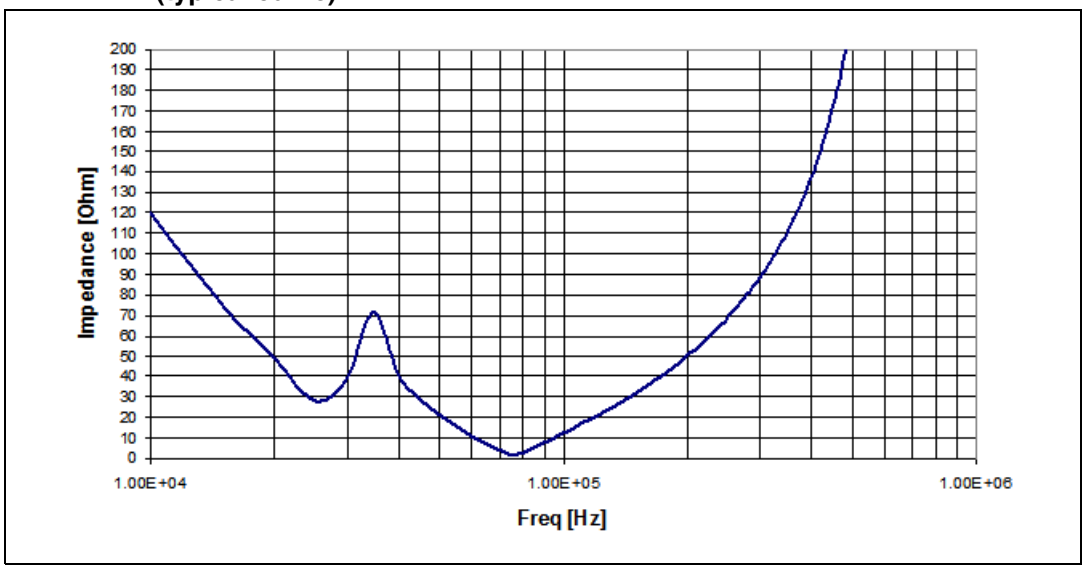
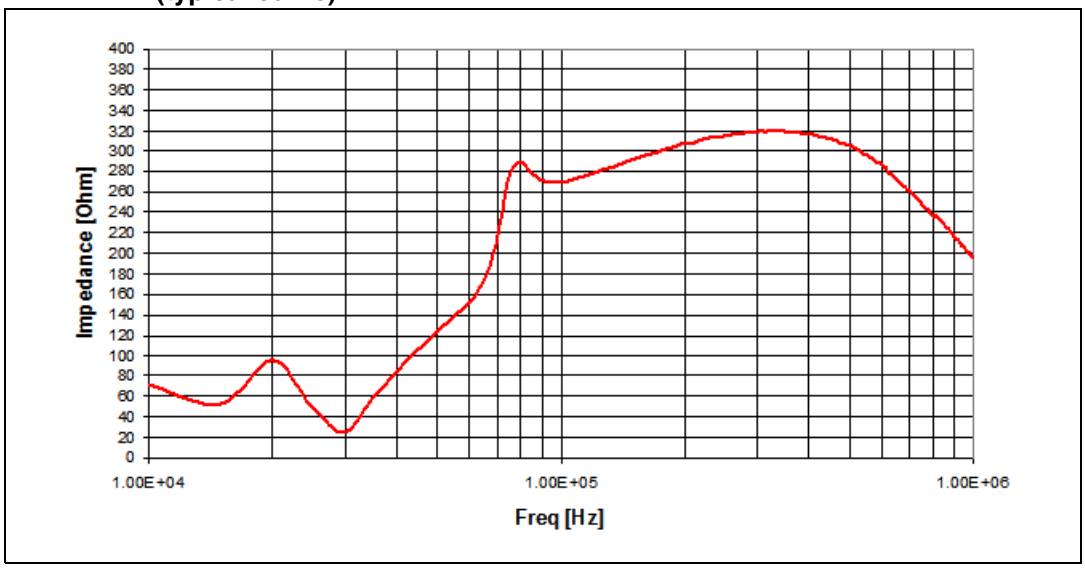


Figure 17. Measured input impedance magnitude of coupling interface in Rx mode (typical curve)



5.2 Conducted disturbances

5.2.1 Conducted emissions

The EN50065-1 standard describes the test setup and procedures for testing conducted emissions.

The conducted emissions measurements have been taken with 220 V_{ac} mains voltage. The test pattern consists of a continuous transmission of a “1010” continuous sequence at 2400 baud, deviation 1. The output signal measured at the CISPR artificial network has a value of 120 $dBuV_{RMS}$ which means a signal of 2 V_{RMS} on the mains output.

The spectrum analyzer performs a peak measurement instead of a quasi-peak measurement, as specified by EN50065-1. For continuous sinusoidal signals the two types of measurement give the same result.

Figure 18. Conducted emissions test setup

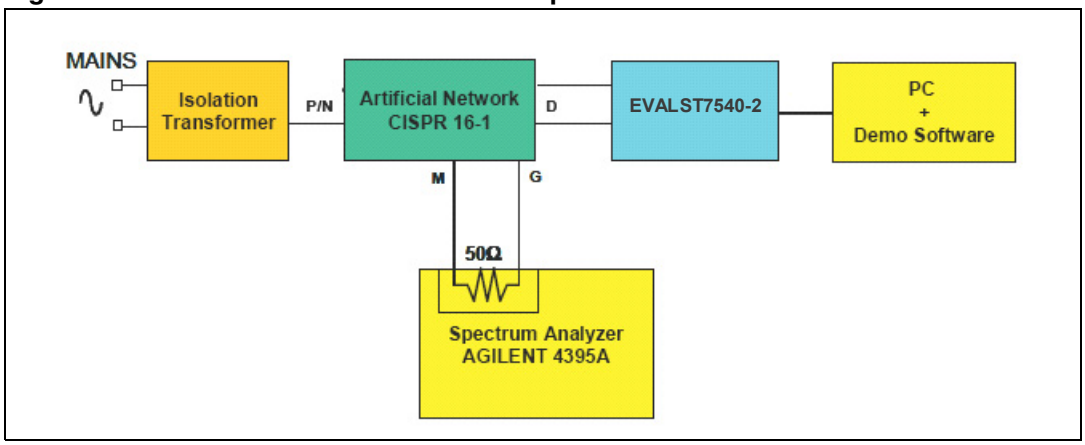
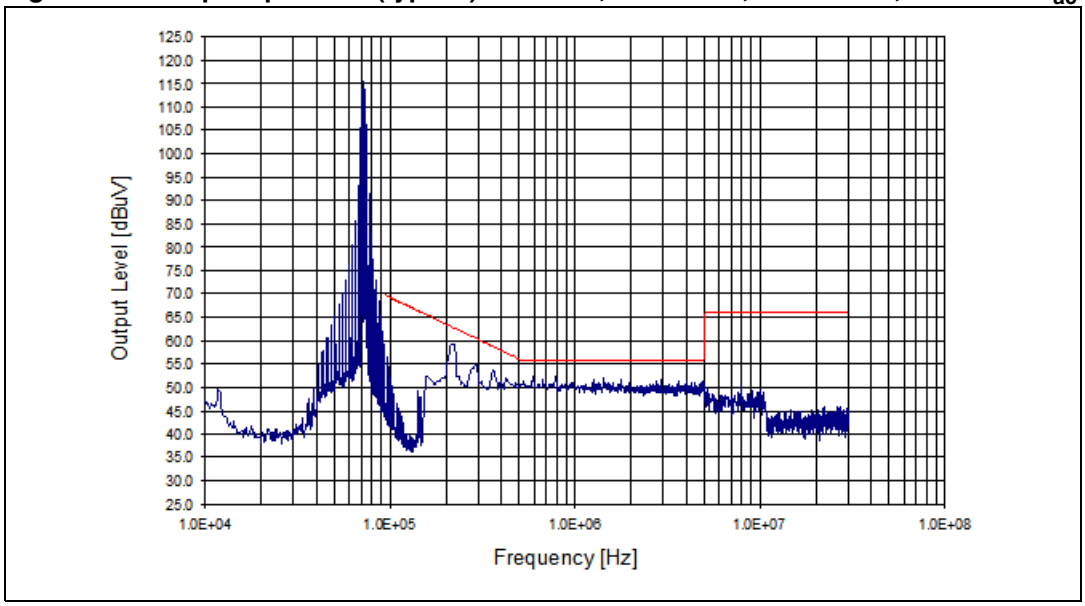


Figure 19 shows the results for the output spectrum measurement. The EN50065-1 disturbance limits mask (traced in red) may be compared to the typical output spectrum of the ST7540 reference design board.

Figure 19. Output spectrum (typical) at 72 kHz, 2400 baud, deviation 1, mains 220V_{ac}



5.2.2 Noise immunity

The tests on immunity against white noise and narrow-band conducted interferences are based on two ST7540 reference design boards performing a simplex (unidirectional) communication. The first board transmits a given bit sequence, while the receiving board passes the received bit stream to a BER tester software on a PC, which evaluates the percentage of correctly received bits.

The noise (white noise or sinusoidal interferer) is produced by a waveform generator and injected into the artificial network through an AC coupling circuit. *Figure 20* shows the test environment used to perform noise immunity tests.

Figure 20. Narrow-band conducted interference test setup

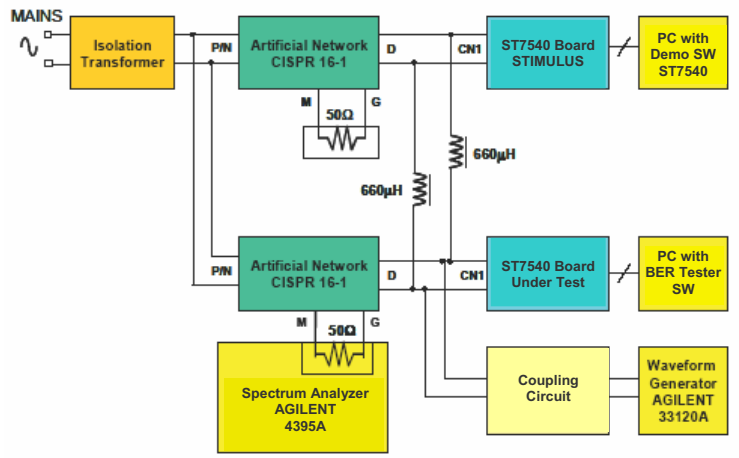


Table 6 reports the parameters for the test conditions settings.

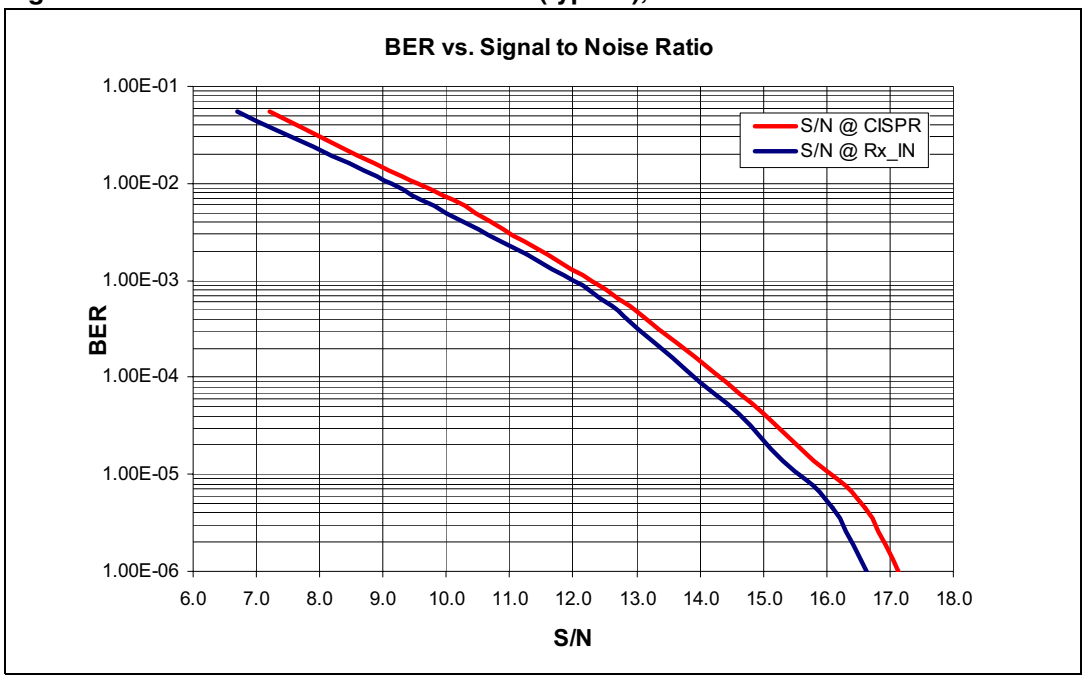
The received signal and noise levels are measured at the mains connector of the board under test. The 3 kHz resolution bandwidth chosen for the Spectrum Analyzer allows measurement of the actual signal and noise levels as seen by the receiving ST7540 internal circuitry, programmed for 2400 baud.

Table 6. Noise immunity test settings

Parameter	Value
Received signal	86 dBuVrms
Frequency	72 kHz
Baud rate	2400
Deviation	1
Detection method	Carrier with conditioning
Detection time	3 ms
Sensitivity	High
Input filter	Off
Transmitted sequence	AACC h
S.A. resolution BW	3 kHz

Figure 21 represents the BER vs. SNR curve in the presence of white noise. It may be noted that a BER of 10^{-3} corresponds to a SNR around 12 dB, as expected from a nonideal FSK demodulator.

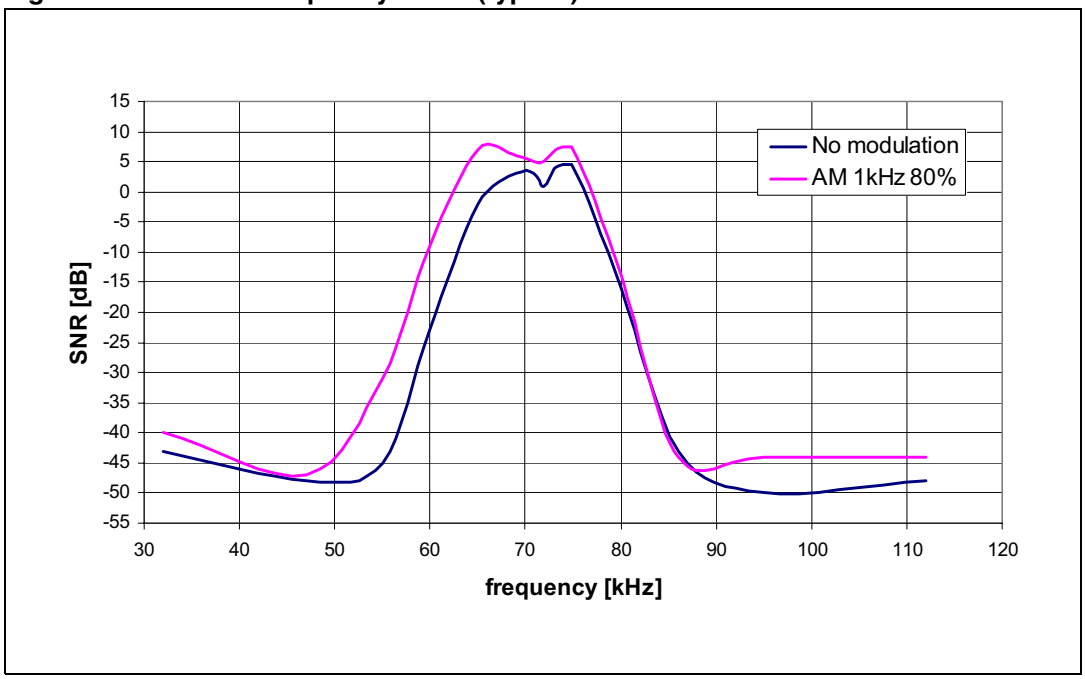
Figure 21. Measured BER vs. SNR curve (typical), white noise



For narrow-band interference tests, two types of interfering noise have been used: a pure sinusoidal tone and an amplitude-modulated signal (modulating signal 1 kHz, modulation depth 80%). In both cases, the amplitude of the noise signal (of the carrier, for modulated signal) has been decreased until the measured BER was lower than 10^{-3} (one error every 1000 transmitted bits).

Figure 22 shows SNR vs. frequency curves for both a pure sinusoidal and an AM modulated interferer.

Figure 22. SNR vs. frequency curve (typical) at BER = 10^{-3}



5.3 Thermal design

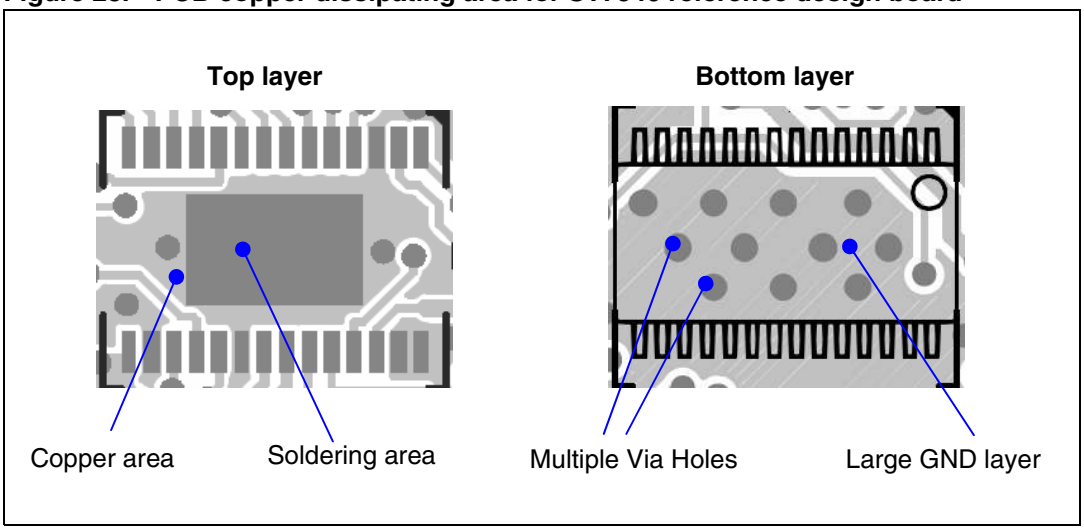
All heat dissipation is based on the heat exchange between the ST7540 IC, the PCB and the surrounding environment.

A large PCB copper area under the device is recommended to make an easier heat transfer from the ST7540 to the environment. The metallic slug under the device (exposed pad of HTSSOP28 package) must be properly soldered to the copper area on the PCB top side, as recommended in the datasheet.

The large ground layer on the bottom side of the board must be connected to the top side layer through multiple via holes.

In the case of ST7540 reference design, an area of about 0.2 cm^2 is put on the PCB top side for exposed pad soldering, while ground layer dissipating area on the bottom side is nearly 1.5 cm^2.

Figure 23. PCB copper dissipating area for ST7540 reference design board



Even if the ST7540 features a built-in thermal shutdown circuitry which turns off the power amplifier (PA) when the die temperature (T_J) exceeds 170 °C. It is however recommended not to exceed 125 °C during normal operating conditions to ensure the functionality of the IC.

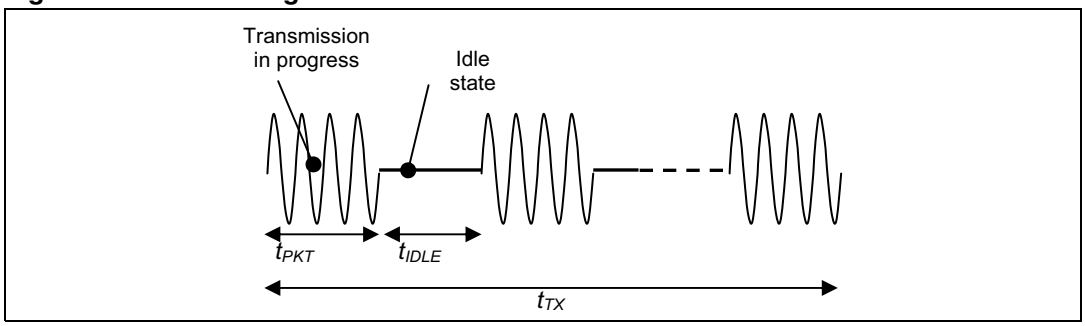
The relationship between junction temperature T_J and power dissipation during transmission P_D is described by the following formula:

Equation 7

$$T_J(t_{TX}, d) = T_A - P_D \bullet \theta_{JA}(t_{TX}, d)$$

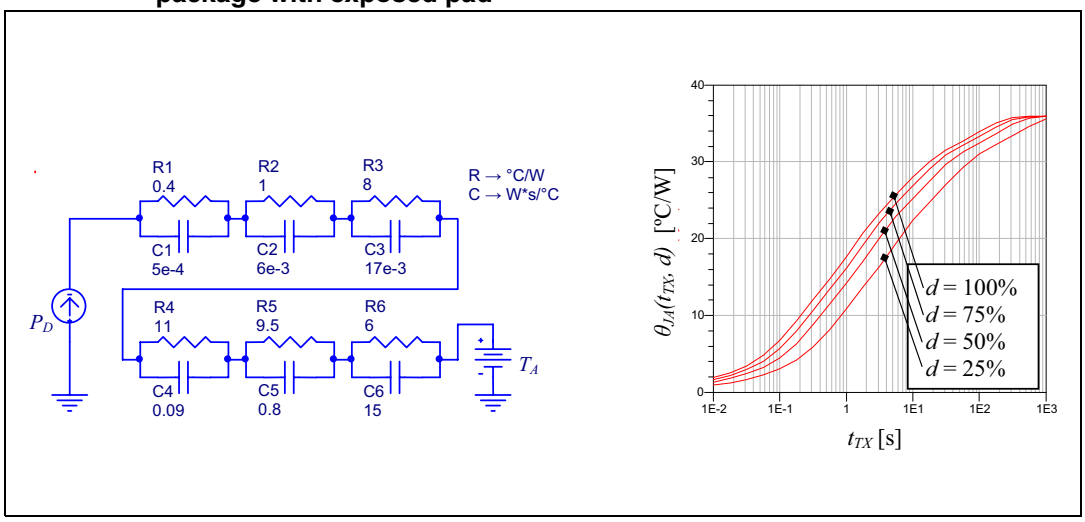
where T_A is the ambient temperature (from -45 to +85 °C) and θ_{JA} is the junction to ambient thermal impedance of the ST7540 IC, which is related to the length of the transmission (t_{TX}) and to the duty cycle $d = t_{PKT} / (t_{PKT} + t_{IDLE})$, assuming a packet-fragmented transmission as illustrated by *Figure 24*.

Figure 24. Packet-fragmented transmission



When soldered to a proper copper area on the PCB as explained above, the IC is characterized by a steady-state thermal impedance of about 35 °C/W. The transient of the thermal impedance θ_{JA} can be estimated by simulating a 6-cell equivalent model, as shown in *Figure 25*. The simulated curve vs. the transmission duration and the duty cycle is also given. It can be noticed that the transient of θ_{JA} takes several hundreds of seconds, after which the static value of 35 °C/W is reached.

Figure 25. Equivalent model of the thermal impedance θ_{JA} of the HTSSOP28 package with exposed pad



This means that during the transient phase (i.e. if the transmission time t_{TX} is some seconds or even less) the IC is able to dissipate power that is well above the one sustainable at steady state. For this reason, a complete thermal analysis requires taking into account the characteristics of the transmission, i.e. duty cycle and duration, determining the value reached by the thermal impedance and then the allowed power dissipation.

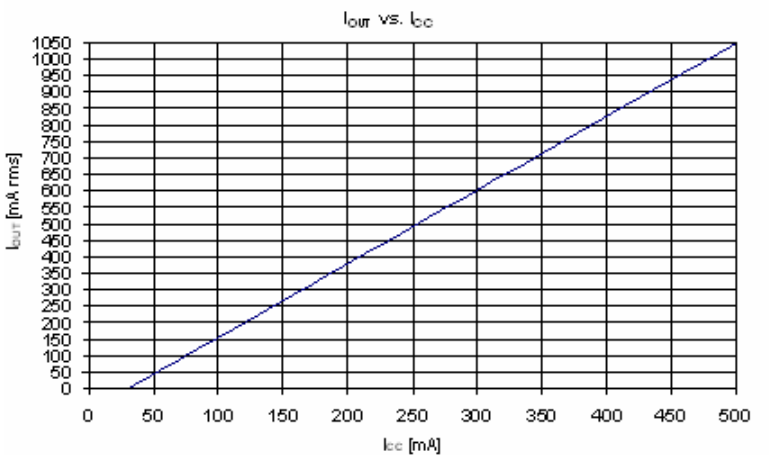
Actual dissipated power P_D can be calculated as:

Equation 8

$$P_D = P_{IN} - P_{OUT}$$

where $P_{IN}=V_{CC}*I_{CC}$ and $POUT=V_{OUT\ rms} * I_{OUT\ rms}$. Note that power consumption by receiving circuitry and linear regulators is considered negligible for thermal analysis purposes. The relationship between current absorption from the power supply (I_{CC}) and PA output current to the load (I_{OUT}) is shown in *Figure 26*. The value of V_{in} can be deduced from the load regulation curve of the SMPS, given in *Figure 37*.

Figure 26. Output current vs. supply current typical curve for ST7540 in Tx mode



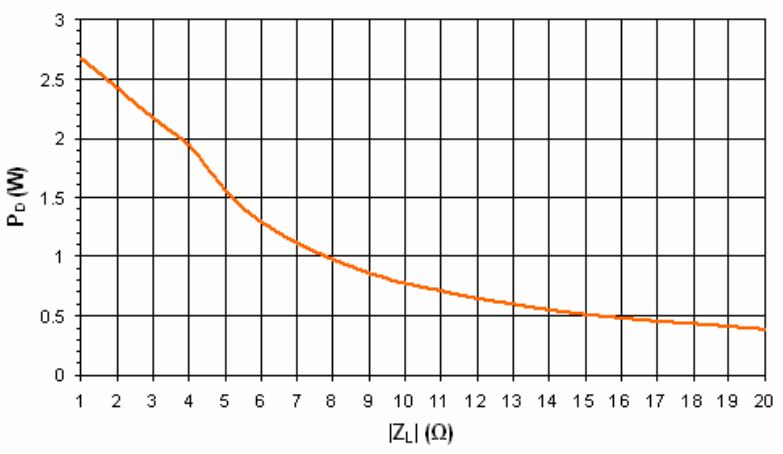
The transmission output level $V_{OUT\ rms}$ of 2 V and the current limit $I_{OUT\ rms(LIMIT)}$ of 500 mA, fixed for the ST7540 reference design, correspond to a maximum output power P_{OUT} of 1 W over a 4 Ω load. In these conditions, the required dissipation results equal:

Equation 9

$$P_{D(LIMIT)} = P_{IN(LIMIT)} - P_{OUT(LIMIT)} \cong (11.7V \bullet 0.25A) - (2V \bullet 0.5A) \cong 2W$$

Figure 27 shows the curve of P_D vs. the load impedance modulus according to the $V_{OUT\ rms}$ and $I_{OUT\ rms(LIMIT)}$ set for the ST7540 reference design.

Figure 27. Dissipated power vs. load impedance modulus typical curve for ST7540 reference design board



Referring to the relationship between dissipated power and temperature, it can be proven that in a continuous transmission, i.e. with θ_{JA} at its steady-state value of 35 °C/W, a 2 W dissipation can be sustained in safe conditions if the ambient temperature remains below 55 °C. Instead, supposing a transmission time t_{TX} of 1 s and a duty cycle d of 50%, according to the graph of *Figure 25* the θ_{JA} would be 15 °C/W only. In this case a power dissipation of 2.7 W (corresponding to a 1 Ω load) is allowed over the entire ambient temperature range of the ST7540.

5.4 Oscillator section

The ST7540 crystal oscillator circuitry is based on a MOS amplifier working in inverter configuration.

This circuitry requires a crystal with a maximum load capacitance of 16 pF and a maximum ESR of 40 Ω.

It is very important to keep the crystal oscillator and the load capacitors as close as possible to the device.

The resonant circuit should be far away from noise sources such as:

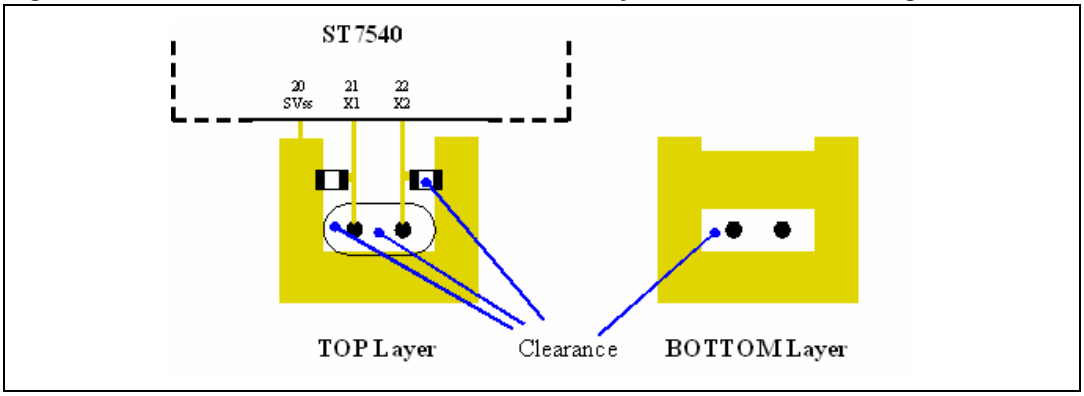
- Power supply circuitry
- Burst and surge protections
- Mains coupling circuits
- Any PCB track or via carrying a signal.

To properly shield and separate the oscillator section from the rest of the board, it is recommended to use a ground plane on both sides of the PCB, filling all the area below the crystal oscillator and its load capacitors. No tracks or vias should cross the ground plane except for the crystal connections.

It is also recommended to use a large clearance on the oscillator related tracks, to minimize humidity problems (see *Figure 28*).

Connecting the case to ground is also a good practice to reduce the effect of radiated signals on the oscillator.

Figure 28. A recommended oscillator section layout for noise shielding



5.5 Surge and burst protection

The specific structure of the coupling interface circuit of the application is a weak point against high voltage disturbances that can come from the external environment. In fact an efficient coupling circuit with low insertion losses consequently allows a very low impedance path from the mains to the powerline interface of the device.

For this reason it is recommended to add some specific protection devices on the mains coupling path, to prevent high energy disturbances coming from the mains from damaging the internal circuitry of the ST7540.

The possible environments for this kind of application can be both indoor and outdoor: residential, commercial and light-industrial locations. To verify the immunity of the system to environmental electrical phenomena, a series of immunity specification standards and tests must be applied to the powerline application.

The requirements for ac-connected ports, fixed by the EN50065-2-3 document (part 7-immunity specifications), include EN610000-4-4 (electric fast transients), EN610000-4-5 (surges), EN610000-4-6 (RF out-of-band disturbances), EN610000-4-11 (voltage dips).

In particular, surge tests are specified as both common and differential modes at level +/- 4 kV, with pulse shape 1.2 x 50 µs. Fast transient burst tests are specified at level +/- 2 kV, with pulse shape 5 x 50 ns and pulse frequency 5 kHz.

Figure 29, *Figure 30* and *Figure 31* illustrate the protection criteria implemented in the ST7540 reference design.

Figure 29 and *Figure 30* show the protection against common mode disturbances. The BAT54S diodes are intended to prevent the voltage on PA_OUT and Rx_IN lines from going above the supply rail (Vcc for PA_OUT and VDC for Rx_IN) or below ground, with a tolerance equal to the forward voltage of the diodes, that is nearly 0.3 V.

Figure 31 describes the protection intervention in case of differential mode disturbances. A differential voltage higher than 12 V is shorted by the bidirectional power transil, which is the most robust protection and also the one capable to absorb most of the energy of incoming disturbances.

Figure 29. Common mode disturbances protection - positive disturbance

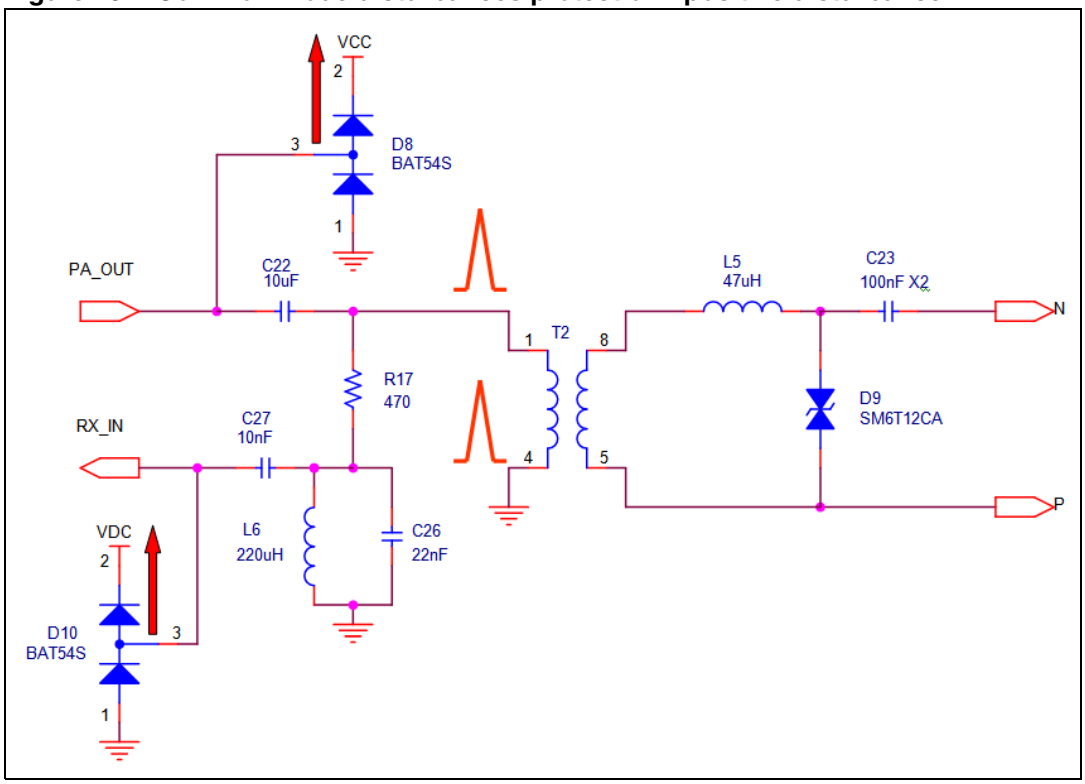


Figure 30. Common mode disturbances protection - negative disturbance

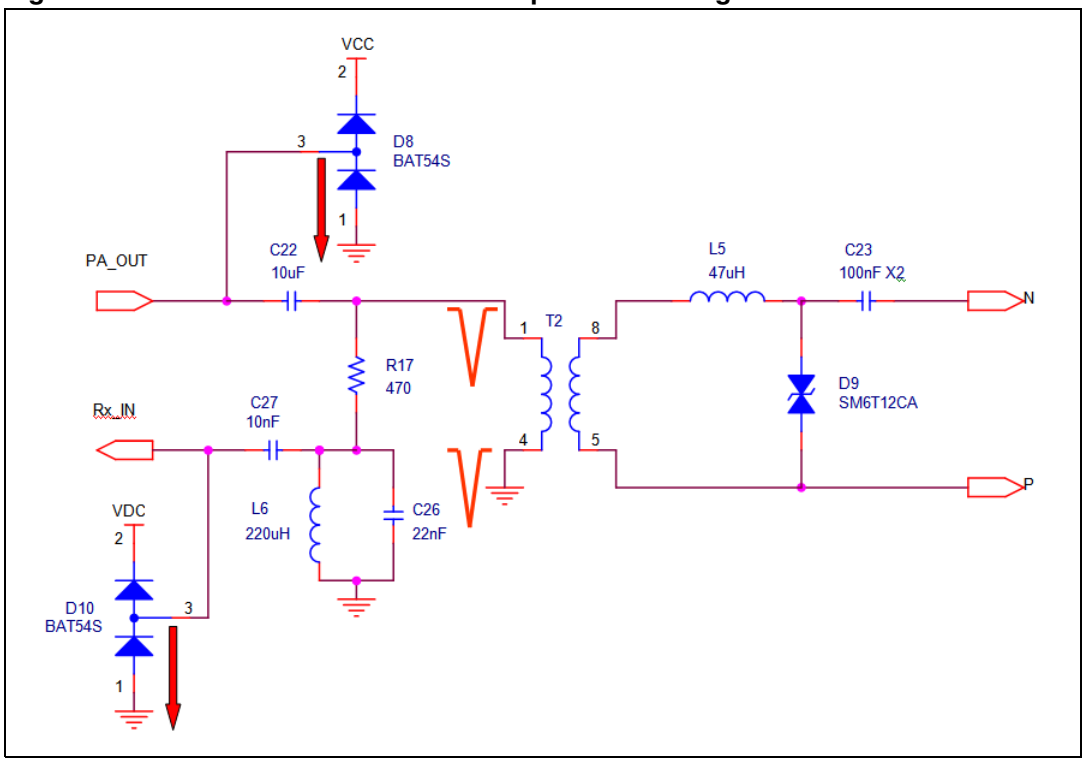
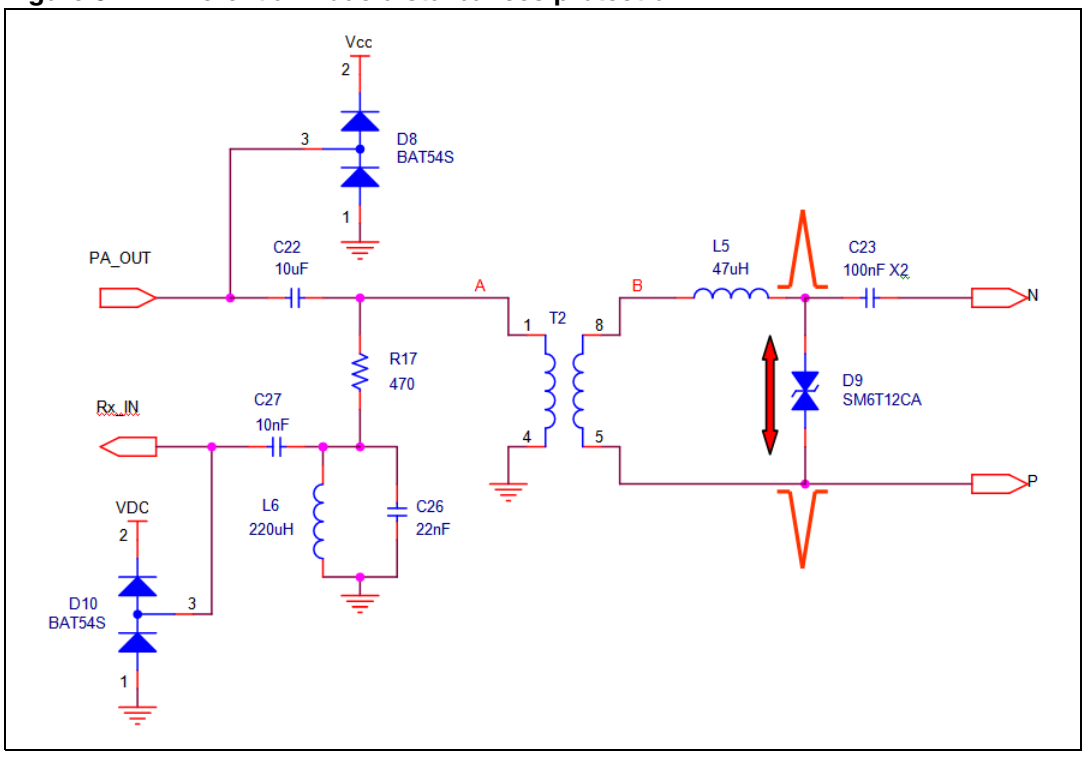
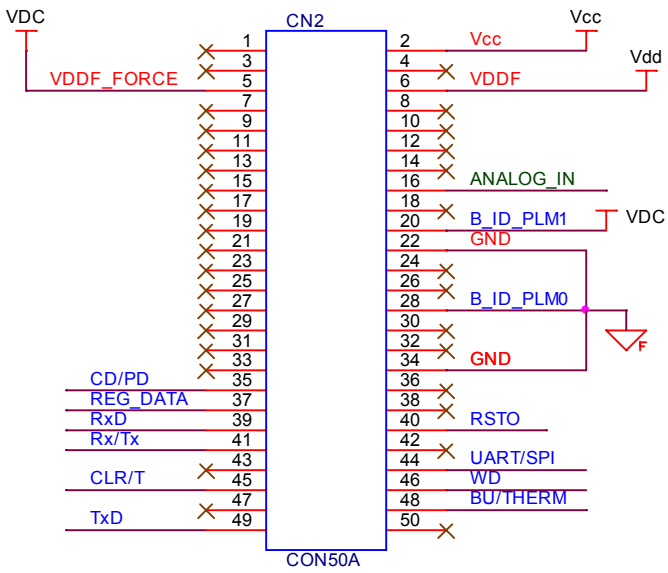


Figure 31. Differential mode disturbances protection



5.6 50-pin connector for the EVALCOMMBOARD

Figure 32. Scheme of the connector for the EVALCOMMBOARD



The ST7540 transceiver requires external digital control to communicate. This is done through an ST7 microcontroller which is accommodated on the EVALCOMMBOARD (see *Chapter 4 on page 11*). Communication with the ST7 microcontroller involves several signals, which can be gathered into 3 groups: Digital signals, Analog signals and Power connections. The signals for each group are listed in *Table 8*, *Table 9* and *Table 10*. Besides the ST7540 input and output signals, the link to the EVALCOMMBOARD includes:

- A 2-bit (B_ID_PLM_1 and B_ID_PLM_0) Board Identification Code, which identifies the hosted powerline transceiver. The microcontroller is able to recognize the ST7540 reference design board through a “10” binary configuration of this code.
- An Analog Input (ANALOG_IN), which is a line intended to implement a Received Signal Strength Indicator (a peak meter used to give an Rx signal level estimation).
- A VDDF_FORCE signal, which forces the microcontroller to refer digital interface levels to the VDDF (VDD) supply voltage provided by the ST7540 reference design board. This way both the modem and the microcontroller “talk” on the same digital levels.

Table 7. 50-pin connector digital signals

Pin number	Signal name	Description	Generated by
20	B_ID_PLM_1	Board ID for PLM applications (MSB)	PLC Board (VDC)
28	B_ID_PLM_0	Board ID for PLM applications (LSB)	PLC Board (GND)
35	CD/PD	Carrier or preamble detected signal	Modem
37	REG_DATA	Data communication or register access	µC
39	RxD	Serial data output	Modem
40	RSTO	Reset output	Modem

Table 7. 50-pin connector digital signals

Pin number	Signal name	Description	Generated by
41	RxTx	Receiving or transmission selection	µC
44	UART/SPI	Host Interface selection	µC
45	CLR/T	Serial data clock	Modem
46	WD	Watchdog timer reset	µC
48	BU/THERM	- Rx mode: band-in-use detection signal - Tx mode: thermal event signal	Modem
49	TxD	Serial data input	µC

Table 8. 50-pin connector analog signals

Pin number	Signal name	Description	Generated by
8	ANALOG_IN	Analog input (for µC processing)	-

Table 9. 50-pin connector power connections

Pin number	Signal name	Description	Generated by
2	PLM_10 V	12 V power supply	PLC Board
4	VDD	3.3 V / 5 V power supply	Modem
5	VDDF_Force	Force microcontroller digital level to VDDF	PLC Board (VDC)
6	VDDF	Digital power supply	Modem (VDD)
22,34	GND	Ground	-

5.7 Power supply

The ST7540 reference design includes a specifically designed Switching Mode Power Supply (SMPS) circuit, based on the ST VIPer12AS-E device.

The VIPer12AS-E is a smart power device with a current mode PWM controller, a startup circuit and protections integrated in a monolithic chip using VIPower M0 technology. It includes a 27 Ω Mosfet with 730 V breakdown voltage and a 400 mA peak drain current limitation. The switching frequency is internally fixed at 60 kHz, in order to provide a good compromise between EMI performances and magnetic parts dimensioning.

The internal control circuit offers the following benefits:

- large input voltage range on VDD pin accommodates changes in supply voltage
- automatic burst mode in low-load condition
- overload and short-circuit protection in hiccup mode

The power supply is designed in isolated flyback configuration. Secondary regulation, implemented through an optocoupler and a Zener diode, takes the requested output tolerance for the specified application into account.

The main specifications are listed in *Table 10*.

Table 10. SMPS specifications

Parameter	Value
Input voltage range, V_{in}	85-265 V_{ac}
Output voltage, V_{OUT}	12 V±10%
Peak output current, $I_{OUT(MAX)}$	500 mA

In the input stage, an EMI filter is implemented (C_1-L_2 plus C_3-L_3-C_2) for both differential and common mode noise, in order to fit the requested standard.

The blocking diode D_2 and the clamping network (R_2-C_4) clamp the peak of the leakage inductance voltage spike, assuring reliable operation of the VIPer12AS-E. D_2 must be very fast recovery and very fast turn-on to avoid additional drain overvoltage. The clamp capacitor C_4 must be low-loss (with polypropylene or polystyrene film dielectric) to reduce power dissipation and prevent overheating, since it is charged with high peak currents by the energy stored in the leakage inductance.

A Leading Edge Blanking (LEB) circuit for leakage inductance spikes filtering has also been implemented (Q_1 - C_5 - R_3). It blanks the spike appearing at the leading edges of the voltage generated by the self-supply winding, greatly improving short circuit behavior.

The output rectifiers have been selected to take the maximum reverse voltage and the RMS secondary current into account. A STPS1H100 Power Schottky rectifier has been chosen for this purpose.

A LC filter has been added on the output (consisting of L_4, C_9 and C_{29}) in order to filter the high frequency ripple without increasing the output capacitors size or quality.

The transformer used for this application has three windings, since one of them is needed to supply the VIPer12AS-E. The primary inductance has been chosen as 2.7 mH and the reflected voltage has been set to 80 V.

A layer type has been chosen with EF12.6 or E13/7/4 core.

The characteristics are listed in *Table 11*.

Table 11. SMPS transformer specifications

Parameter	Value
Core geometry	SRW12.6ES or E13/7/4
Primary inductance	2.7 mH±10%
Leakage inductance	180 µH max
N_P	224 turns – 0.1 mm
N_{AUX}	39 turns – 0.1 mm
N_{SEC}	31 turns – 0.2 mm (TEX-E wire)
Withstanding voltage	4 kV_{RMS}

Some significant waveforms are represented in the following figures. *Figure 33* and *Figure 34* show typical waveforms in both open-load and full-load conditions.

In any SMPS, protection against an output short-circuit is very important. All tests have been done by shorting the SMPS output at maximum input voltage. The results are given in *Figure 35*.

The main parameters are the drain-source voltage (V_{DS}), the output current (I_{OUT}) and the supply voltage (V_{DD}).

The output current is an important parameter to be checked during shorts. Although the output current peaks are quite high, the mean value is very low, thus preventing component melting for excessive dissipation. In this way, the output rectifier, transformer windings and PCB traces don't get overstressed. This assures system reliability against long-term shorts.

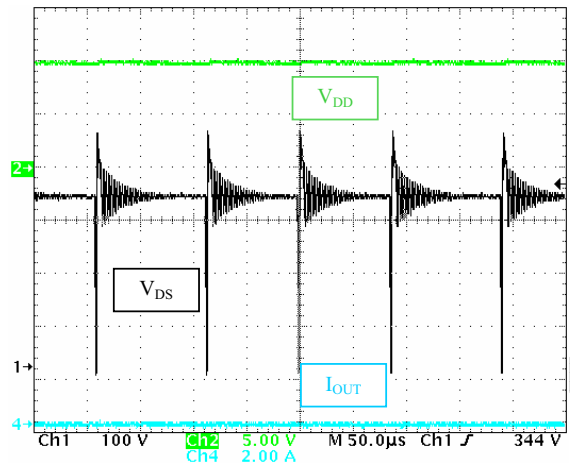
In case of device overheating, the integrated thermal protection stops the device operation until the device temperature falls.

The startup phase could be critical for the SMPS. Output overshoot occurs if the circuit is not properly designed. Care must be taken in designing a proper clamp network in order to prevent voltage spikes, due to leakage inductance, from exceeding the breakdown voltage of the device (730 V minimum value).

The startup transient is shown in *Figure 36*. It may be noted that the maximum drain-source voltage doesn't exceed the minimum breakdown voltage BV_{DSS}, with a reasonable safety margin.

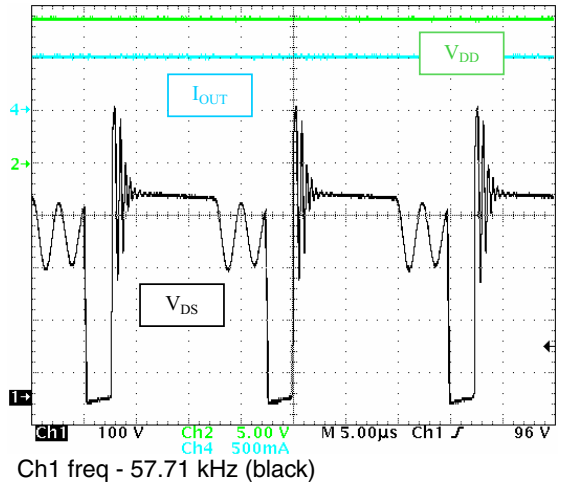
Finally, load regulation is presented in *Figure 37*, for different input voltages. With $230V_{ac}$, the output voltage ranges from 12.3V to 11.1 V, within the requested tolerance.

Figure 33. Typical waveforms at 230 V_{ac}: open load



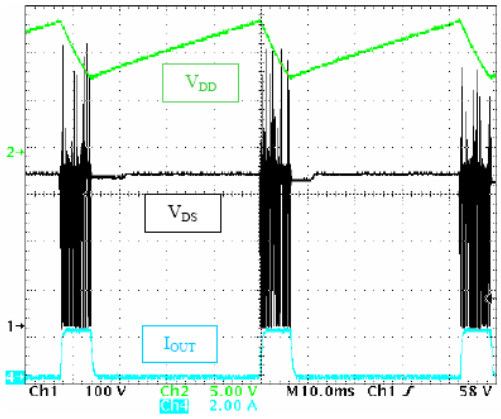
Ch1 freq - 9.62 kHz (black)
Ch2 mean - 9.90 V (green)

Figure 34. Typical waveforms at 230 V_{ac}: full load



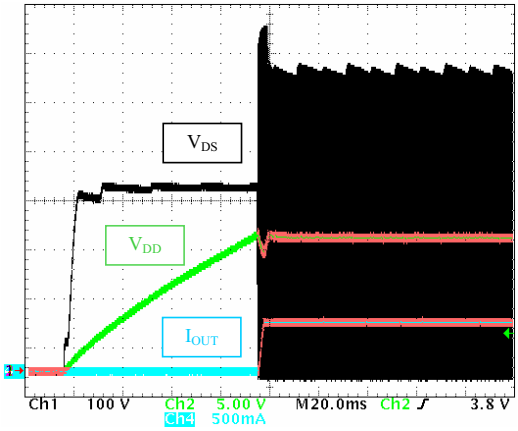
Ch1 freq - 57.71 kHz (black)
Ch2 mean - 13.79 V (green)
Ch4 max - 503 mA (light blue)

Figure 35. Typical waveforms at 265 V_{ac}: short-circuit



Ch1 freq - 23.50 Hz (green)
Ch4 max - 2.08 A (light blue)
Ch4 mean - 383 mA (light blue)

Figure 36. Typical waveforms at 265 V_{ac}: startup



Ch1 max - 702 V (black)
Ch2 mean - 19.72 V (green)
Ch4 max - 500 mA (light blue)

Figure 37. Load regulation

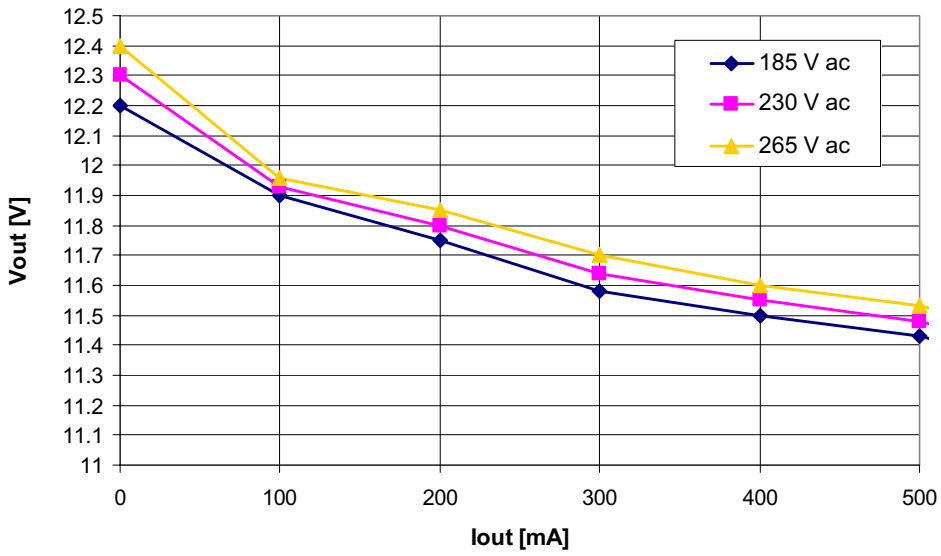
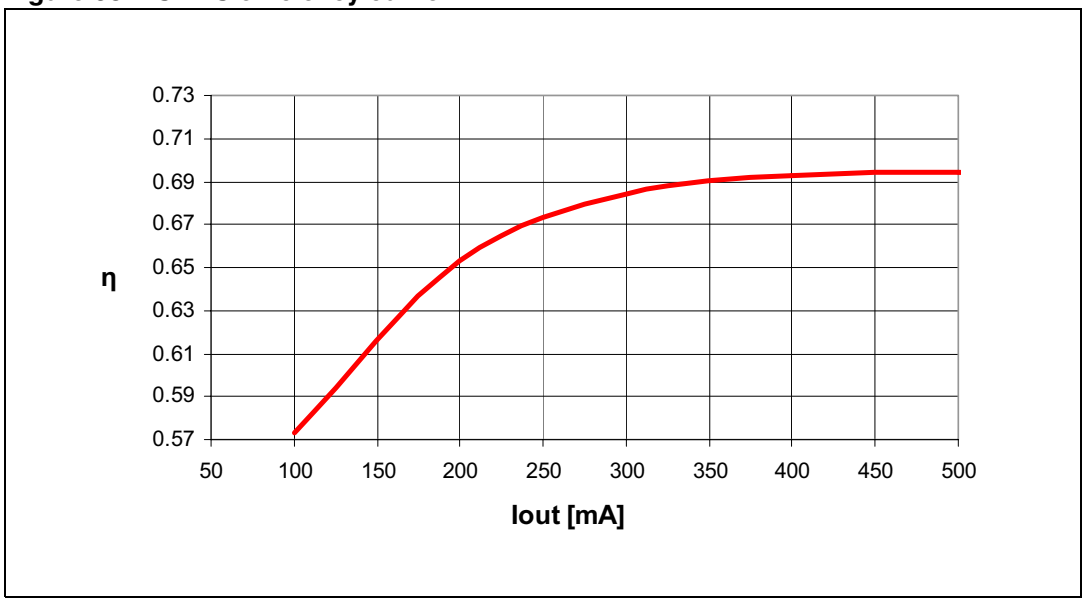


Figure 38 shows the efficiency vs. output current curve. Minimum efficiency occurs at low-load condition, as expected from any SMPS. This is not an issue for our application, since low efficiency corresponds also to low power consumption and thus to low dissipation.

On the other hand, at output current values over 500 mA (full-load condition), both the transformer and the VIPer are forced to operate close to their current limitations and thus the efficiency is reduced.

In general, efficiency is affected by the losses which are due to R1 (series input resistor limiting in-rush current) and to the filtering on both the primary and secondary side. Filtering is more important than efficiency because a powerline communication appliance has very restrictive EM disturbance limits and it is also highly sensitive to noise coming from the power supply.

Figure 38. SMPS efficiency curve



6 Performance and ping tests

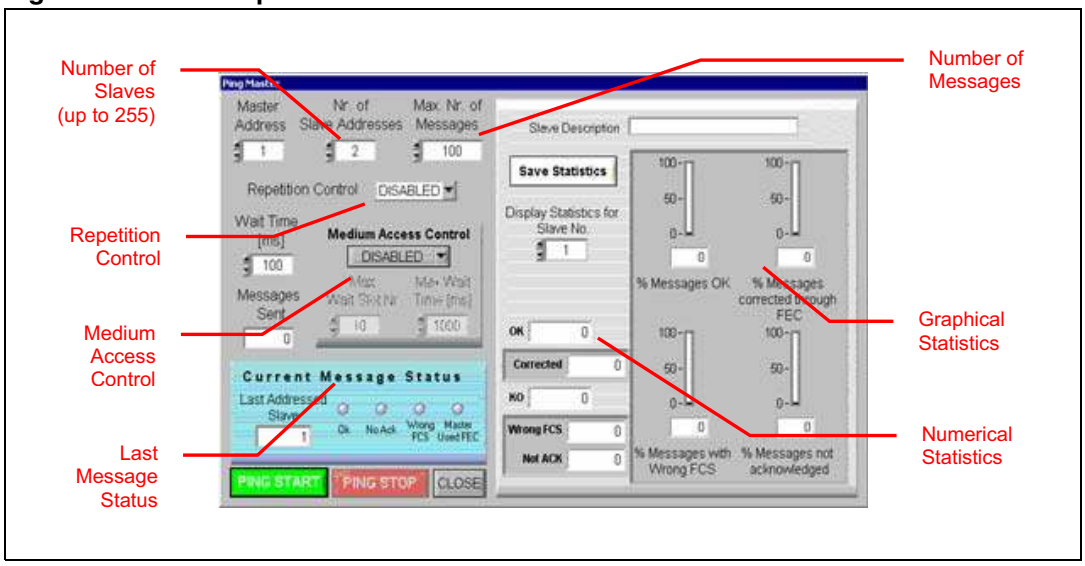
Our evaluation system includes a ping test embedded into the ST7540 powerline modem demonstration kit and the FW of the EVALCOMMBOARD. This feature allows the user to perform in-field communication tests and to evaluate reachability of PLC network nodes.

A ping session is based on a master board sending a sequence of messages to one or more slave boards. if the messages are correctly received by the slave boards, they are resent one by one to the master.

The PC connected to the master keeps statistics of the messages sent and correctly received by the slave boards, thus making it possible to get a numerical evaluation of the reachability of each node corresponding to a slave.

Figure 39 represents the ping window of the ST7540 powerline modem demonstration kit for the master node. The main characteristics of this tool are indicated in red.

Figure 39. ST7540 powerline modem demonstration kit window for the master board



Special controls are included in the ping test:

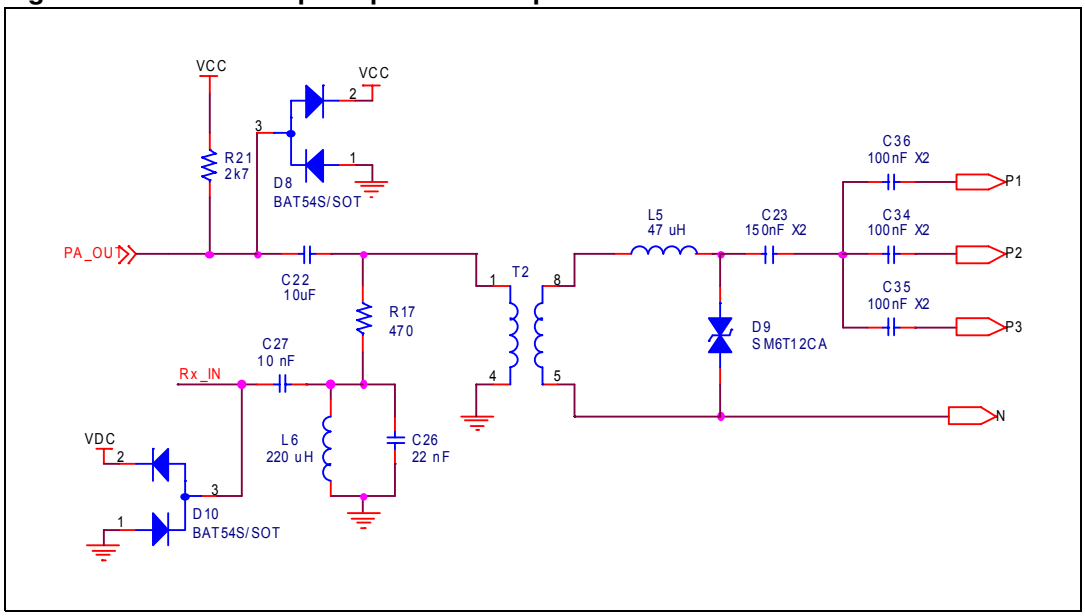
- Repetition control: may be used to improve communication reliability. When repetition control is enabled, a message not responded by a slave is resent up to three times before sending a new message
- Medium access control: defines what type of medium access has to be used. Choices are “none”, “BU” or “PD”. In the last two cases, messages are sent to the slave only if the BU or CD/PD lines of the ST7540 modem are not active. If the PD setting is selected, the content of the ST7540 internal control register is changed to select “Preamble” as the detection method.

For further details about ST7540 powerline modem demonstration kit, please refer to the user manual UM0239 “ST7540 power line modem demo kit graphical user interface”.

7 Application ideas

7.1 Three-phase architecture

Figure 40. Scheme of principle for three-phase architecture



The ST7540 modem can be used to communicate on a three-phase network. The coupling solution depicted in Figure 40 can be used.

In that topology, the total impedance that the ST7540 power amplifier is required to drive is equal to the parallel of the impedance seen on each of the three phases, so probably the device will be required to force an higher output current.

For concentrator nodes in metering networks (usually put at the low voltage substations), the impedance per each phase is higher, so the suggested solution will give better performance.

7.2 Zero crossing detector

Often, in AMR (Automatic Meter Reading) applications, it is necessary to know which phase each meter is placed on. This information is mainly useful at system level in order to check for unexpected losses on the distribution line due to failures or energy theft.

Since the three phases on the mains are sinusoidal waveforms with a phase shift of 120° from each other (equal to 6.67 ms at 50 Hz / 5.5 ms at 60 Hz), the simplest way to associate the meter to its correct phase is to synchronize the transmission to the phase itself. To do that, the meter should always start its transmission synchronously with zero voltage transitions on its phase and the concentrator should measure the delay between the beginning of the incoming frame and the transition on its reference phase. The act of detecting the zero voltage transitions on the mains phase is called zero crossing detection.

Figure 41 and *Figure 42* show two possible zero crossing detector circuit implementations. N and P mean neutral and phase lines respectively at the meter/concentrator side, while ZC_OUT is a digital output to the application microcontroller.

Particular attention should be paid to current rating (see solution in *Figure 42*) The maximum allowable current for 1W dissipation, sustainable by two ½ W resistors in a series, is 4.5 mA rms = 6.4 mA peak.

Such a current flowing into the LED of the optocoupler can minimize the delay between the actual zero crossing of the mains voltage and the edge of the ZC_OUT signal, if the optocoupler has been chosen to have an activation current I_F about 10 times smaller than the peak current.

Figure 43 shows the behavior of the ZC_OUT digital signal versus the AC Mains Input for both circuits.

Warning: The circuit in *Figure 41* is only applicable to a non-isolated board topology. It is not possible to implement it directly on the ST7540 reference design.

Figure 41. Schematic of a zero crossing detection circuit for non-isolated coupling

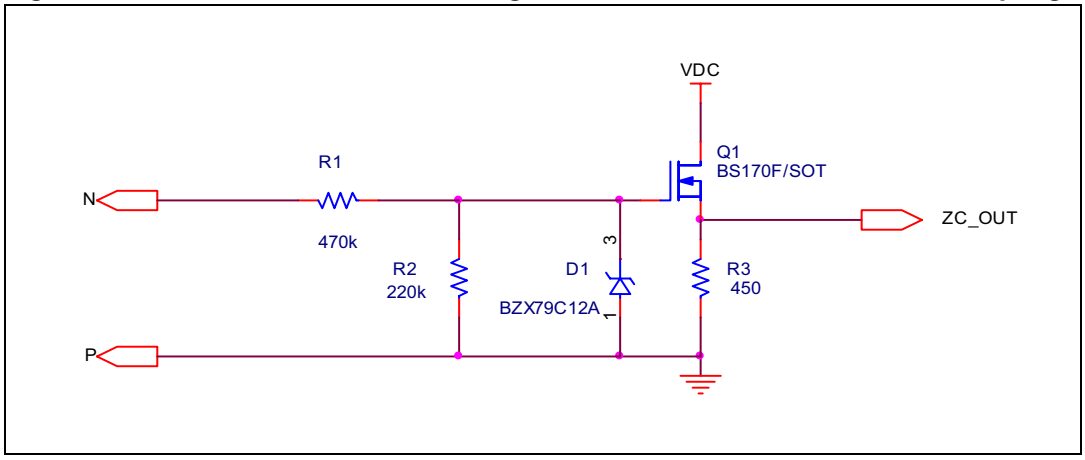


Figure 42. Schematic of a zero crossing detection circuit for isolated coupling

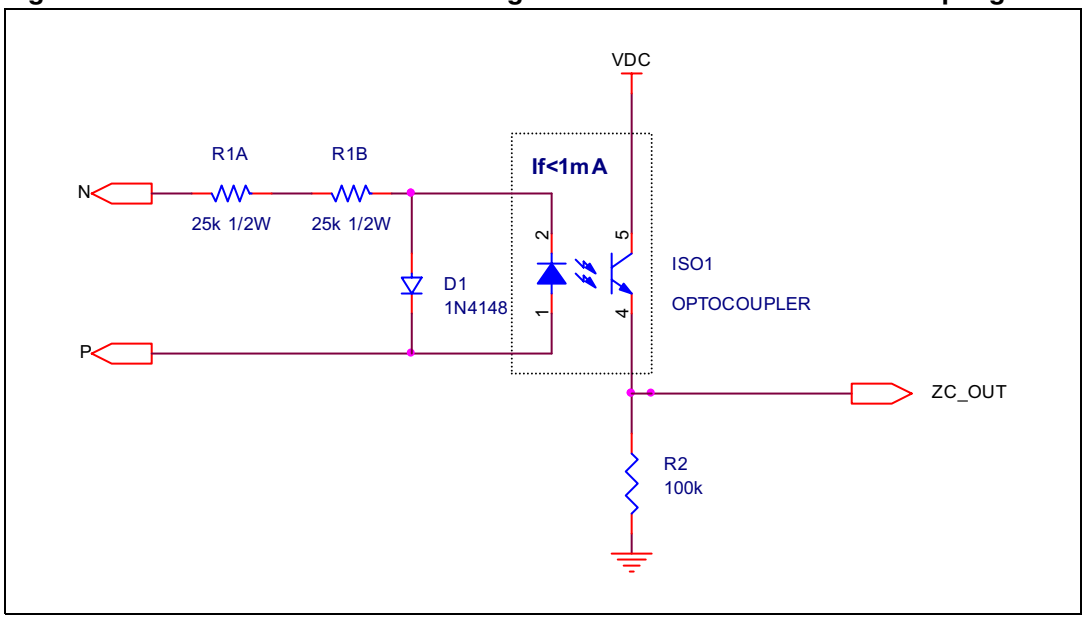
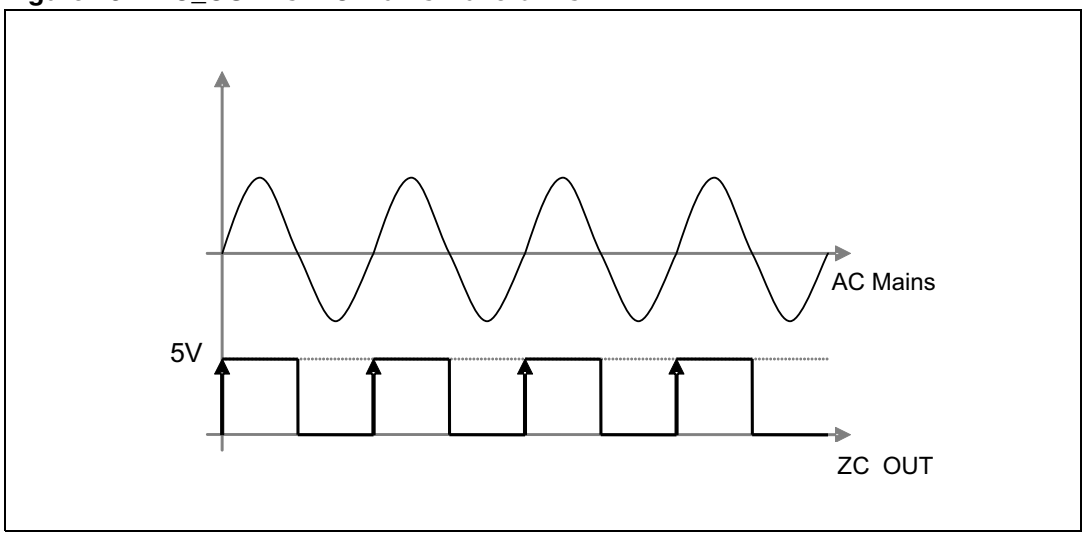


Figure 43. ZC_OUT vs. AC mains waveforms



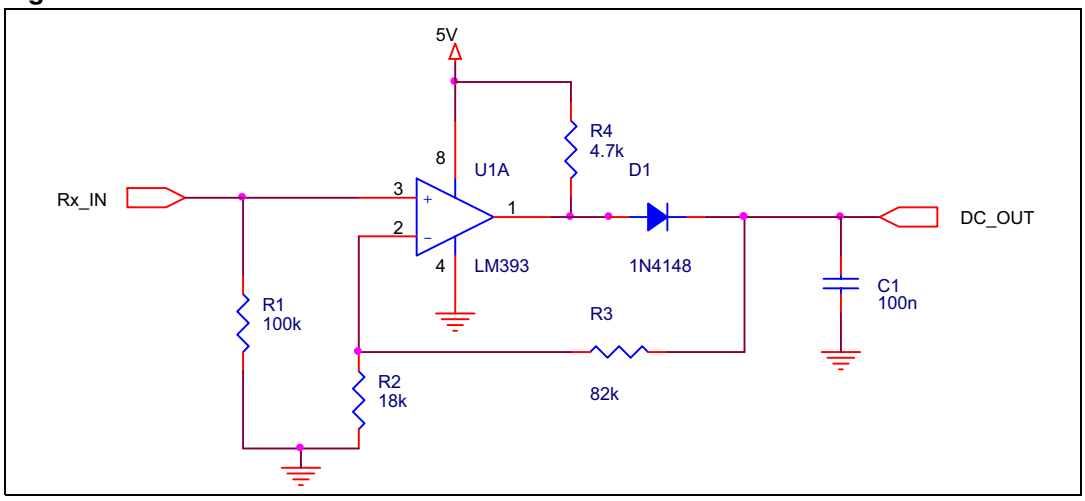
7.3 Received signal strength indicator (RSSI)

In many application fields, measuring the strength of the incoming signal is useful to:

- Evaluate the SNR (signal to noise ratio) at the node
- Choose the best routing through the network (if repeaters are allowed)

One possible implementation for the received signal strength indicator (RSSI) is the one depicted in *Figure 44*, where a peak detector is used to measure the amplitude of the incoming signal.

Figure 44. Peak detector electrical schematic

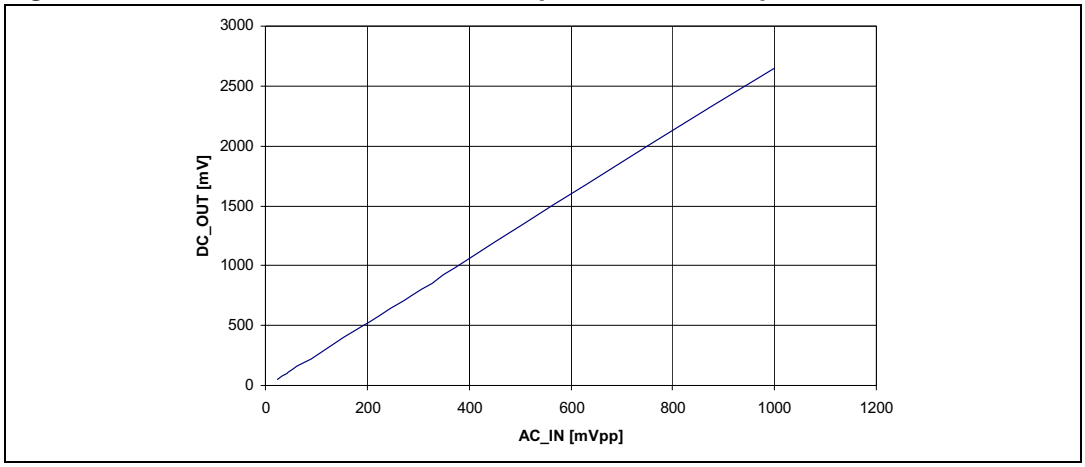


The schematic above is based on a simple diode-capacitor (D1-C1) circuit improved with an LM393 comparator so that:

- The comparator eliminates the diode reverse voltage.
- The feedback network (R3/R2) introduces a gain of 4 to improve performance against low amplitude signals.

In the end this circuit gives, on DC_OUT line, a DC voltage proportional to the AC peak-to-peak level at the input. *Figure 45* shows the measured behavior of this circuit with a given pure sinusoidal waveform at the input. The DC_OUT signal should be converted through an integrated A/D converter by the application microcontroller.

Figure 45. Measured DC_OUT Vs. AC_IN peak detector response

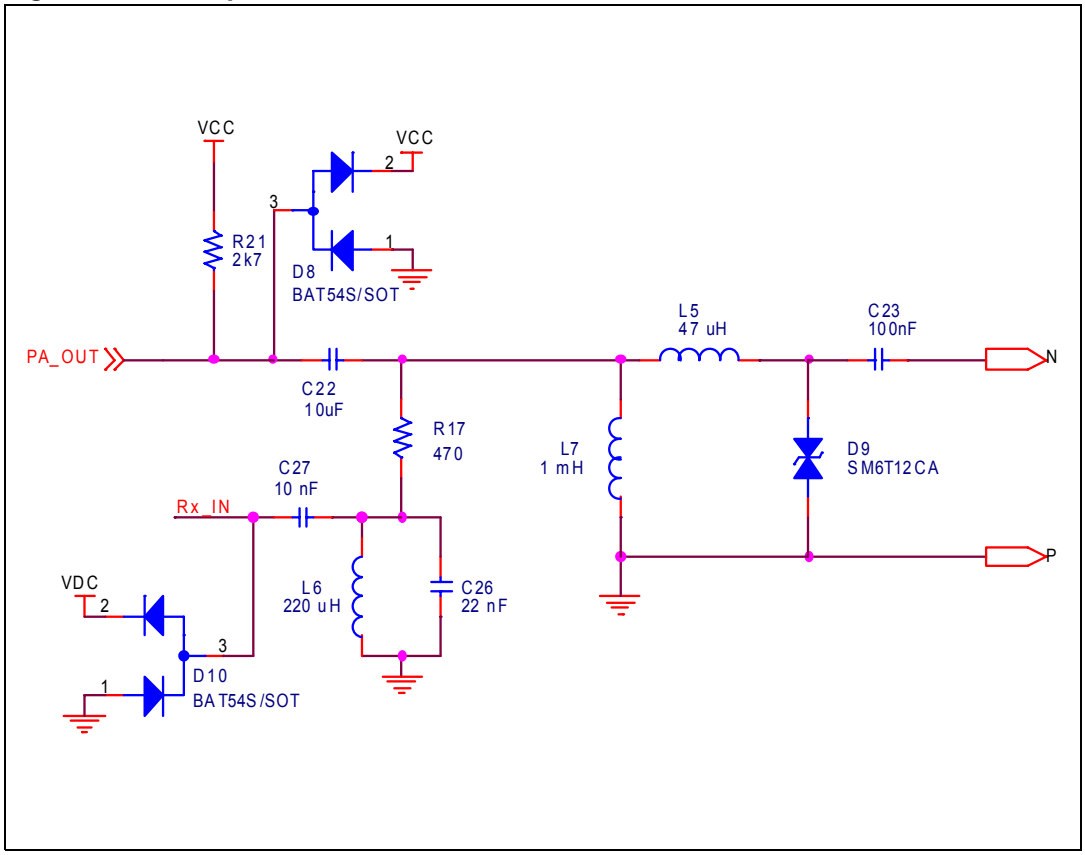


7.4 Non-isolated coupling

A possible alternative solution for line coupling is a non-isolated circuit. An example is shown in *Figure 46*, in which the transformer T2 has been substituted with the shunt inductor L7. The value of the inductor has been chosen to give about 100 dB rejection to the mains voltage through a C23-L7 high pass filter. Advantages arising from non-isolated

topologies mainly include cost optimization, eliminating the need for isolation components, and circuit simplicity.

Figure 46. Example schematic for non-isolated solution



7.5 DC powerline applications

The ST7540 reference design can be adapted to communicate over a DC power line. In this case, the schematic of *Figure 46* has to be referred to as line coupling, with two modifications: L7 can be removed and the C23 capacitor can be substituted with a lower voltage ceramic component.

A DC-DC converter will substitute the ac-dc SMPS. For example, the L5970 DC-DC step-down switching regulator can be used in case of 24 V bus to obtain the 12 V supply for the ST7540 device.

7.6 110 and 132.5 kHz coupling circuit

In this paragraph application circuits for CENELEC band B and C are provided. The 110 and 132.5 kHz channels of the ST7540 transceiver are suitable for home automation applications and in general for applications not subject to the European AMR regulations.

Figure 47 and *Figure 48* show the schematics for the line coupling interface tuned respectively to the 110 and 132.5 kHz channels.

Figure 47. Line coupling interface for 110 kHz channel

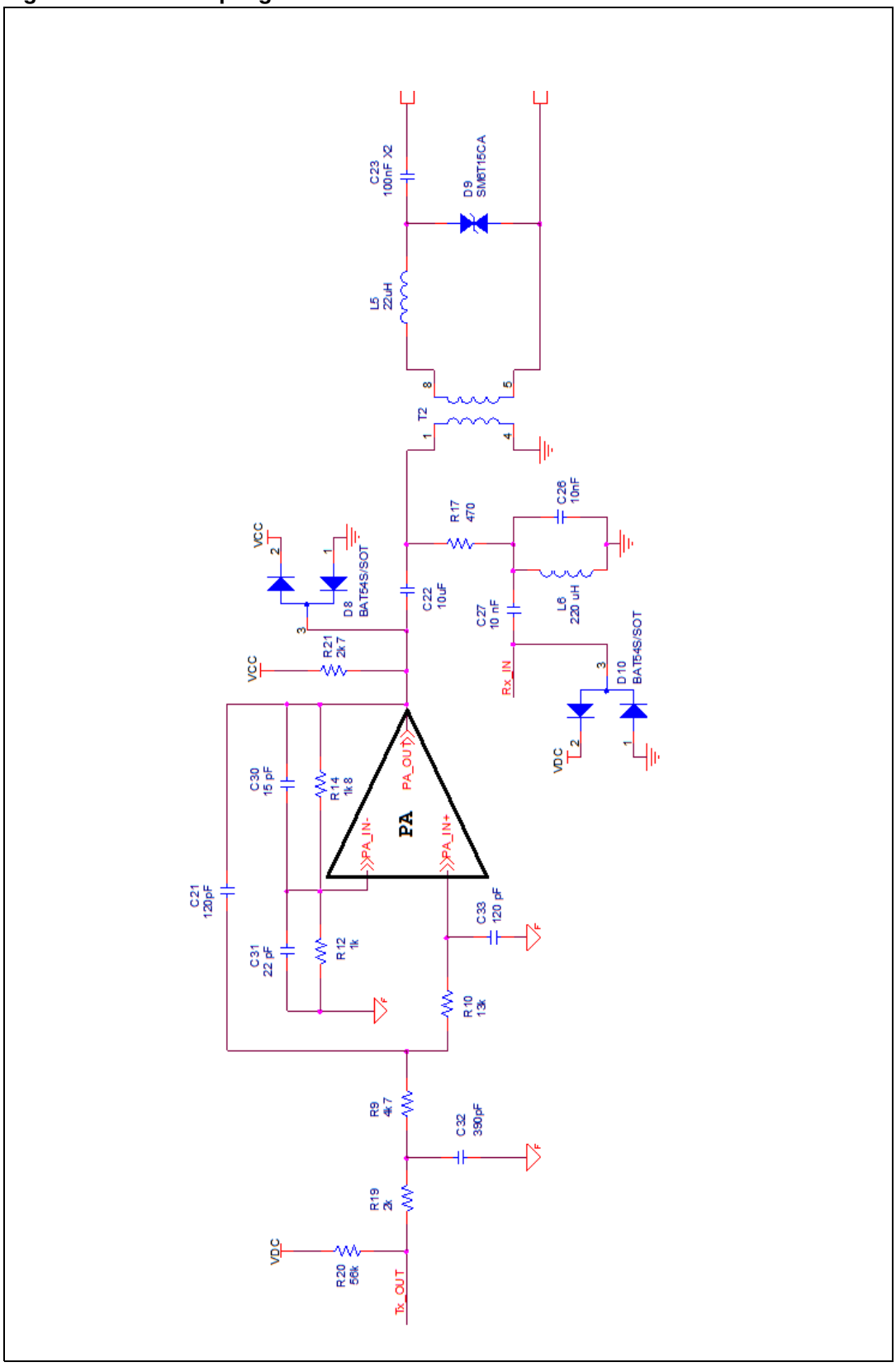
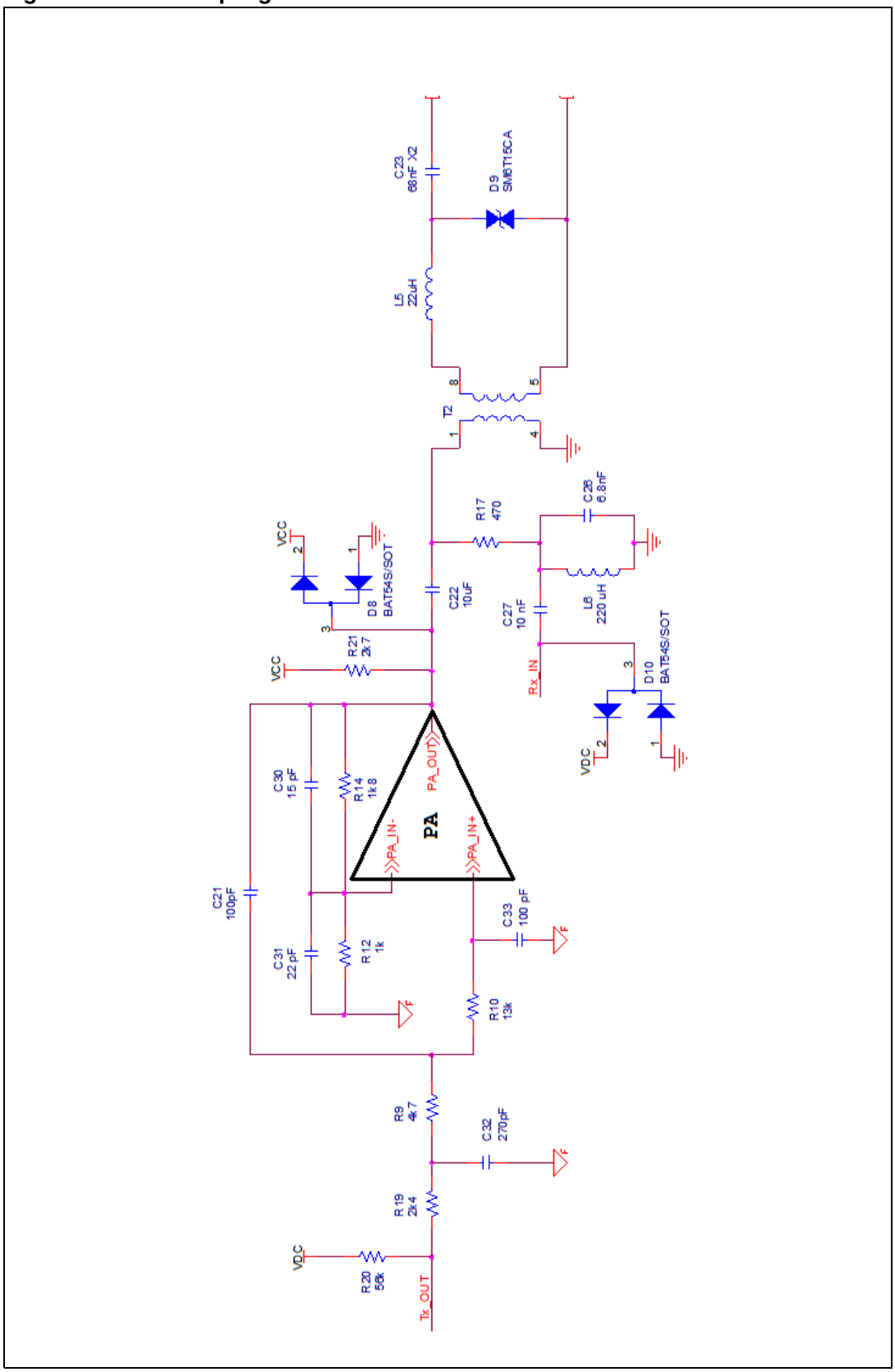


Figure 48. Line coupling interface for 132.5 kHz channel



8 Troubleshooting

In this section the most frequently asked questions are described.

1. Problem: the ST7540 reference design board does not work at all.

What to check:

   a) Check that the AC mains supply cable is well connected to CN1.
   b) Check if the green LED D6 is on.
   c) Check the voltage on the Vcc test pad. The value must be about 12 V.

2. Problem: the ST7540 reference design board is not responding.

What to check:

   a) Check the VDC voltage. The value must be about 5 V. In a noisy environment, spurious voltage spikes could compromise the internal linear regulator startup.
   b) If Vdd is not externally connected to the VDC line, verify the Vdd voltage. The value must be about 3.3 V.
   c) Check if the MCLK selected frequency is present.
   d) Check the connection between the reference design board and the EVALCOMMBOARD and the connection between the EVALCOMMBOARD and the PC.

3. Problem: the ST7540 reference design board does not transmit.

What to check:

   a) Check the voltage on the PA_OUT test pad with the oscilloscope ground probe connected to the SVss signal ground. The programmed carrier frequency must be present on the PA_OUT line.
   b) Check there is no short-circuit impedance on the mains at the transmitting frequency.
   c) Check the CL voltage. It fixes the current limiting threshold. It has to be lower than 1.9 V, otherwise the IC is put in current-limit mode.

If the current-limit mode is forced on the transceiver, modify the value of the R6 feedback resistor to exit from limitation according to the actual load forced by the mains network.

4. Problem: the ST7540 reference design board transmits only for a short time.

What to check:

   a) Check the transmission timeout setting. It has to be disabled for continuous transmission.
   b) Check if continuous or single sequence transmission is selected in the Tx panel of the ST7540 powerline modem demonstration kit window. Select continuous mode to be able to force a lasting transmission.
   c) Check there is no short-circuit impedance on the mains at the selected transmitting channel.

5. Problem: the ST7540 reference design board does not receive.

What to check:

a) Check if the carrier frequency is present on the RAI pin voltage with the oscilloscope ground probe connected to the DVss signal ground pin.

b) Check that the transmitting frequency matches the carrier frequency selected through the control register panel of the ST7540 powerline modem demonstration kit window.

c) Check the preamble detection setting on the control register panel of the ST7540 powerline modem demonstration kit window.

d) Check if data are present on the RxD pin.

6. Problem: during a ping test or a transmission test, the ST7540 reference design board shows high bit error rate.

Note: This point refers to a half-duplex communication involving two ST7540 reference design boards communicating with each other.

What to check:

a) Check that both reference design boards are programmed to transmit/receive on the same carrier frequency.

b) Check preamble detection setting on the control register panel of the ST7540 powerline modem demonstration kit window.

c) Check if the carrier frequency is present on the RAI pin voltage with the oscilloscope ground probe connected to the DVss signal ground pin.

d) Check if data are present on the RxD pin.

Appendix A Board layout

Figure 49. PCB layout - component placing

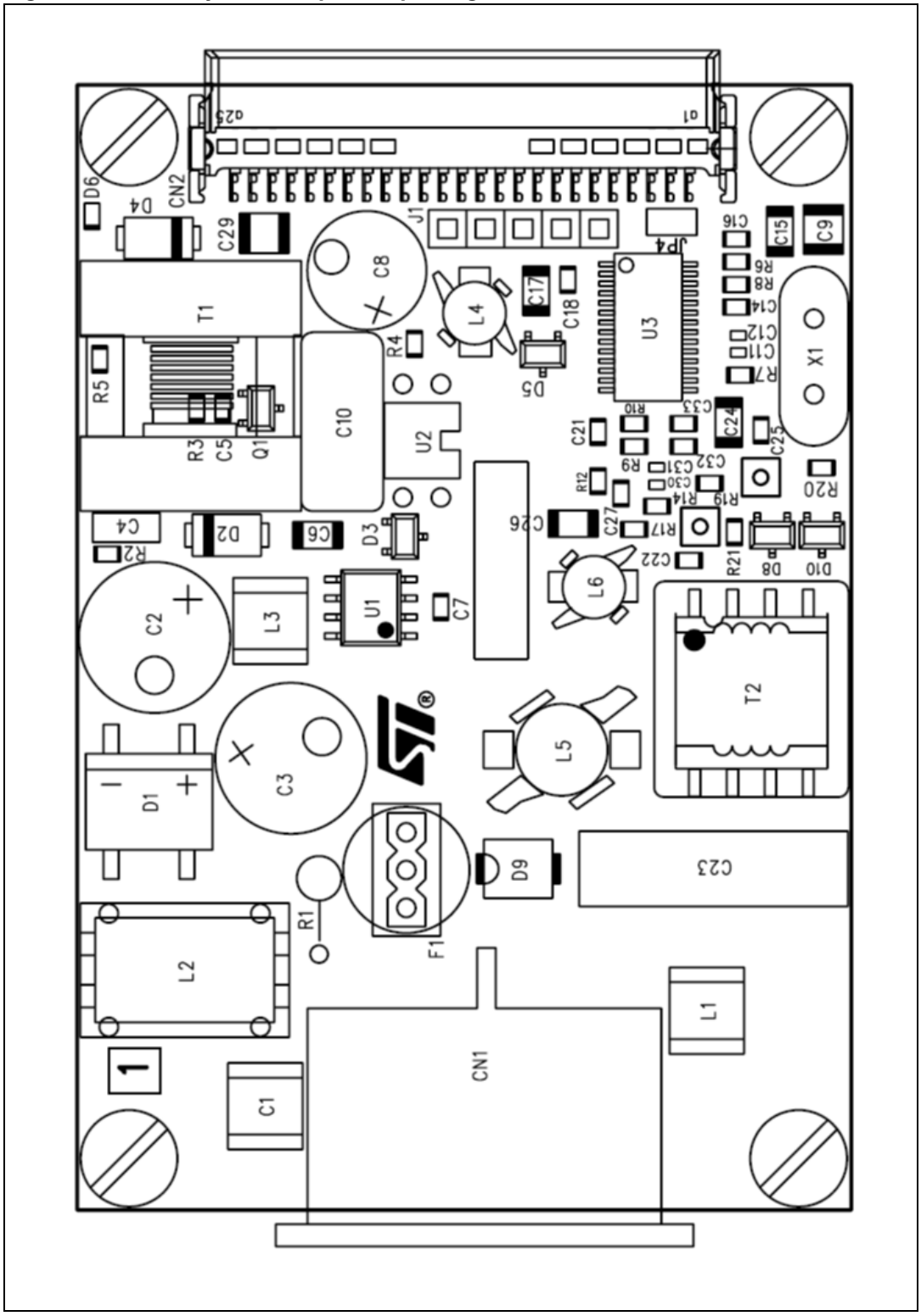


Figure 50. PCB layout - top view

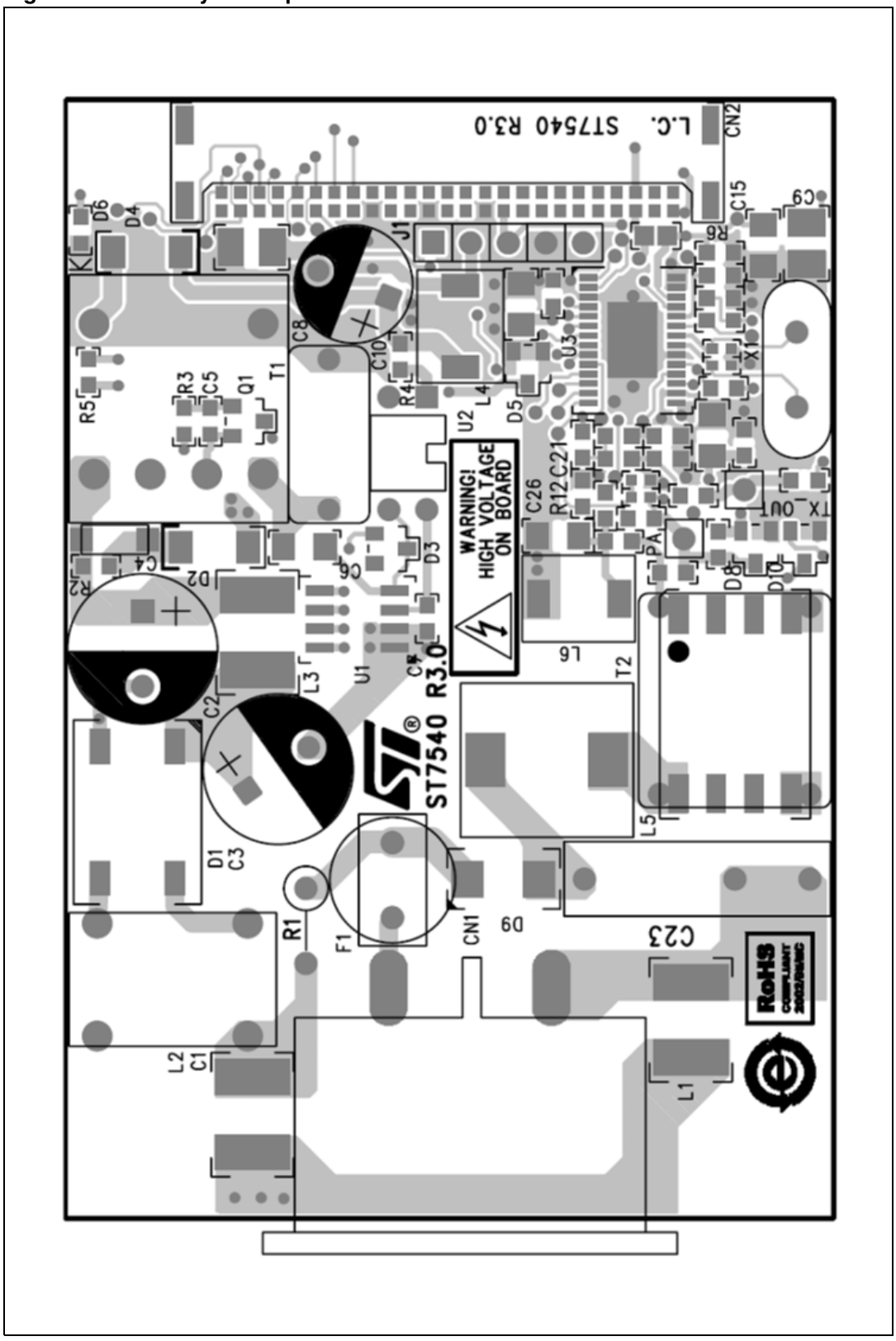
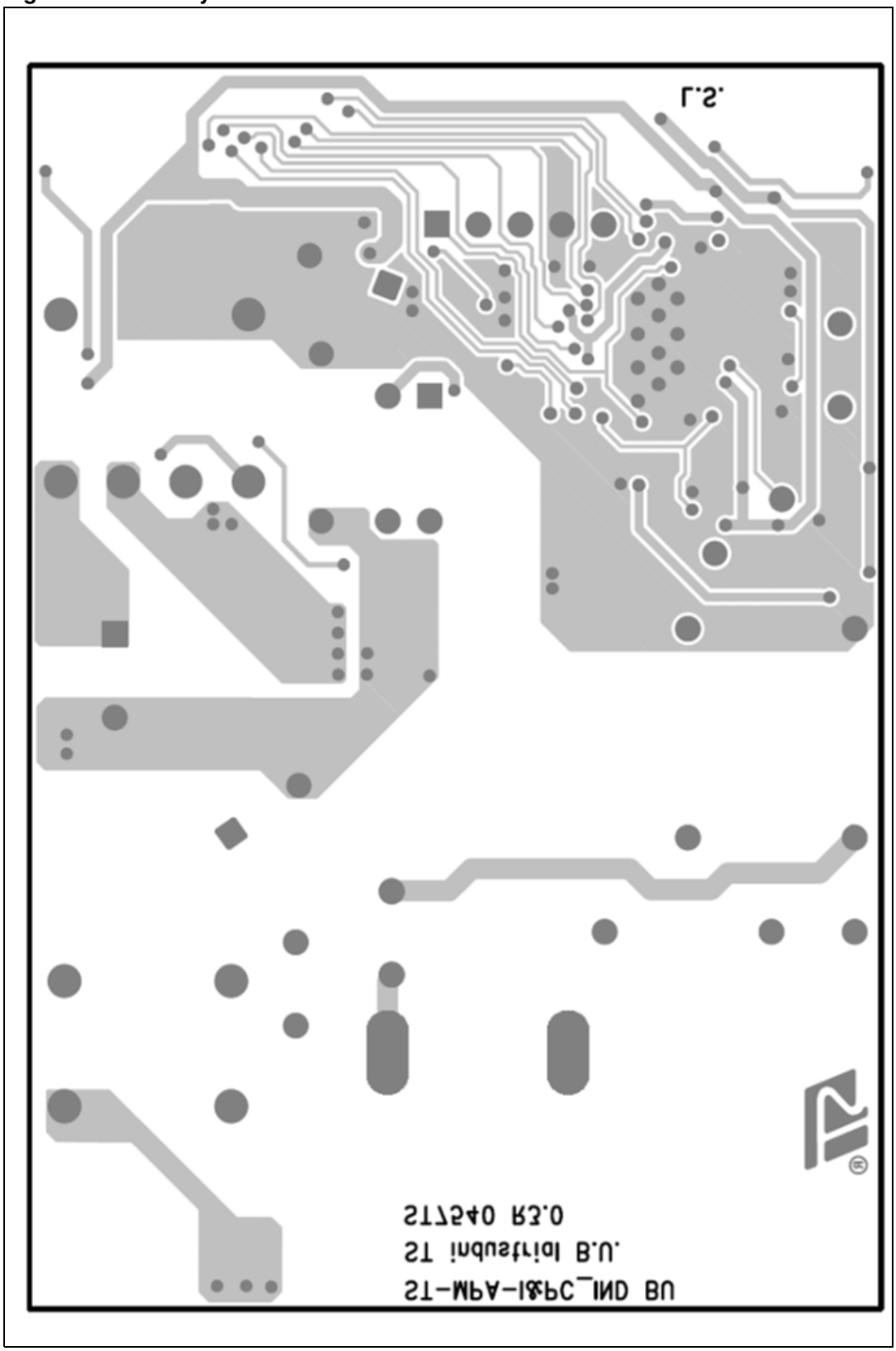


Figure 51. PCB layout - bottom view



List of normative references

EN50065: Signaling on low voltage electrical installations in the frequency range 3 kHz to 148.5 kHz.

- Part 1: General requirements, frequency bands and electromagnetic disturbances
- Part 2-1: Immunity requirements
- Part 4-2: Low voltage decoupling filters - safety requirements
- Part 7: Equipment impedance

Revision history

Table 12. Document revision history

Date	Revision	Changes
10-Jan-2007	1	First issue
28-Jan-2008	2	*Figure 2*, *7*, *8*, *9*, *23*, *46*, *49*, *50* and *51* modified *Figure 47* inserted *Table 3*, *4* and *5* modified *Section 7.5* and *7.6* inserted *Equation 2* modified
19-Jan-2010	3	Updated *Figure 1*, *2*, *5*, *6*, *7*, *9*, *10*, *11*, *12*, *13*, *14*, *15*, *16*, *17*, *18*, *19*, *29*, *30*, *31*, *40*, *46*, *47*, *48*, *49*, *50* and *51* Updated *Table 1*, *3* and *4*