7A SINGLE CHANNEL MOBILE PWM SWITCHING REGULATOR

TARGET SPECIFICATION

Pb Free Product

DESCRIPTION

The NX9548 is buck switching converter in multi chip module designed for step down DC to DC converter in portable applications. It is optimized to convert single supply up to 20V bus voltage to as low as 0.75V output voltage.The output current can be up to 7A. It can be selected to operate in synchronous mode or non-synchronous mode to improve the efficiency at light load. Constant on time control provides fast response, good line regulation and nearly constant frequency under wide voltage input range. Over current protection and FB UVLO followed by latch feature. Other features includes: internal boost schottky diode, 5V gate drive capability, power good indicator, over current protection, over voltage protection and adaptive dead band control.NX9548 is available in 5x5 MCM package.

FEATURES

- Internal Boost Schottky Diode
- Ultrasonic mode operation available
- Bus voltage operation from 4.5V to 20V
- Less than 1uA shutdown current with Enable low
- Excellent dynamic response with constant on time control
- Selectable between Synchronous CCM mode and diode emulation mode to improve efficiency at light load
- Programmable switching frequency
- Current limit and FB UVLO with latch off
- Over voltage protection with latch off

APPLICATIONS

- UMPC, Notebook PCs and Desknotes
- Tablet PCs/Slates
- On board DC to DC such as 12V to 3.3V, 2.5V or 1.8V
- Hand-held portable instruments

TYPICAL APPLICATION

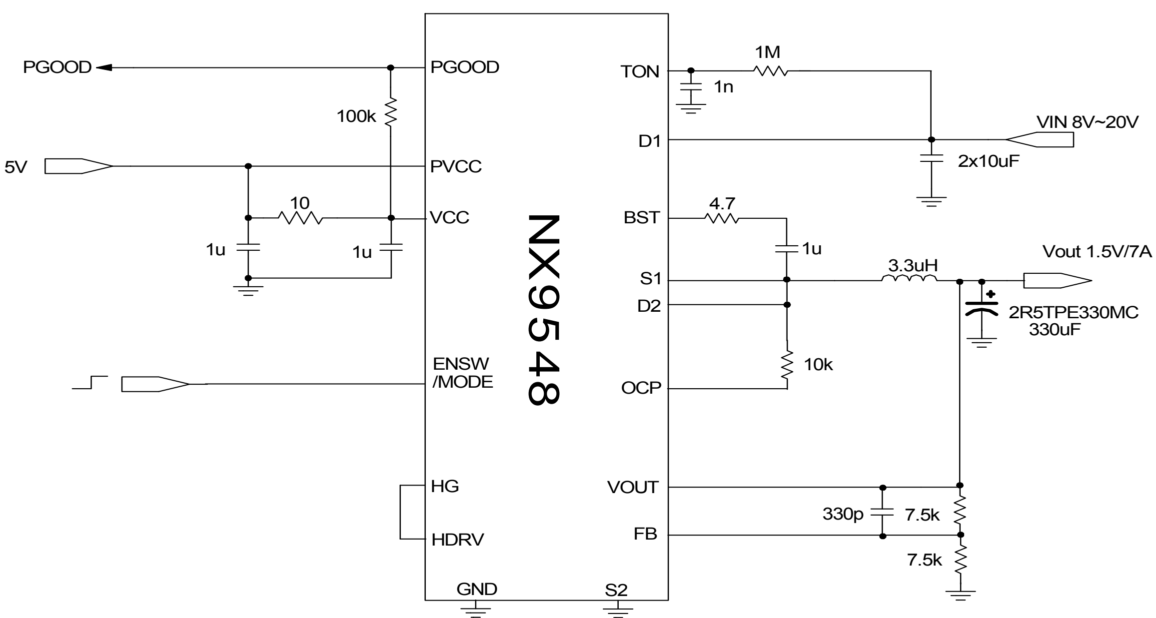


Figure 1 -Typical application of 9548

ORDERING INFORMATION

Device	Temperature	Package	Pb-Free
NX9548CMTR	0 to 70°C	5X5 MCM-32L	Yes

Microsemi
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 800-877-6458, 714-898-8121, Fax: 714-893-2570

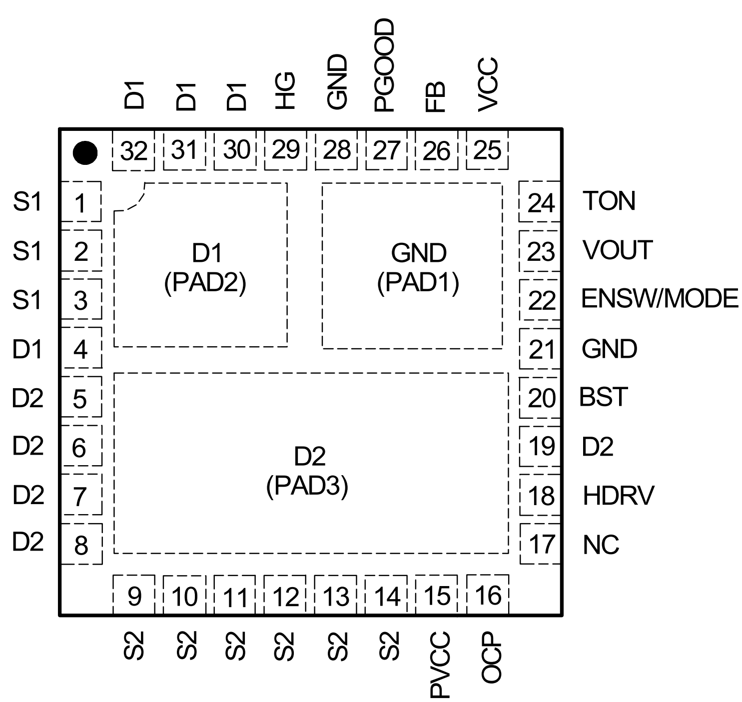
ABSOLUTE MAXIMUM RATINGS

VCC,PVCC to GND & BST to SW voltage .... -0.3V to 6.5V
TON to GND .... -0.3V to 28V
HDRV to SW Voltage .... -0.3V to 6.5V
D1 to S1and D2 to S2 .... 30V
All other pins .... -0.3V to VCC+0.3V or 6.5V
Storage Temperature Range .... -65°C to 150°C
Operating Junction Temperature Range .... -40°C to 125°C
ESD Susceptibility 2kV
Power Dissipation .... Internally Limited by OTP

CAUTION: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

PACKAGE INFORMATION

32-LEAD PLASTIC MCM 5 x 5



ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc = 5V, V_{IN} = 12V and T_A = 0 to 70°C. Typical values refer to T_A = 25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
VIN						
recommended voltage range			4.5		20	V
Shut down current		ENSW=GND		1		uA
VCC,PVCC Supply						
Input voltage range	V_{in}		4.5		5.5	V
Operating quiescent current		FB=0.85V, ENSW=5V		1.8		mA
Shut down current		ENSW=GND		1	u	A
VCC UVLO						
Under-voltage Lockout threshold	V_{CC}_UVLO		3.9	4.1	4.5	V
Falling VCC threshold			3.7	3.9	4.3	V
ON and OFF time						
TON operating current		VIN=15V, Rton=1Mohm		15		uA
ON -time	V	IN=9V,VOUT=0.75V,Rton =1Mohm	312	390	468	ns
Minimum off time			380	590	800	ns
FB voltage						
Internal FB voltage	Vref		0.739	0.75	0.761	V
Input bias current				200		nA
Line regulation		VCC from 4.5V to 5.5V	-1		1	%
OUTPUT voltage						
Output range			0.75		5	V
VOUT shut down discharge resistance		ENSW/MODE=GND		30		ohm
Soft start time				1.5		ms
PGOOD						
PGOOD high rising threshold				90		% Vref
PGOOD delay after softstart		NOTE1		1.6		ms
PGOOD propagation delay filter		NOTE1		2		us
PGOOD hysteresis				5		%
PGOOD output switch impedance		13				ohm
PGOOD leakage current				1		uA
ENSW/MODE threshold and bias current						
PFM/Non Synchronous Mode			80% VCC		VCC+ 0.3V	V
Ultrasonic Mode			60% VCC		80% VCC	V
Synchronous Mode		Leave it open or use limits in spec	2		60% VCC	V
Shutdown mode			0		0.8	V
Input bias current		ENSW/MODE=VCC		5	u	A
		ENSW/MODE=GND	-	5		uA

Microsemi
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11861 Western Avenue, Garden Grove, CA. 92841, 800-877-6458, 714-898-8121, Fax: 714-893-2570

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
SW zero cross comparator						
Offset voltage				5		mV
Current Limit						
Ocset setting current			20	24	28	uA
Over temperature						
Threshold	N	OTE1		155		°C
Hysteresis				15		°C
Under voltage						
FB threshold				70		%Vref
Over voltage						
Over voltage tripp point				125		%Vref
Internal Schottky Diode						
Forward voltage drop		forward current=50mA		500		mV
Ouput Stage						
High Side MOSFET R_{DSON}				23		mohm
Low Side MOSFET R_{DSON}				20		mohm
Output Current				7		A

NOTE1: This parameter is guaranteed by design but not tested in production(GBNT).

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1-3	S1	Source of high side MOSFET. These pins must be connected directly to the drain of low side MOSFET via a plane connection.
4,30-32 PAD2	D1	Drain of high side MOSFET
5-8,19, PAD3	D2	Drain of low side MOSFET and the controller pin out SW
9-14	S2	Source of low side MOSFET and need to be directly connected to power ground via multiple vias.
15	PVCC	This pin provides the voltage supply to the lower MOSFET drivers. Place a high frequency decoupling capacitor 1uF X5R from this pin to GND.
16	OCP	This pin is connected to the drain of the external low side MOSFET via resistor and is the input of the over current protection(OCP) comparator. An internal current source is flown from this pin to the external resistor which sets the OCP voltage across the Rdson of the low side MOSFET. Current limit point is this voltage divided by the Rds-on. Once this threshold is reached the chip is latched out.
17	NC	Not used.
18	HDRV	High side gate driver output which needs to be connected to high side MOSFET gate HG pin. A small value resistor may be placed between two pins to slow down the high side MOSFET, reducing the ringing on SW nodes.
20	BST	This pin supplies voltage to high side FET driver. A minimum high freq 0.47uF ceramic capacitor is placed as close as possible to and connected to this pin and respected pin 19. A 4.7ohm resister is recommended in series with this capacitor.
22	ENSW/ MODE	Switching converter enable input. Connect to VCC for PFM/Non synchronous mode, connected to an external resistor divider equals to 70%VCC for ultrasonic, connected to GND for shutdown mode, floating or connected to 2V for the synchronous mode.
23	VOUT	This pin is directly connected to the output of the switching regulator and senses the VOUT voltage. An internal MOSFET discharges the output during turn off.
24	TON	VIN sensing input. A resistor connects from this pin to VIN will set the frequency. A 1nF capacitor from this pin to GND is recommended to ensure the proper operation.
25	VCC	This pin supplies the internal 5V bias circuit. A 1uF X7R ceramic capacitor is placed as close as possible to this pin and ground pin.
26	FB	This pin is the error amplifiers inverting input. This pin is connected via resistor divider to the output of the switching regulator to set the output DC voltage from 0.75V to 3.3V.
27	PGOOD	PGOOD indicator for switching regulator. It requires a pull up resistor to Vcc or lower voltage. When FB pin reaches 90% of the reference voltage PGOOD transitions from LO to HI state.
21,28 PAD1	GND	Ground pin.
29	HG	High side MOSFET gate.

BLOCK DIAGRAM

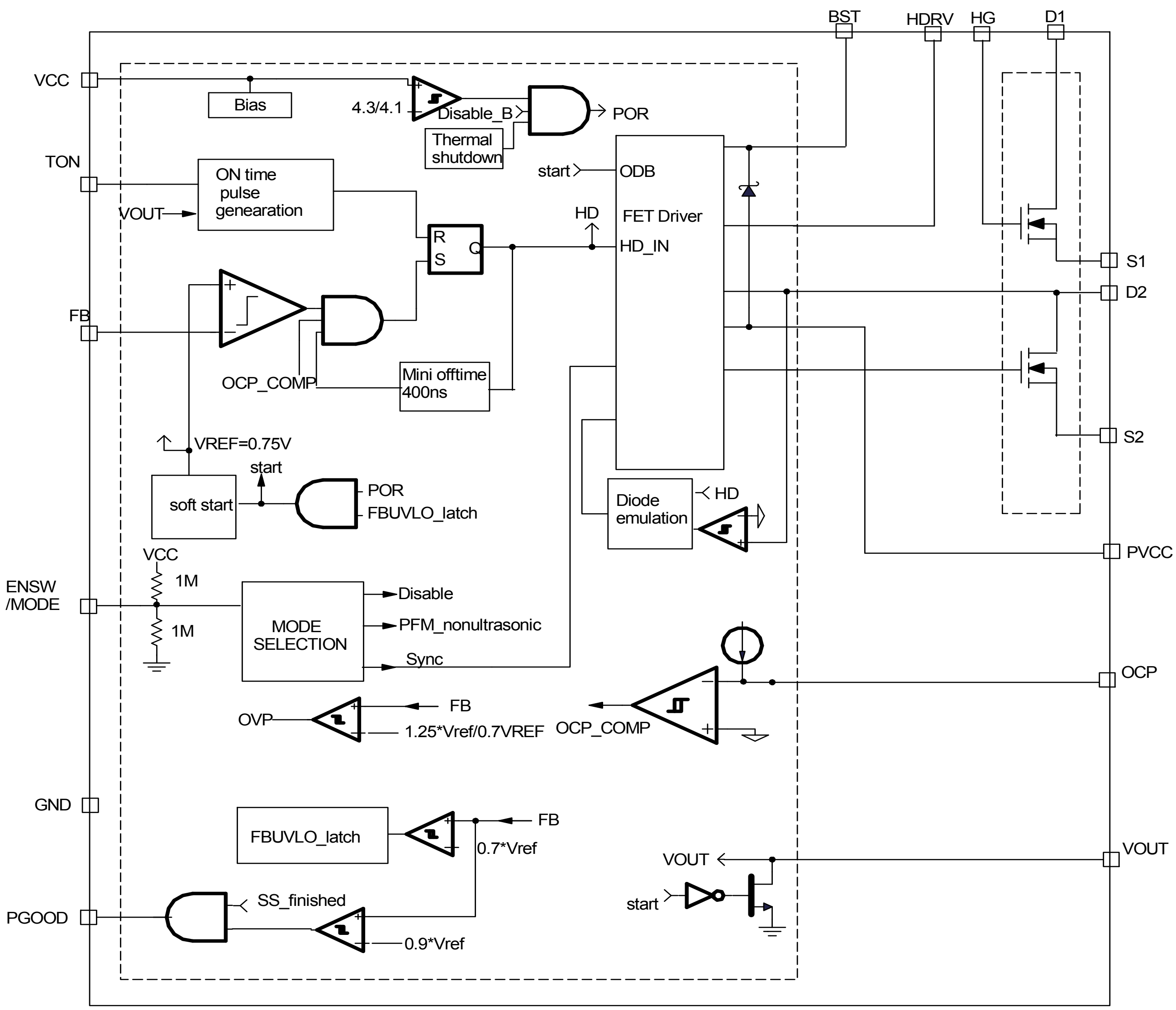

Figure 2 - Simplified block diagram of the NX9548

Demoboard design and waveforms

sdfd

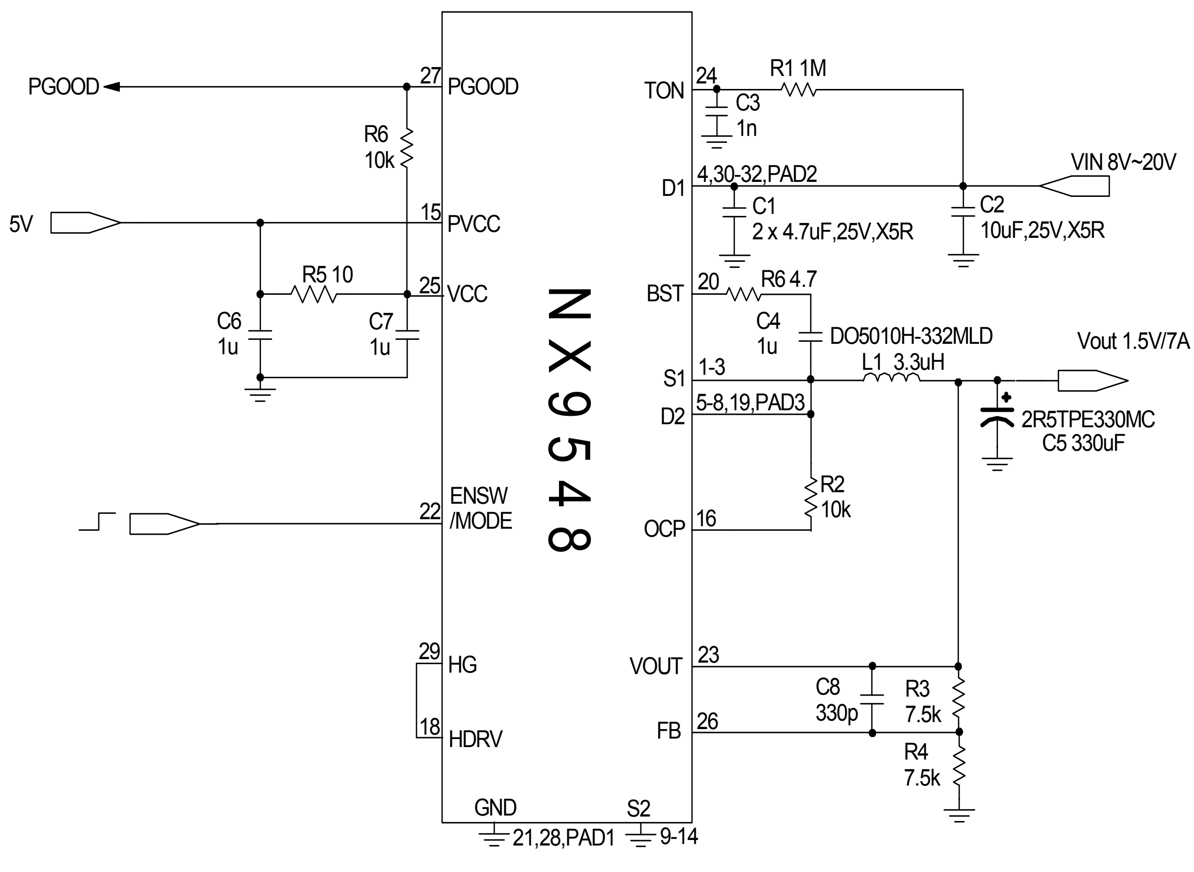

Figure 3 - Demoboard schematic of NX9548

Bill of Materials

Item	Quantity	Reference	Part	Manufacturer
1	2	C1	4.7uF,25V,X5R	
2	1	C2	10uF,25V,X5R	
3	1	C3	1nF,50V,X7R	
4	3	C4,C6,C7	1uF,10V,X7R	
5	1	C5	2R5TPE330MC	SANYO
6	1	C8	330pF	
7	1	R1	1MEG	
8	2	R2,R6	10k	
9	2	R3,R4	7.5k	
10	1	R5	10	
11	1	R6	4.7	
12	1	L1	DO5010H-332MLD	COILCRAFT
13	1	U1	NX9548	MICROSEMI

Demoboard Waveforms

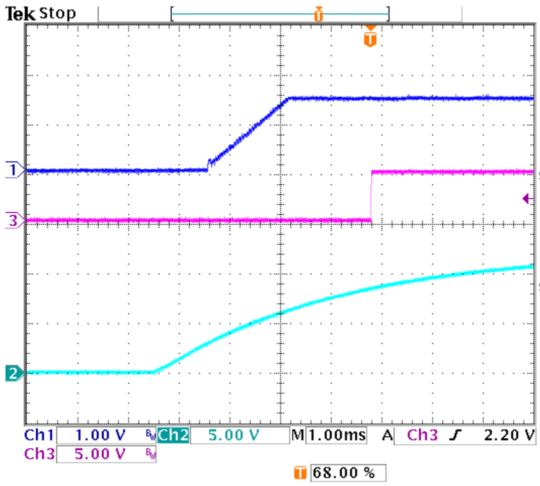

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Fig.4 Startup when 5V is present and 12V bus is started up, output load current is at 1.5A.

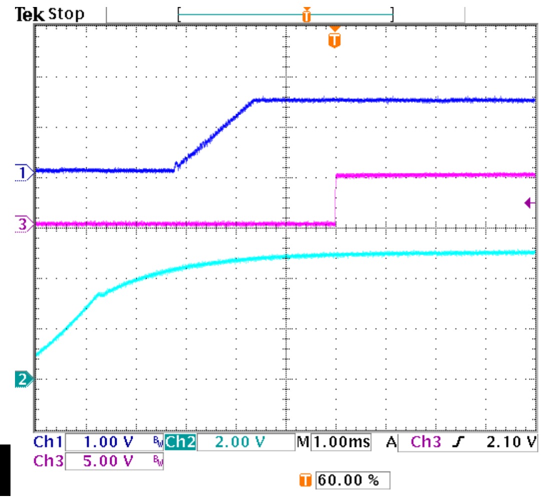

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Fig.5 Startup when 12V bus is present and 5V is started up.

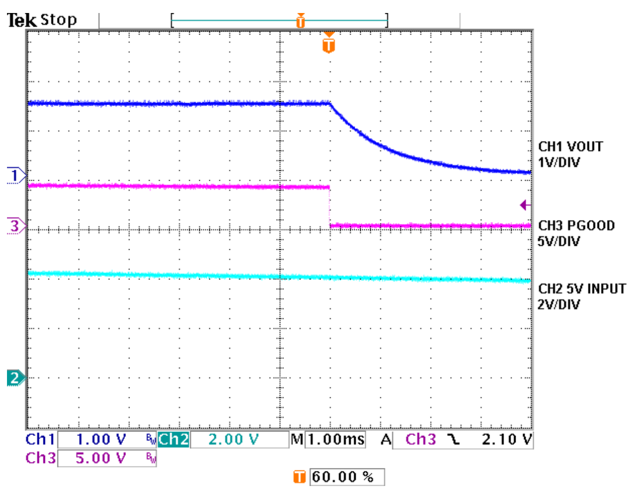

Fig.6 Shutdown when 12V bus is present and 5V is shuted down.

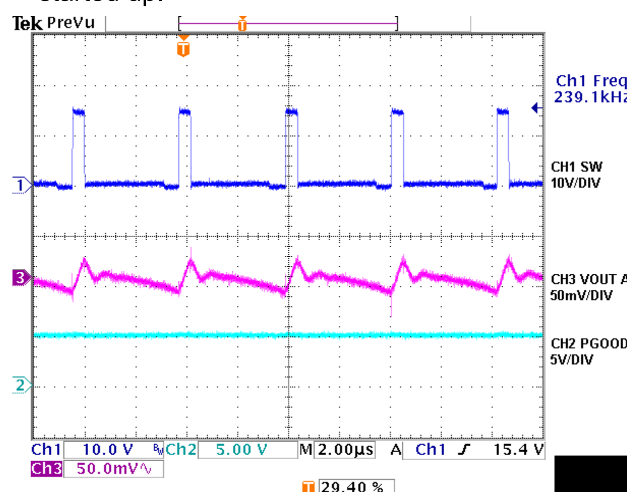

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Fig.7Output ripple (VIN=15V IOUT=1.2A)

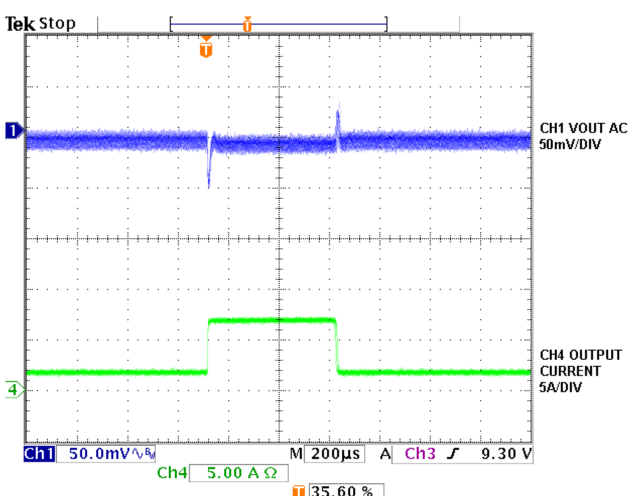

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Fig.8 5A step response(VIN=5V)

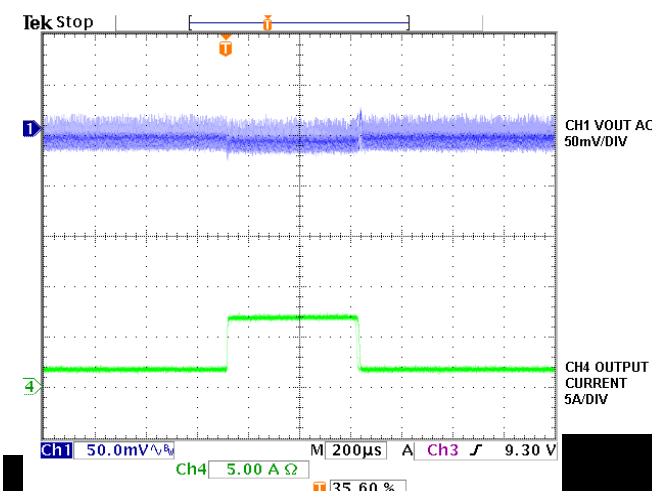

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Fig.9 5A step response(VIN=20V)

NX9548 Efficiency

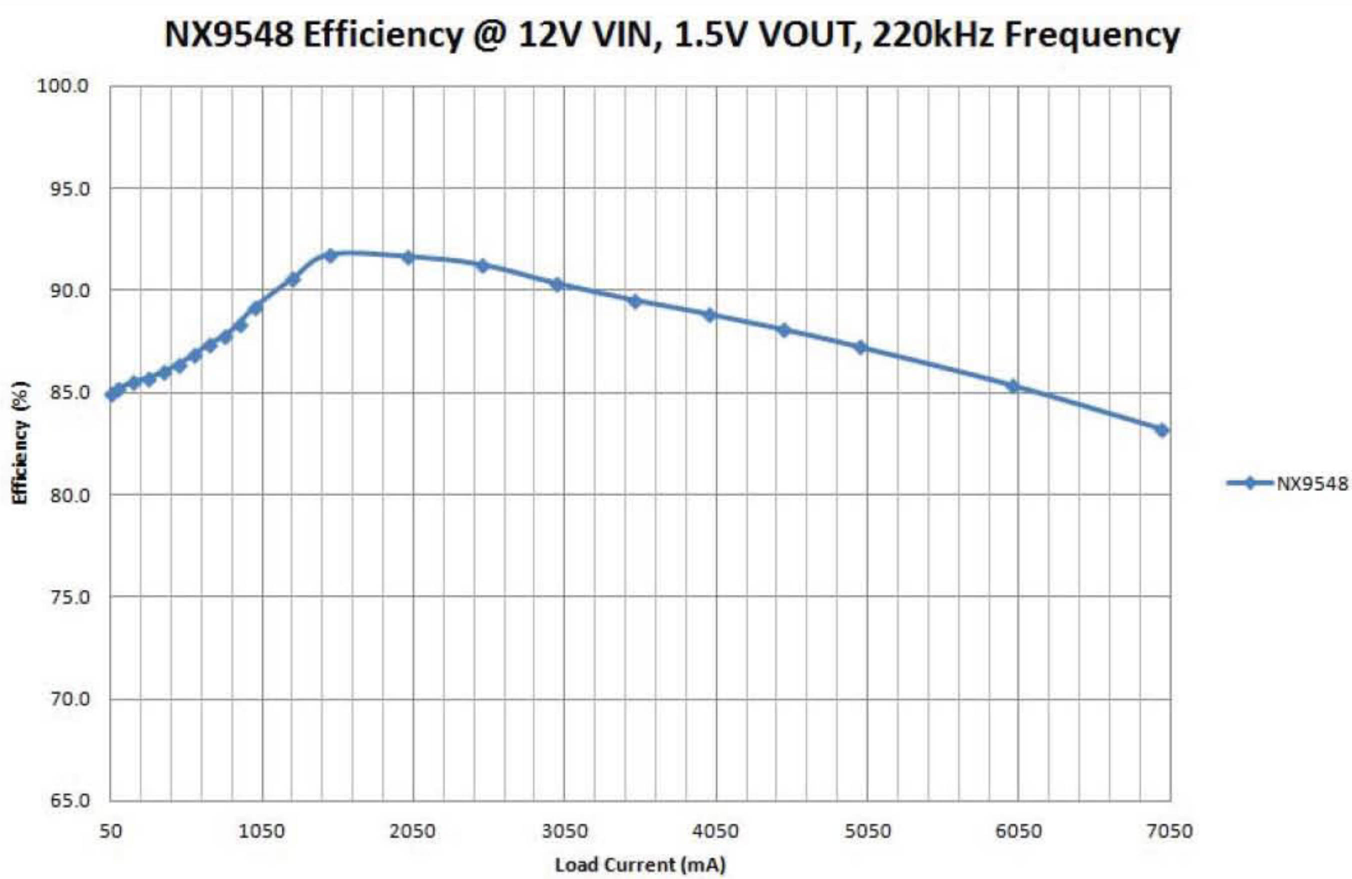

Fig.10 Output efficiency at 1.5V output voltage

VOUT	INDUCTOR
1.5V	Coilcraft DO5010P-332HC, 3.3uH

NX9548 Efficiency

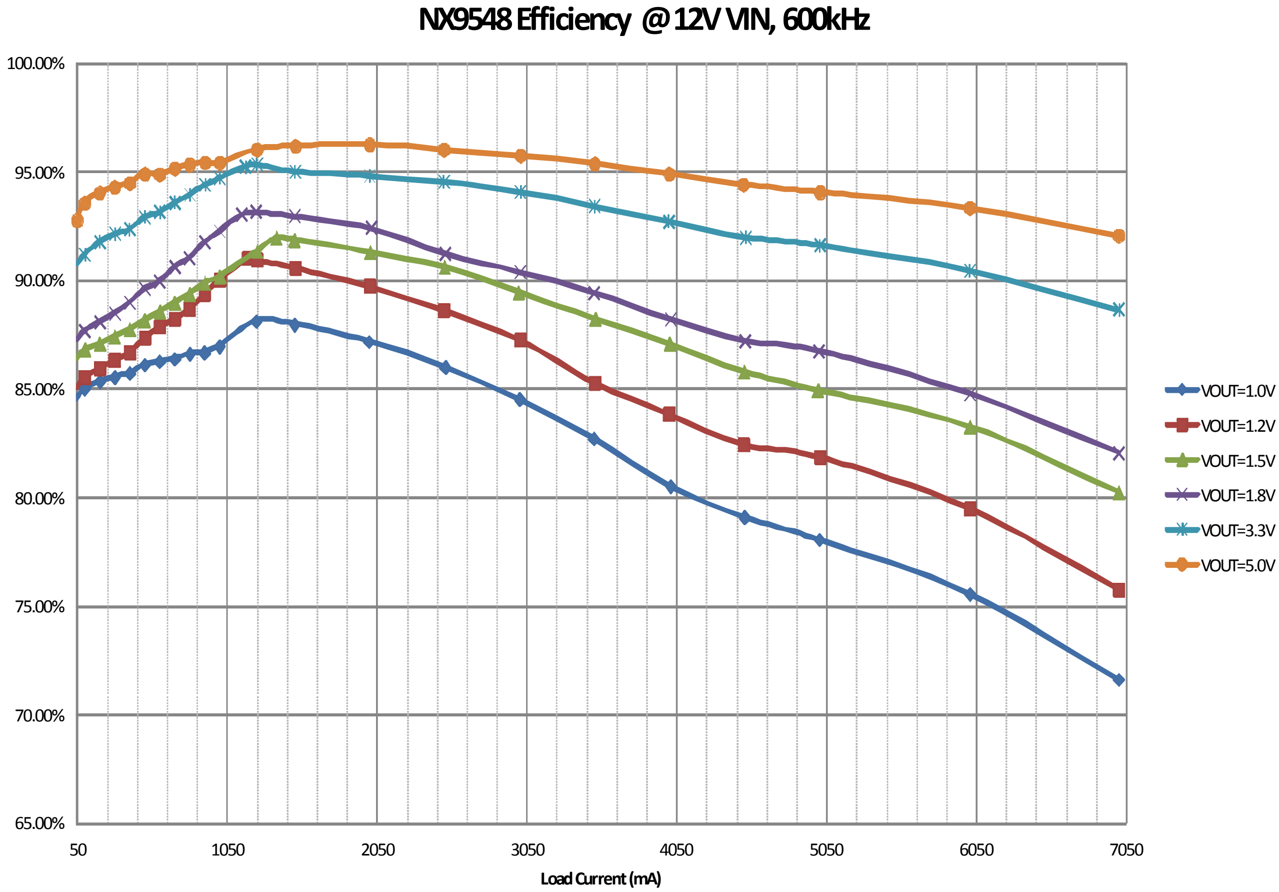

Fig.11 Output efficiency at different output voltage

Fig. 11 efficiency data uses the same schematic as Fig.3, except for R1 is adjusted to have 600kHz working frequency and inductor values specified in table below.

VOUT	INDUCTOR
1V, 1.2V, 1.5V	Coilcraft DO5010P-152HC, 1.5uH
1.8V	Coilcraft DO5010P-222HC, 2.2uH
3.3V	Coilcraft DO5010P-332HC, 3.3uH

APPLICATION INFORMATION

Symbol Used In Application Information:

V_{IN} - Input voltage
V_{OUT} - Output voltage
I_{OUT} - Output current
ΔV_{RIPPLE} - Output voltage ripple
F_S - Working frequency
ΔI_{RIPPLE} - Inductor current ripple

Design Example

The following is typical application for NX9548, the schematic is figure 1.

V_{IN} = 8 to 22V
V_{OUT}=1.5V
F_S=220kHz
I_{OUT}=7A
ΔV_{RIPPLE} <=60mV
ΔV_{DROOP}<=60mV @ 3A step

On_Time and Frequency Calculation

The constant on time control technique used in NX9548 delivers high efficiency, excellent transient dynamic response, make it a good candidate for step down notebook applications.

An internal one shot timer turns on the high side driver with an on time which is proportional to the input supply V_{IN} as well inversely proportional to the output voltage V_{OUT}. During this time, the output inductor charges the output cap increasing the output voltage by the amount equal to the output ripple. Once the timer turns off, the Hdrv turns off and cause the output voltage to decrease until reaching the internal FB voltage of 0.75V on the PFM comparato r. At this point the comparator trips causing the cycle to repeat itself. A minimum off time of 400nS is internally set.

The equation setting the On Time is as follows:

$$TON = \frac{4.45\times10^{-12}\times R_{TON}\times V_{OUT}}{V_{IN}-0.5V} \quad ...(1)$$

$$F_S = \frac{V_{OUT}}{V_{IN}\times TON} \quad ...(2)$$

In this application example, the RTON is chosen to be 1Mohm, when VIN=22V, the TON is 310nS and F_S is around 220kHz.

Output Inductor Selection

The value of inductor is decided by inductor ripple current and working frequency. Larger inductor value normally means smaller ripple current. However if the inductance is chosen too large, it brings slow response and lower efficiency. The ripple current is a design freedom which can be decided by design engineer according to various application requirements. The inductor value can be calculated by using the following equations:

$$L_{OUT} = \frac{(V_{IN}-V_{OUT})\times T_{ON}}{I_{RIPPLE}}$$
$$I_{RIPPLE} = k\times I_{OUTPUT} \quad ...(3)$$

where k is percentage of output current.

In this example, inductor from COILCRAFT DO5010H-332 with L=3.3uH is chosen.

Current Ripple is recalculated as below:

$$I_{RIPPLE} = \frac{(V_{IN}-V_{OUT})\times T_{ON}}{L_{OUT}}$$
$$= \frac{(22V-1.5V)\times310nS}{3.3uH} \quad ...(4)$$
$$=1.925A$$

Output Capacitor Selection

Output capacitor is basically decided by the amount of the output voltage ripple allowed during steady state(DC) load condition as well as specification for the load transient. The optimum design may require a couple of iterations to satisfy both conditions.

Based on DC Load Condition

The amount of voltage ripple during the DC load condition is determined by equation(5).

$$\Delta V_{RIPPLE} = ESR\times\Delta I_{RIPPLE} + \frac{\Delta I_{RIPPLE}}{8\times F_S\times C_{OUT}} \quad ...(5)$$

Where ESR is the output capacitors' equivalent series resistance, C_{OUT} is the value of output capacitors.

Typically POSCAP is recommended to use in NX9548's applications. The amount of the output voltage ripple is dominated by the first term in equation(5) and the second term can be neglected.

For this example, one POSCAP 2R5TPE330MC is chosen as output capacitor, the ESR and inductor current typically determines the output voltage ripple. When VIN reach maximum voltage, the output voltage ripple is in the worst case.

$$ESR_{desire} = \frac{\Delta V_{RIPPLE}}{\Delta I_{RIPPLE}} = \frac{30mV}{1.925A} = 15.5m\Omega \qquad ...(6)$$

If low ESR is required, for most applications, multiple capacitors in parallel are needed. The number of output capacitor can be calculate as the following:

$$N = \frac{ESR_E \times \Delta I_{RIPPLE}}{\Delta V_{RIPPLE}} \qquad ...(7)$$

$$N = \frac{12m\Omega \times 1.925A}{30mV}$$

N =0.77

The number of capacitor has to be round up to a integer. Choose N =1.

Based On Transient Requirement

Typically, the output voltage droop during transient is specified as

$\Delta V_{droop} < \Delta V_{tran}$ @step load ΔI_{STEP}

During the transient, the voltage droop during the transient is composed of two sections. One section is dependent on the ESR of capacitor, the other section is a function of the inductor, output capacitance as well as input, output voltage. For example, for the overshoot when load from high load to light load with a ΔI_{STEP} transient load, if assuming the bandwidth of system is high enough, the overshoot can be estimated as the following equation.

$$\Delta V_{overshoot} = ESR \times \Delta I_{step} + \frac{V_{OUT}}{2 \times L \times C_{OUT}} \times \tau^2 \qquad ...(8)$$

where τ is the a function of capacitor,etc.

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \frac{L \times \Delta I_{step}}{V_{OUT}} - ESR \times C_{OUT} & \text{if} \quad L \ge L_{crit} \end{cases} \qquad ...(9$$

where

$$L_{crit} = \frac{ESR \times C_{OUT} \times V_{OUT}}{\Delta I_{step}} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} \qquad ...(10)$$

where ESR_E and C_E represents ESR and capacitance of each capacitor if multiple capacitors are used in parallel.

The above equation shows that if the selected output inductor is smaller than the critical inductance, the voltage droop or overshoot is only dependent on the ESR of output capacitor. For low frequency capacitor such as electrolytic capacito r, the product of ESR and capacitance is high and $L \le L_{crit}$ is true. In that case, the transient spec is mostly like to dependent on the ESR of capacitor.

Most case, the output capacitor is multiple capacitor in parallel. The number of capacitor can be calculated by the following

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2 \qquad ...(11)$$

where

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \frac{L \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E & \text{if} \quad L \ge L_{crit} \end{cases} \qquad ...(12)$$

For example, assume voltage droop during transient is 60mV for 3A load step.

If one POSCAP 2R5TPE330MC(330uF, 12mohm ESR) is used, the crticial inductance is given as

$$L_{crit} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} =$$

$$\frac{12m\Omega \times 3300\mu F \times 1.8V}{3A} = 23.76\mu H$$

The selected inductor is 3.3uH which is smaller than critical inductance. In that case, the output voltage transient mainly dependent on the ESR.

number of capacitor is

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}}$$

$$= \frac{12m\Omega \times 4.5A}{60mV}$$

$$= 0.9$$

Choose N=1.

Based On Stability Requirement

ESR of the output capacitor can not be chosen too low which will cause system unstable. The zero caused by output capacitor's ESR must satisfy the requirement as below:

$$F_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \le \frac{F_{SW}}{4} \quad ...(13)$$

Besides that, ESR has to be bigger enough so that the output voltage ripple can provide enough voltage ramp to error amplifier through FB pin. If ESR is too small, the error amplifier can not correctly dectect the ramp, high side MOSFET will be only turned off for minimum time 400nS. Double pulsing and bigger output ripple will be observed. In summary, the ESR of output capacitor has to be big enough to make the system stable, but also has to be small enough to satify the transient and DC ripple requirements.

Input Capacitor Selection

Input capacitors are usually a mix of high frequency ceramic capacitors and bulk capacitors. Ceramic capacitors bypass the high frequency noise, and bulk capacitors supply switching current to the MOSFETs. Usually 1uF ceramic capacitor is chosen to decouple the high frequency noise.The bulk input capacitors are decided by voltage rating and RMS current rating. The RMS current in the input capacitors can be calculated as:

$$I_{RMS} = I_{OUT} \times \sqrt{D} \times \sqrt{1-D}$$
$$D = T_{ON} \times F_S \quad ...(14)$$

When V_{IN} = 22V, V_{OUT}=1.5V, I_{OUT}=7A, the result of input RMS current is 1.8A.

For higher efficiency, low ESR capacitors are recommended. One 10uF/X5R/25V and two 4.7uF/X5R /25V ceramic capacitors are chosen as input capacitors.

Output Voltage Calculation

Output voltage is set by reference voltage and external voltage divider. The reference voltage is fixed at 0.75V. The divider consists of two ratioed resistors so that the output voltage applied at the Fb pin is 0.75V when the output voltage is at the desired value.

The following equation applies to figure 12, which shows the relationship between V_{OUT}, V_{REF} and voltage divider.

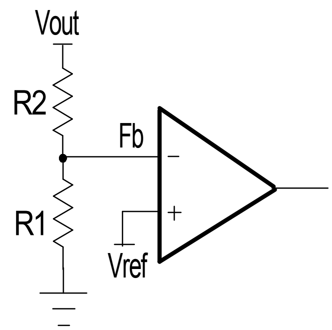

Figure 12 - Voltage Divider

$$R_1 = \frac{R_2 \times V_{REF}}{V_{OUT} - V_{REF}} \quad ...(15)$$

where R_2 is part of the compensator, and the value of R_1 value can be set by voltage divider.

Mode Selection

NX9548 can be operated in PFM mode, ultrasonic PFM mode, CCM mode and shutdown mode by applying different voltage on ENSW/MODE pin.

When VCC applied to ENSW/MODE pin, NX9548 is In PFM mode. The low side MOSFET emulates the function of diode when discontinuous continuous mode happens, often in light load condition. During that time, the inductor current crosses the zero ampere border and becomes negative current. When the inductor current reaches negative territor y, the low side MOSFET is turned off and it takes longer time for the output voltage to drop, the high side MOSFET waits longer to be turned on. At the same time, no matter light load and heavy load, the on time of high side MOSFET keeps the same. Therefore the lightier load, the lower the switching frequency will be. In ultrosonic PFM mode, the lowest frequency is set to be 25kHz to avoid audio frequency modulation. This kind of reduction of frequency keeps the system running at light light with high efficiency.

In CCM mode, inductor current zero-crossing sensing is disabled, low side MOSFET keeps on even when inductor current becomes negative. In this way the efficiency is lower compared with PFM mode at light load, but frequency will be kept constant.

Over Current Protection

Over current protection for NX9548 is achieved by sensing current through the low side MOSFET. An typical internal current source of 24uA flows through an external resistor connected from OCSET pin to SW node sets the over current protection threshold. When synchronous FET is on, the voltage at node SW is given as

$V_{SW} = -I_L \times R_{DSON}$

The voltage at pin OCSET is given as

$I_{OCP} \times R_{OCP} + V_{SW}$

When the voltage is below zero, the over current occurs as shown in figure below.

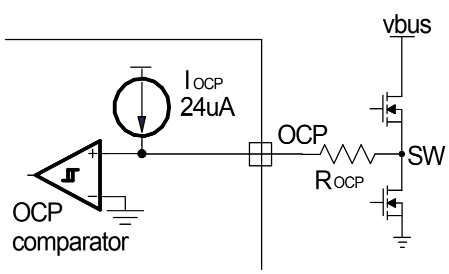

Figure 13 - Over Voltage Protection

The over current limit can be set by the following equation.

$I_{SET} = I_{OCP} \times R_{OCP} / R_{DSON}$

The low side MOSFET R_{DSON} is 24mΩ at the OCP occuring moment, and the current limit is set at 10A, then

$$R_{OCP} = \frac{I_{SET} \times R_{DSON}}{I_{OCP}} = \frac{10A \times 24m\Omega}{24uA} = 10k\Omega$$

Choose R_{OCP}=10kΩ

Power Good Output

Power good output is open drain output, a pull up resistor is needed. Typically when softstart is finised and FB pin voltage is over 90% of V_{REF}, the PGOOD pin is pulled to high after a 1.6ms delay.

Over Output Voltage Protection

Typically when the FB pin voltage is over 125% of V_{REF}, the high side MOSFET will be turned off and the low side MOSFET will be latched to be on to discharge the output voltage. To resume the switching operation, reset VCC or EN is necessary.

Under Output Voltage Protection

Typically when the FB pin voltage is under 70% of V_{REF}, the high side and low side MOSFET will be turned off. To resume the switching operation, VCC or ENSW has to be reset.

Demoboard Schematic

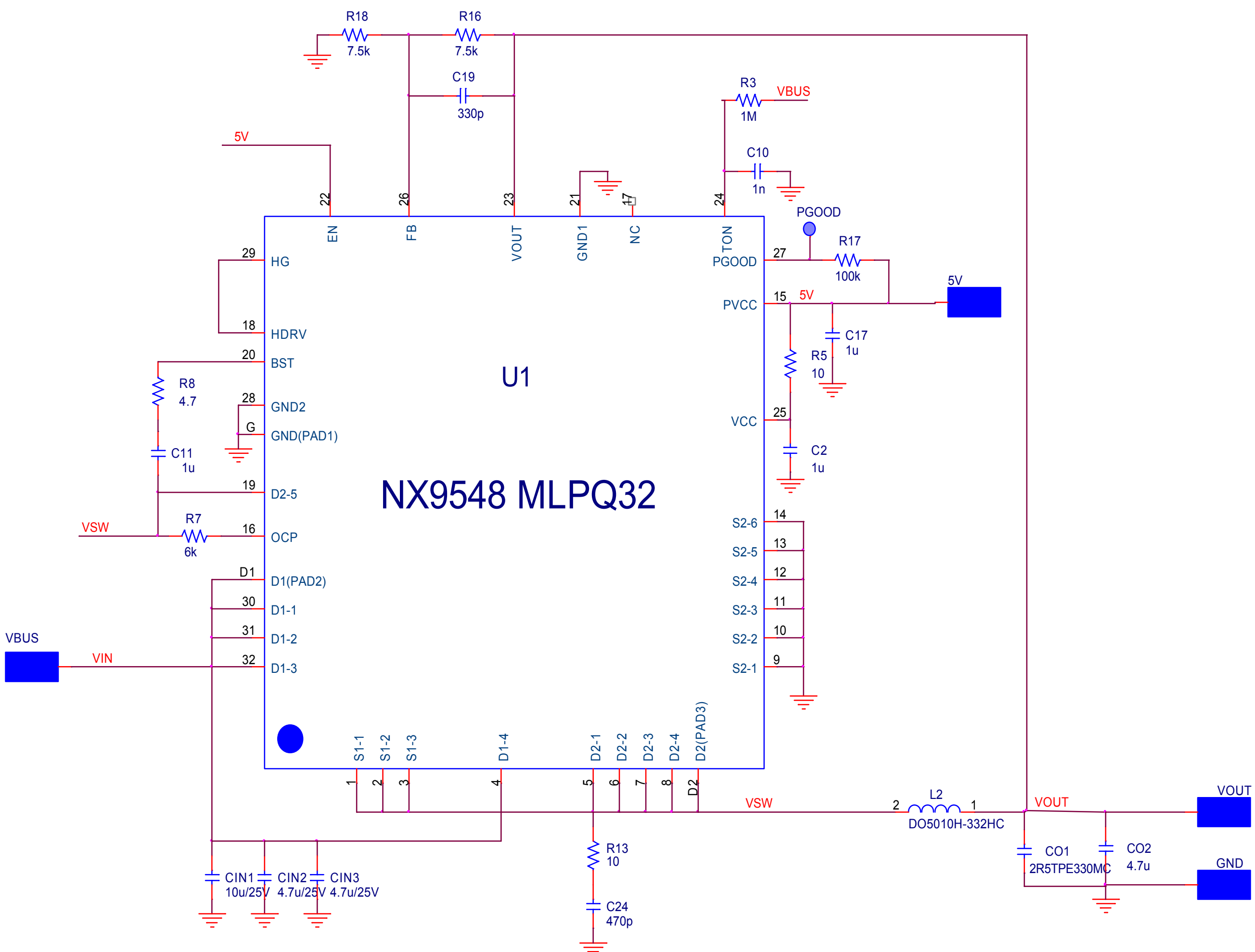

Figure 14 - NX9548 schematic for the demoboard layout

Demoboard Layout

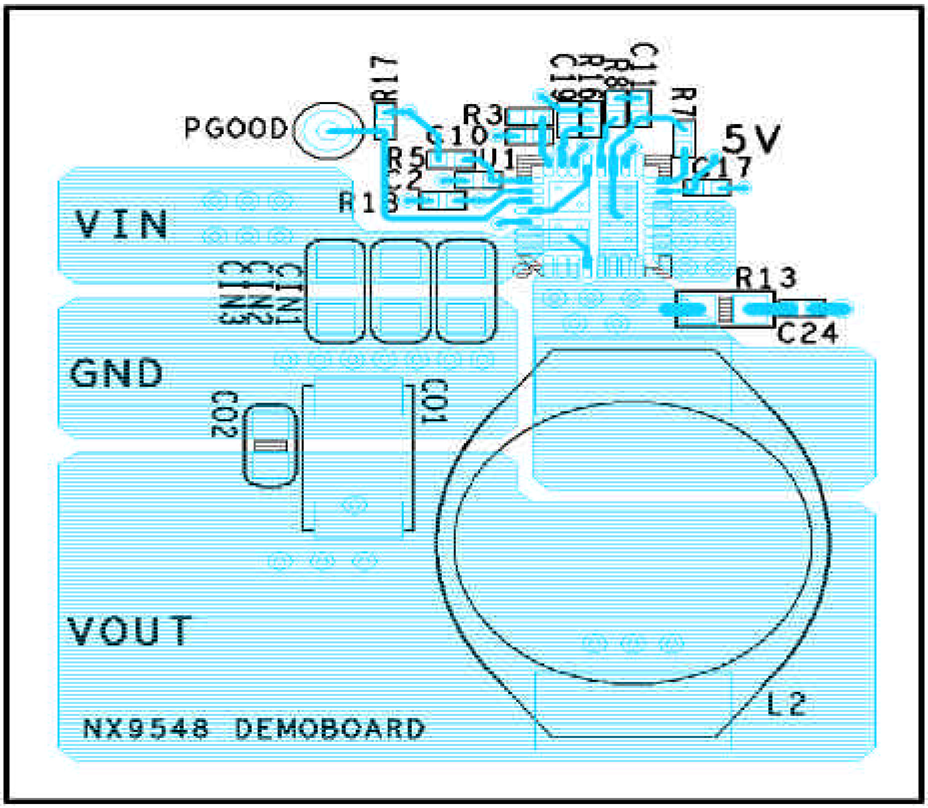

Figure 15 Top layer

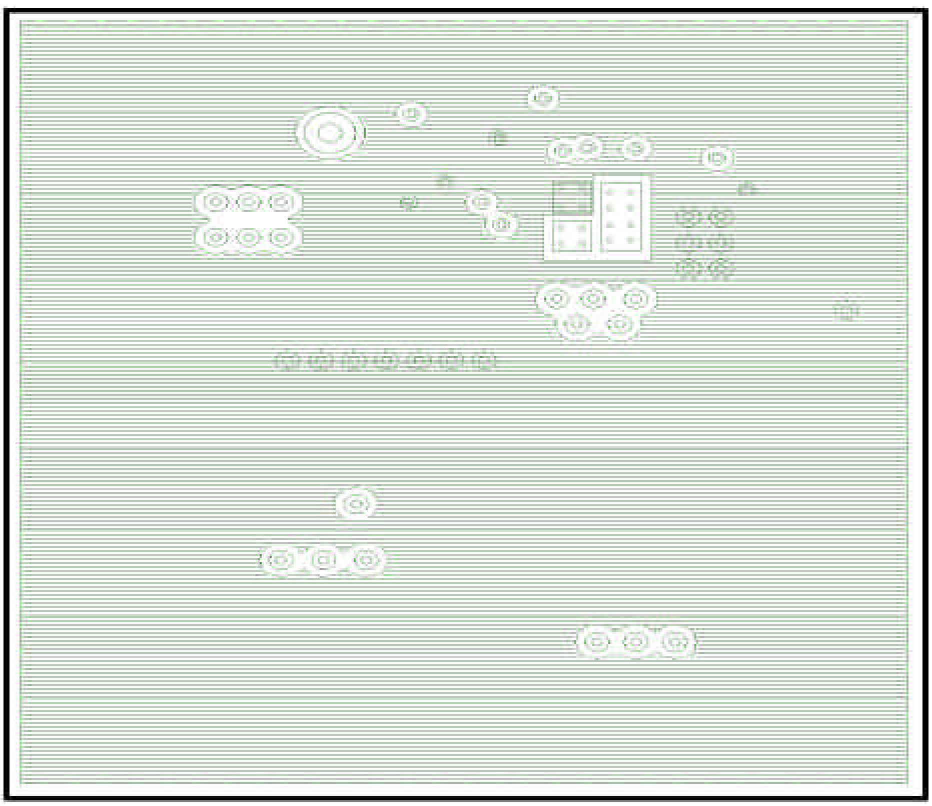

Figure 16 Ground layer

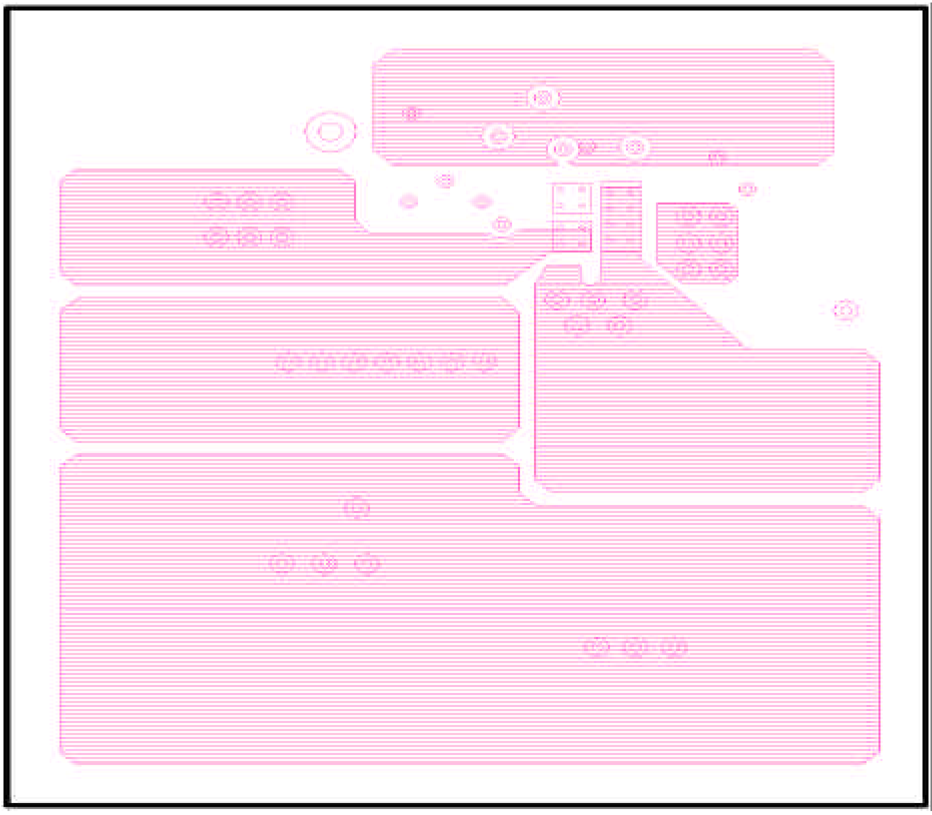

Figure 17 Power layer

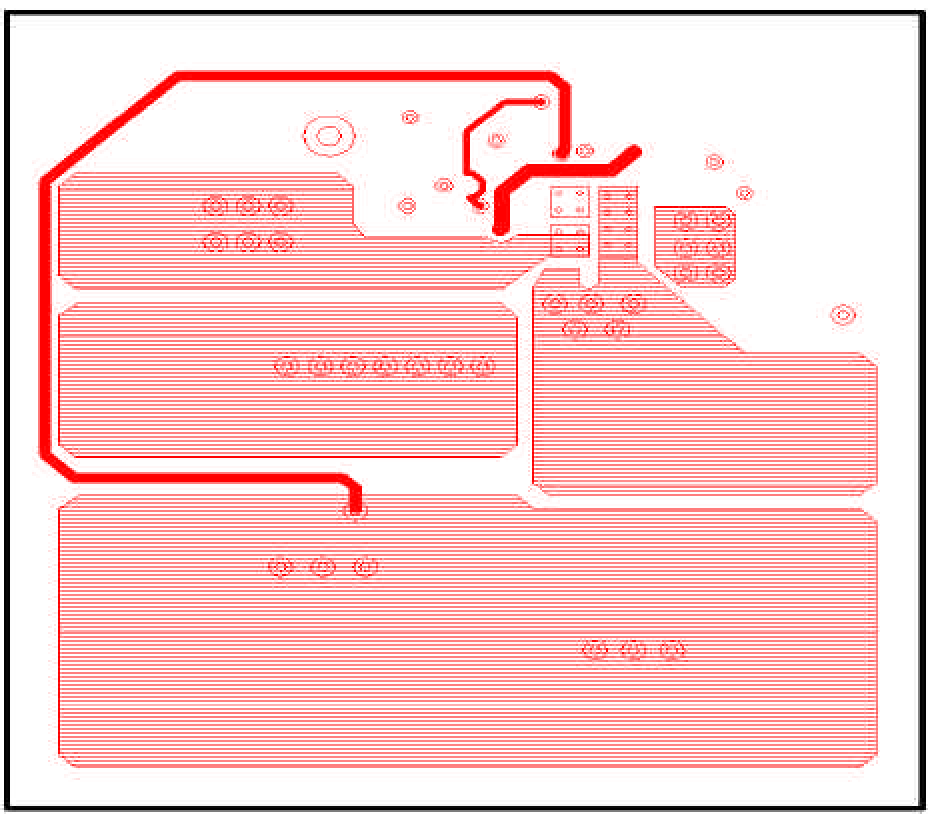

Figure 18 Bottom layer

Microsemi
Analog Mixed Signal Group
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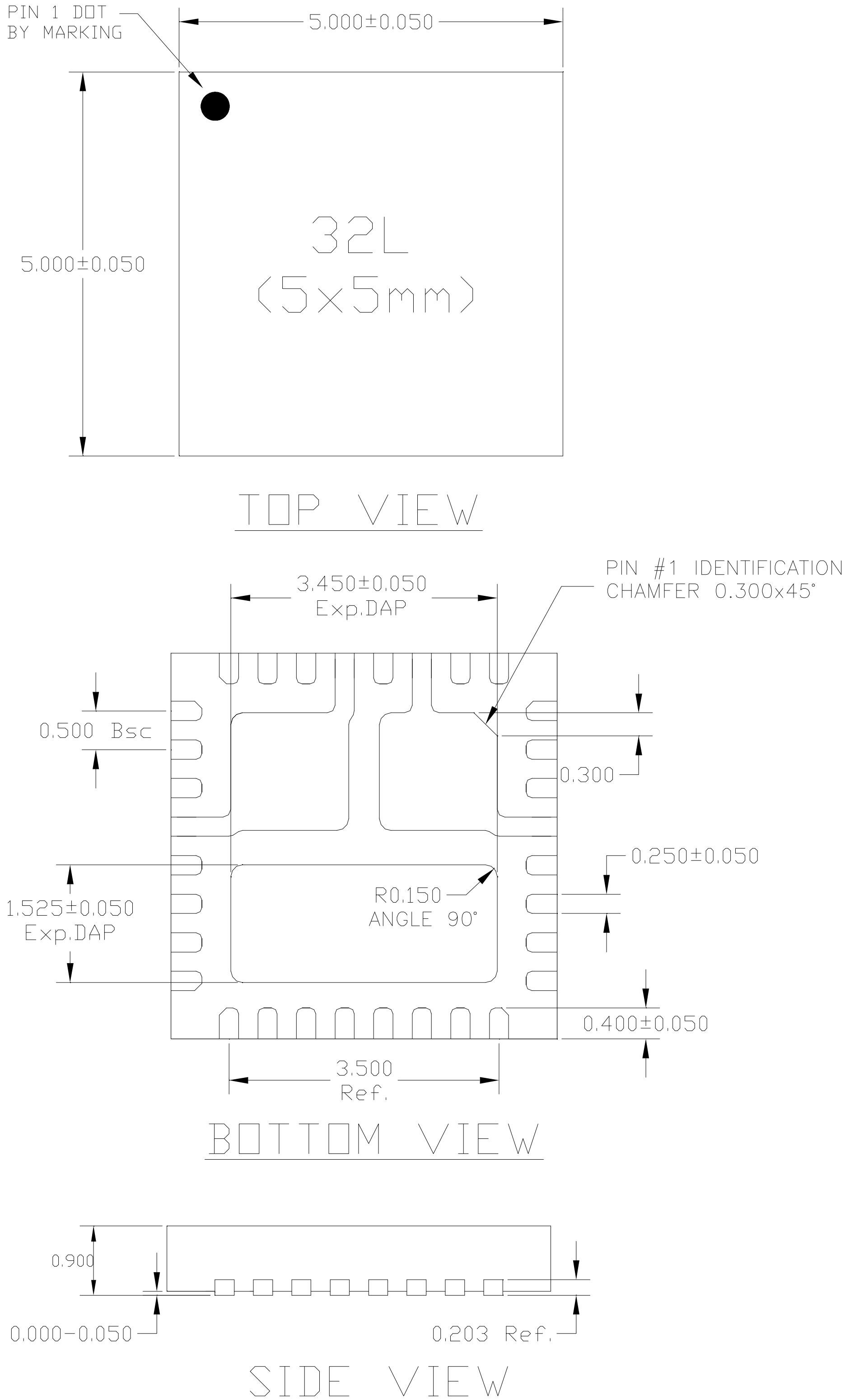
MCM 32 PIN 5 x 5 PACKAGE OUTLINE DIMENSIONS



NOTE: ALL DIMENSIONS ARE DISPLAYED IN MILLIMETERS.