

TSM7N90 Taiwan Semiconductor

ALOGEN

N-Channel Power MOSFET

 $900V,\,7A,\,1.9\Omega$

FEATURES

- Low RDS(on) 1.9Ω (Max.)
- Low gate charge typical @49nC (Typ.)
- Improve dV/dt capability
- Pb-free plating
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEE 2002/96/EC

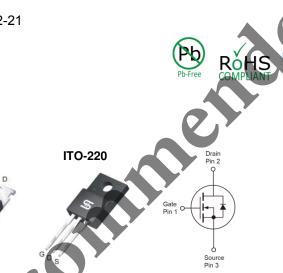
TO-220

Halogen-free according to IEC 61249-2-21
definition

APPLICATION

- Power Supply
- Lighting

KEY PERFORMANCE PARAMETERSPARAMETERVALUEUNIT V_{DS} 900V $R_{DS(on)}$ (max)1.9 Ω Q_g 49nC



ABSOLUTE MAXIMUM RATINGS (T _A = 25°C unless otherwise noted)							
PARAMETER		SYMBOL	TO-220	ITO-220	UNIT		
Drain-Source Voltage		V _{DS}	900		V		
Gate-Source Voltage		V_{GS}	±30		V		
Continuous Drain Current (Note 1)	T _C = 25°C	l _D	7		А		
	T _C = 100°C		4.31		А		
Pulsed Drain Current (Note 2)		I _{DM}	28		А		
Total Power Dissipation @ $T_c = 25^{\circ}C$		P _{DTOT}	250	40.3	W		
Single Pulsed Avalanche Energy (Note 3)		E _{AS}	106		mJ		
Single Pulsed Avalanche Current (Note 3)		I _{AS}	7		А		
Operating Junction and Storage Temperature Range		T_J, T_STG	- 55 to +150		°C		

THERMAL PERFORMANCE				
PARAMETER	SYMBOL	TO-220	ITO-220	UNIT
Junction to Case Thermal Resistance	R _{ejc}	0.5	3.1	°C/W
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	62.5		°C/W

Notes: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB with minimum recommended footprint in still air.



TSM7N90

Taiwan Semiconductor

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 4)	•	L			1	
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250 \mu A$	BV _{DSS}	900			V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	V _{GS(TH)}	2		4	V
Gate Body Leakage	$V_{GS} = \pm 30V, V_{DS} = 0V$	I _{GSS}			±100	nA
Zero Gate Voltage Drain Current	V _{DS} = 900V, V _{GS} = 0V	I _{DSS}			10	μA
Drain-Source On-State Resistance	V_{GS} = 10V, I_{D} = 3.5A	R _{DS(on)}		1.52	1.9	Ω
Dynamic (Note 5)						
Total Gate Charge		Qg		49		nC
Gate-Source Charge	$V_{DS} = 720V, I_D = 7A,$	Q _{gs}	/	7		
Gate-Drain Charge	V _{GS} = 10V	Q _{gd}		20		
Input Capacitance		C _{iss}		1969		pF
Output Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz	C _{oss}		133		
Reverse Transfer Capacitance		Crss		11		
Switching (Note 6)						
Turn-On Delay Time	$V_{DD} = 380V,$ $R_{GEN} = 25\Omega,$ $I_D = 10A, V_{GS} = 10V,$	t _{d(on)}		39		ns
Turn-On Rise Time		t _r		38		
Turn-Off Delay Time		t _{d(off)}		155		
Turn-Off Fall Time		t _f		45		
Source-Drain Diode (Note 4)						
Forward On Voltage	I _S = 10A, V _{GS} = 0V	V _{SD}			1.4	V
Reverse Recovery Time	I _S = 7A,	t _{rr}		464		ns
Reverse Recovery Charge	dl _F /dt = 100A/µs	Q _{rr}		4.7		μC

1. Current limited by package.

2.

Pulse width limited by the maximum junction temperature. L = 4.1mH, I_{AS} = 7A, V_{DD} = 50V, R_G = 25 Ω , Starting T_J = 25°C 100% Eas Test Condition: L = 1mH, I_{AS} = 3.5A, V_{DD} = 50V, R_G = 25 Ω , Starting T_J = 25°C 3.

4. Pulse test: $PW \le 300\mu s$, duty cycle $\le 2\%$.

For DESIGN AID ONLY, not subject to production testing. 5.

Switching time is essentially independent of operating temperature. 6.

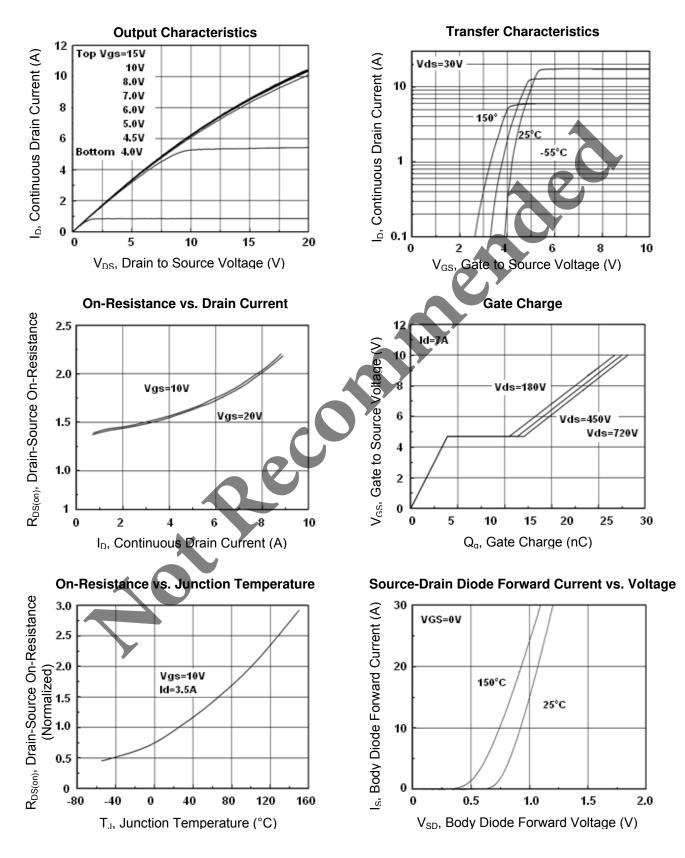


ORDERING INFORMATION



CHARACTERISTICS CURVES

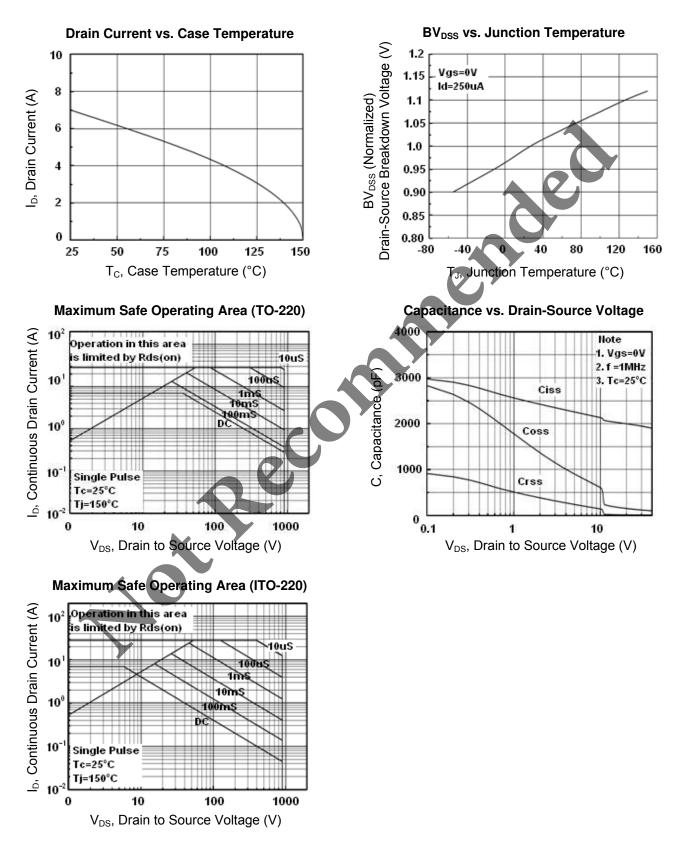
(T_C = 25°C unless otherwise noted)





CHARACTERISTICS CURVES

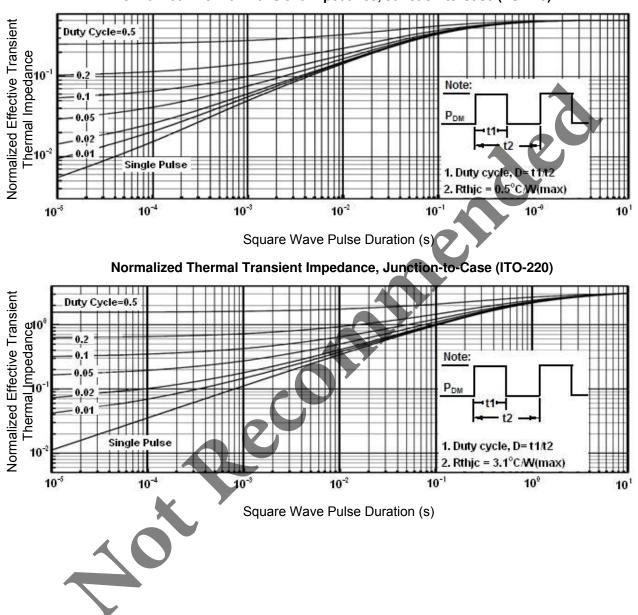
(T_c = 25° C unless otherwise noted)





CHARACTERISTICS CURVES

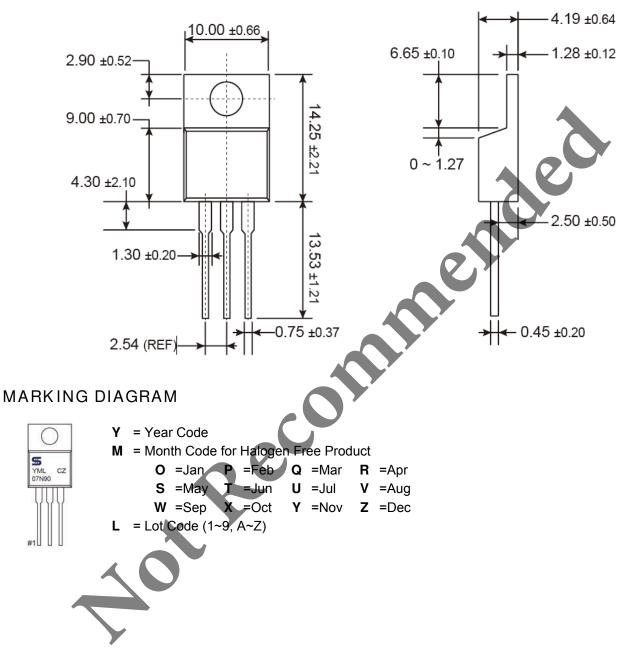
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Normalized Thermal Transient Impedance, Junction-to-Case (TO-220)



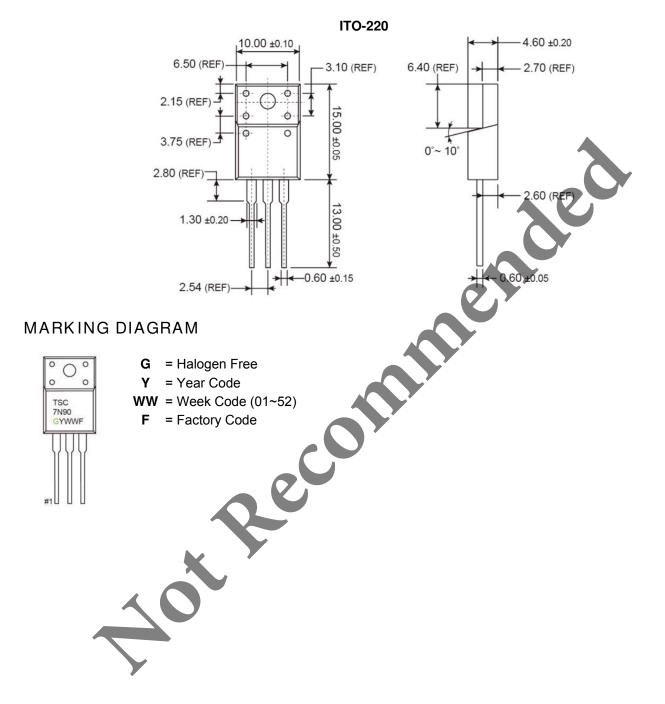
PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



TO-220



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)







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