

NCV8405A, NCV8405B

Self-Protected Low Side Driver with Temperature and Current Limit

NCV8405A/B is a three terminal protected Low-Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain-to-Gate clamping for overvoltage protection. This device is suitable for harsh automotive environments.

Features

- Short-Circuit Protection
- Thermal Shutdown with Automatic Restart
- Overvoltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

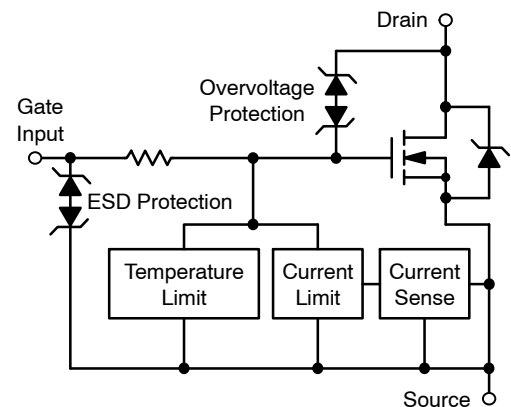


ON Semiconductor®

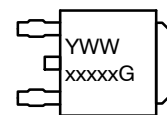
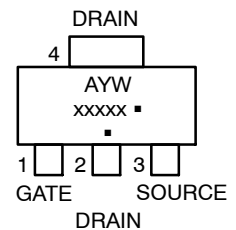
www.onsemi.com

| $V_{(BR)DSS}$ (Clamped) | $R_{DS(ON)}$ TYP | I_D MAX |
|----------------------------|------------------|-----------|
| 42 V | 90 mΩ @ 10 V | 6.0 A* |

*Max current limit value is dependent on input condition.



MARKING DIAGRAM



A = Assembly Location

Y = Year

W, WW = Work Week

xxxxx = 8405A or 8405B

G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

NCV8405A, NCV8405B

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|--|--------------------|------|
| Drain-to-Source Voltage Internally Clamped | V _{DSS} | 42 | V |
| Drain-to-Gate Voltage Internally Clamped (R _G = 1.0 MΩ) | V _{DGR} | 42 | V |
| Gate-to-Source Voltage | V _{GS} | ± 14 | V |
| Continuous Drain Current | I _D | Internally Limited | |
| Power Dissipation – SOT-223 Version @ T _A = 25°C (Note 1) @ T _A = 25°C (Note 2) @ T _S = 25°C | P _D | 1.0 | W |
| Power Dissipation – DPAK Version @ T _A = 25°C (Note 1) @ T _A = 25°C (Note 2) @ T _S = 25°C | | 11.4 | |
| Thermal Resistance – SOT-223 Version Junction-to-Ambient Steady State (Note 1) Junction-to-Ambient Steady State (Note 2) Junction-to-Soldering Point Steady State | R _{θJA} R _{θJA} R _{θJS} | 130 72 11 | °C/W |
| Thermal Resistance – DPAK Version Junction-to-Ambient Steady State (Note 1) Junction-to-Ambient Steady State (Note 2) Junction-to-Soldering Point Steady State | R _{θJA} R _{θJA} R _{θJS} | 60 50 3.0 | |
| Single Pulse Drain-to-Source Avalanche Energy (V _{DD} = 40 V, V _G = 5.0 V, I _{PK} = 2.8 A, L = 80 mH, R _{G(ext)} = 25 Ω, T _J = 25°C) | E _{AS} | 275 | mJ |
| Load Dump Voltage V _{LD} = V _A + V _S (V _{GS} = 0 and 10 V, R _I = 2.0 Ω, R _L = 6.0 Ω, t _d = 400 ms) | V _{LD} | 53 | V |
| Operating Junction Temperature | T _J | -40 to 150 | °C |
| Storage Temperature | T _{stg} | -55 to 150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Surface-mounted onto min pad FR4 PCB, (2 oz. Cu, 0.06" thick).
- Surface-mounted onto 2" sq. FR4 board (1" sq., 1 oz. Cu, 0.06" thick).

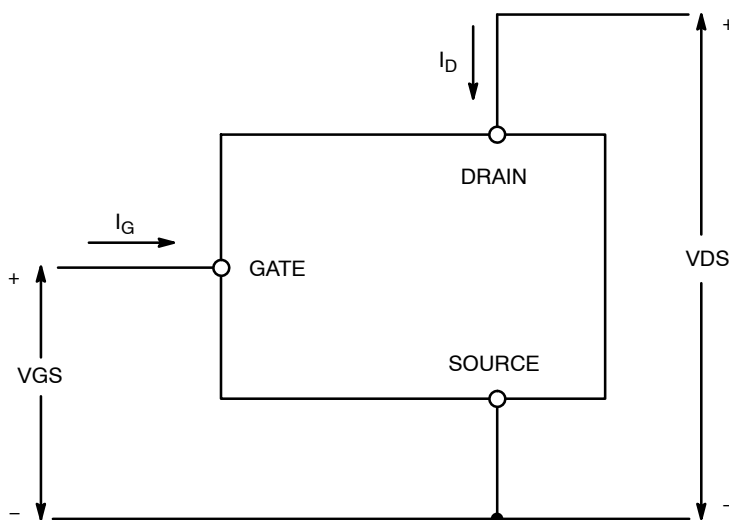


Figure 1. Voltage and Current Convention

NCV8405A, NCV8405B

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

| Parameter | Test Condition | Symbol | Min | Typ | Max | Unit |
|--|--|----------------------|-----|-----|-----|------|
| OFF CHARACTERISTICS | | | | | | |
| Drain-to-Source Breakdown Voltage (Note 3) | V _{GS} = 0 V, I _D = 10 mA, T _J = 25°C | V _{(BR)DSS} | 42 | 46 | 51 | V |
| | V _{GS} = 0 V, I _D = 10 mA, T _J = 150°C (Note 5) | | 42 | 45 | 51 | |
| Zero Gate Voltage Drain Current | V _{GS} = 0 V, V _{DS} = 32 V, T _J = 25°C | I _{DSS} | | 0.5 | 2.0 | μA |
| | V _{GS} = 0 V, V _{DS} = 32 V, T _J = 150°C (Note 5) | | | 2.0 | 10 | |
| Gate Input Current | V _{DS} = 0 V, V _{GS} = 5.0 V | I _{GSSF} | | 50 | 100 | μA |

ON CHARACTERISTICS (Note 3)

| | | | | | | |
|--|--|-------------------------------------|-----|------|-----|--------|
| Gate Threshold Voltage | V _{GS} = V _{DS} , I _D = 150 μA | V _{GS(th)} | 1.0 | 1.6 | 2.0 | V |
| Gate Threshold Temperature Coefficient | | V _{GS(th)} /T _J | | 4.0 | | -mV/°C |
| Static Drain-to-Source On-Resistance | V _{GS} = 10 V, I _D = 1.4 A, T _J = 25°C | R _{DS(on)} | | 90 | 100 | mΩ |
| | V _{GS} = 10 V, I _D = 1.4 A, T _J = 150°C (Note 5) | | | 165 | 190 | |
| | V _{GS} = 5.0 V, I _D = 1.4 A, T _J = 25°C | | | 105 | 120 | |
| | V _{GS} = 5.0 V, I _D = 1.4 A, T _J = 150°C (Note 5) | | | 185 | 210 | |
| | V _{GS} = 5.0 V, I _D = 0.5 A, T _J = 25°C | | | 105 | 120 | |
| | V _{GS} = 5.0 V, I _D = 0.5 A, T _J = 150°C (Note 5) | | | 185 | 210 | |
| Source-Drain Forward On Voltage | V _{GS} = 0 V, I _S = 7.0 A | V _{SD} | | 1.05 | | V |

SWITCHING CHARACTERISTICS (Note 5)

| | | | | | | |
|---|--|-------------------------------------|--|-----|--|------|
| Turn-ON Time (10% V _{IN} to 90% I _D) | V _{GS} = 10 V, V _{DD} = 12 V I _D = 2.5 A, R _L = 4.7 Ω | t _{ON} | | 20 | | μs |
| Turn-OFF Time (90% V _{IN} to 10% I _D) | | t _{OFF} | | 110 | | |
| Slew-Rate ON (70% V _{DS} to 50% V _{DS}) | V _{GS} = 10 V, V _{DD} = 12 V, R _L = 4.7 Ω | -dV _{DS} /dt _{ON} | | 1.0 | | V/μs |
| Slew-Rate OFF (50% V _{DS} to 70% V _{DS}) | | dV _{DS} /dt _{OFF} | | 0.4 | | |

SELF PROTECTION CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Note 4)

| | | | | | | |
|------------------------------|--|-----------------------|-----|------|-----|----|
| Current Limit | V _{DS} = 10 V, V _{GS} = 5.0 V, T _J = 25°C | I _{LIM} | 6.0 | 9.0 | 11 | A |
| | V _{DS} = 10 V, V _{GS} = 5.0 V, T _J = 150°C (Note 5) | | 3.0 | 5.0 | 8.0 | |
| | V _{DS} = 10 V, V _{GS} = 10 V, T _J = 25°C | | 7.0 | 10.5 | 13 | |
| | V _{DS} = 10 V, V _{GS} = 10 V, T _J = 150°C (Note 5) | | 4.0 | 7.5 | 10 | |
| Temperature Limit (Turn-off) | V _{GS} = 5.0 V (Note 5) | T _{LIM(off)} | 150 | 180 | 200 | °C |
| Thermal Hysteresis | V _{GS} = 5.0 V | ΔT _{LIM(on)} | | 15 | | |
| Temperature Limit (Turn-off) | V _{GS} = 10 V (Note 5) | T _{LIM(off)} | 150 | 165 | 185 | |
| Thermal Hysteresis | V _{GS} = 10 V | ΔT _{LIM(on)} | | 15 | | |

GATE INPUT CHARACTERISTICS (Note 5)

| | | | | | | |
|--|--|------------------|--|------|--|----|
| Device ON Gate Input Current | V _{GS} = 5 V, I _D = 1.0 A | I _{GON} | | 50 | | μA |
| | V _{GS} = 10 V, I _D = 1.0 A | | | 400 | | |
| Current Limit Gate Input Current | V _{GS} = 5 V, V _{DS} = 10 V | I _{GCL} | | 0.05 | | mA |
| | V _{GS} = 10 V, V _{DS} = 10 V | | | 0.4 | | |
| Thermal Limit Fault Gate Input Current | V _{GS} = 5 V, V _{DS} = 10 V | I _{GTL} | | 0.22 | | mA |
| | V _{GS} = 10 V, V _{DS} = 10 V | | | 1.0 | | |

ESD ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Note 5)

| | | | | | | |
|-------------------------------------|------------------------|-----|------|--|--|---|
| Electro-Static Discharge Capability | Human Body Model (HBM) | ESD | 4000 | | | V |
| | Machine Model (MM) | | 400 | | | |

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Fault conditions are viewed as beyond the normal operating range of the part.
5. Not subject to production testing.

TYPICAL PERFORMANCE CURVES

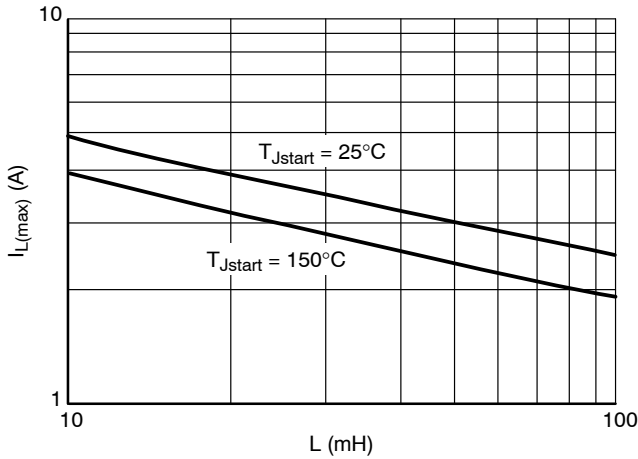


Figure 2. Single Pulse Maximum Switch-off Current vs. Load Inductance

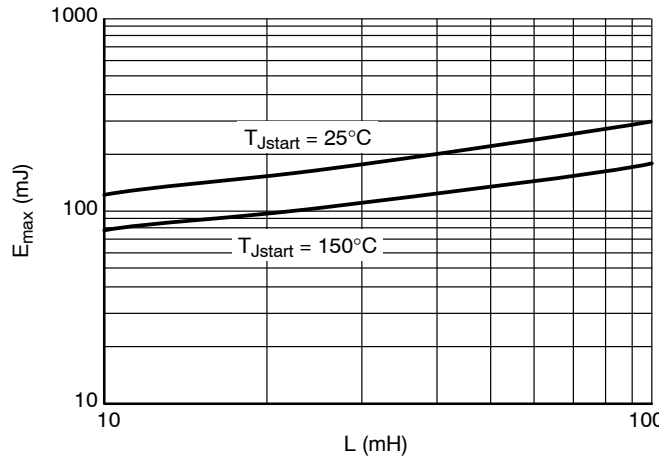


Figure 3. Single Pulse Maximum Switching Energy vs. Load Inductance

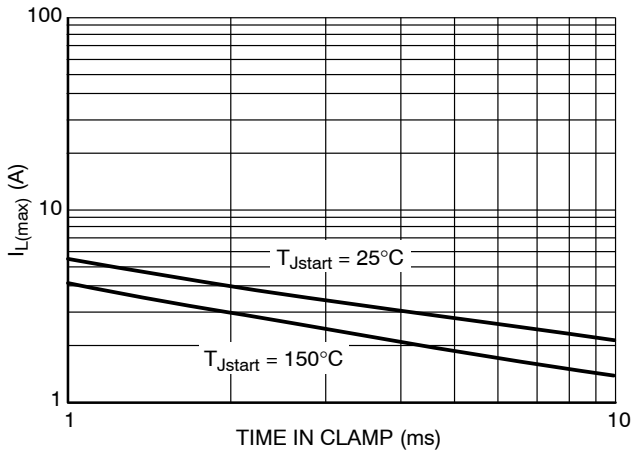


Figure 4. Single Pulse Maximum Inductive Switch-off Current vs. Time in Clamp

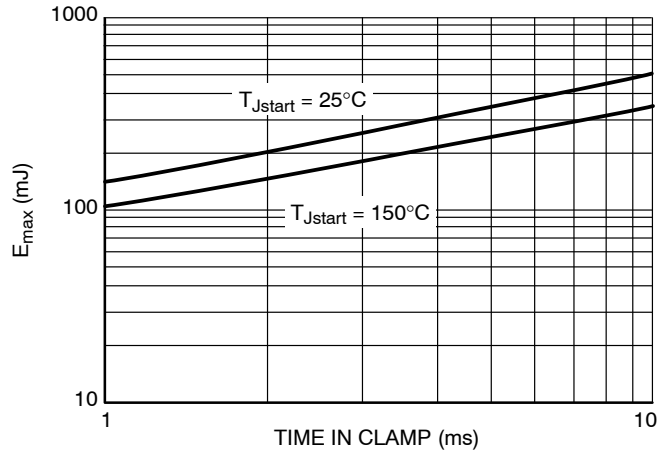


Figure 5. Single Pulse Maximum Inductive Switching Energy vs. Time in Clamp

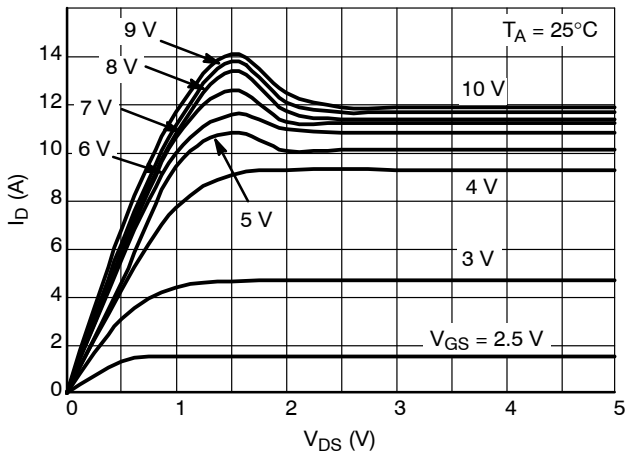


Figure 6. Output Characteristics

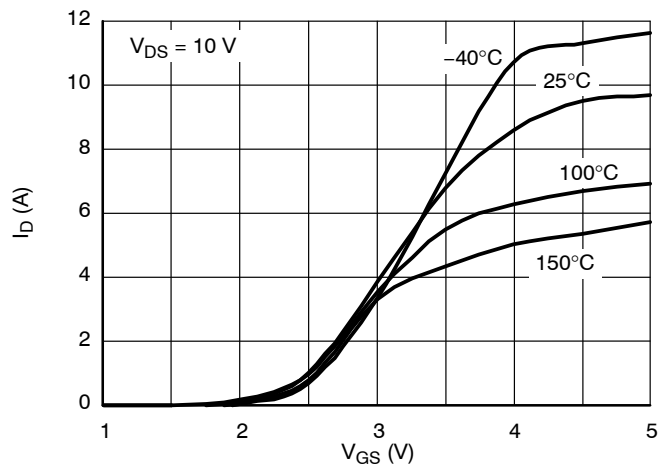


Figure 7. Transfer Characteristics

TYPICAL PERFORMANCE CURVES

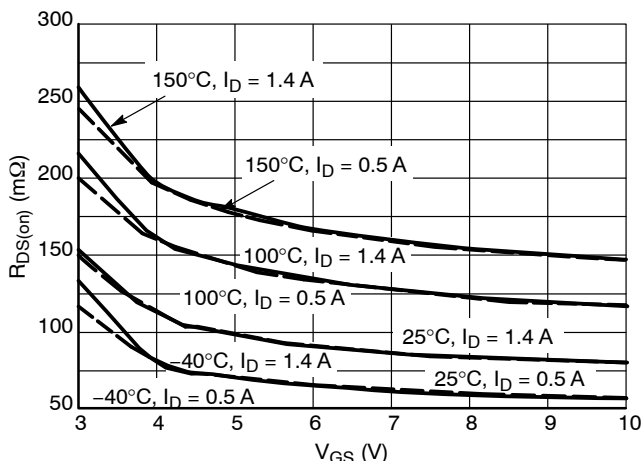


Figure 8. $R_{DS(on)}$ vs. Gate-Source Voltage

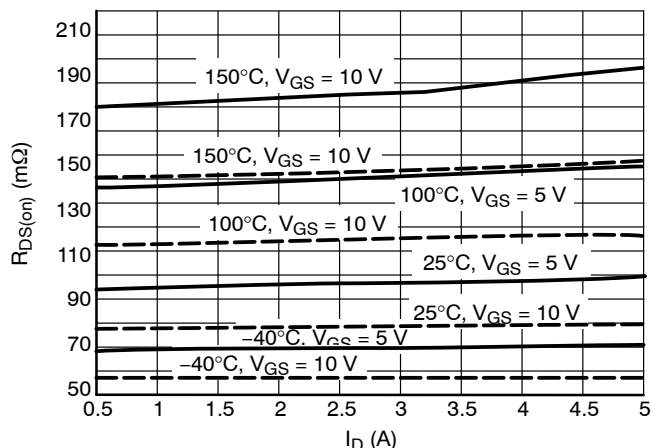


Figure 9. $R_{DS(on)}$ vs. Drain Current

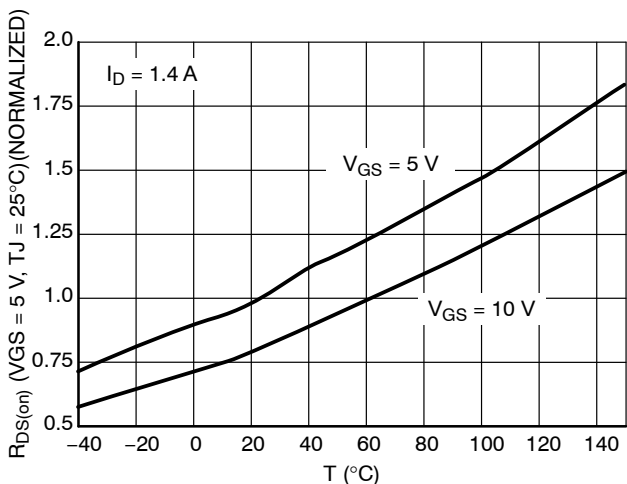


Figure 10. Normalized $R_{DS(on)}$ vs. Temperature

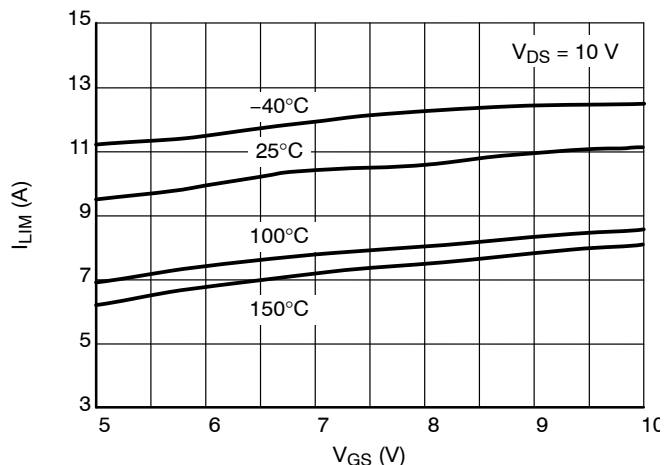


Figure 11. Current Limit vs. Gate-Source Voltage

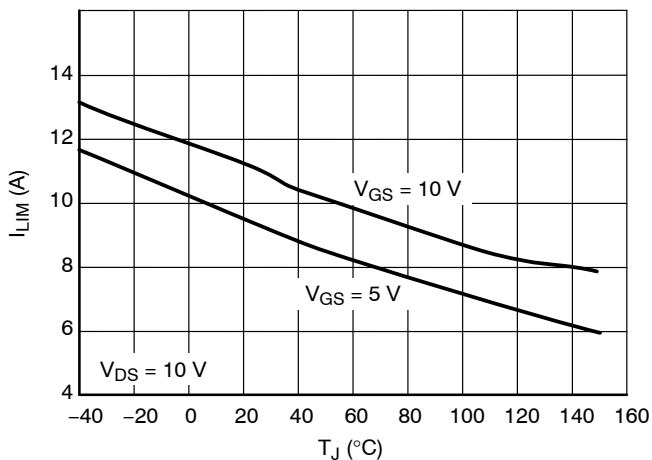


Figure 12. Current Limit vs. Junction Temperature

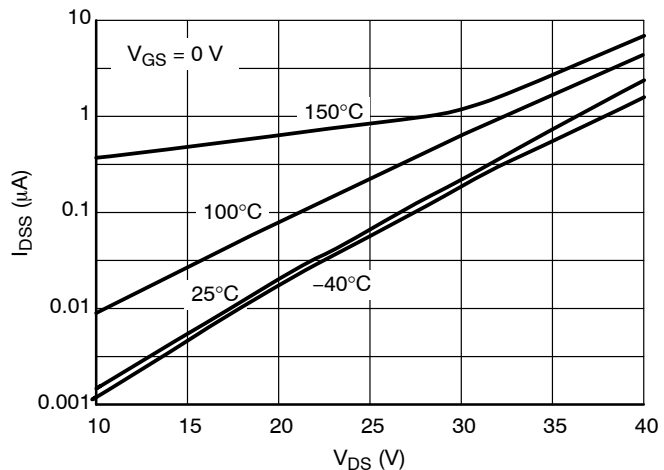


Figure 13. Drain-to-Source Leakage Current

TYPICAL PERFORMANCE CURVES

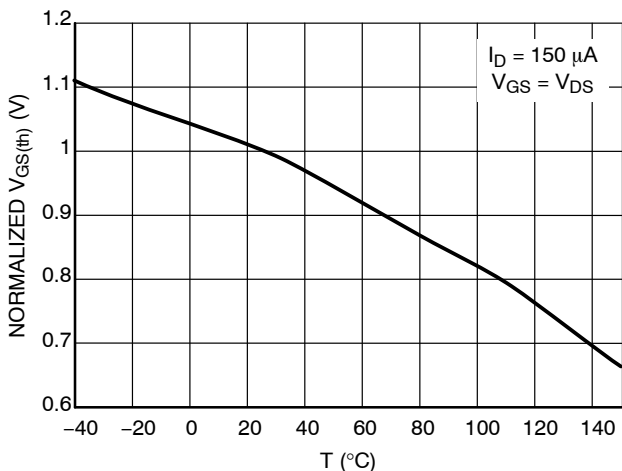


Figure 14. Normalized Threshold Voltage vs. Temperature

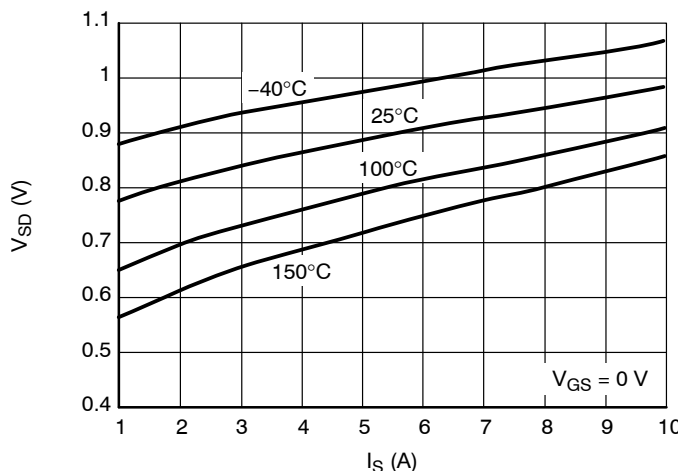


Figure 15. Body-Diode Forward Characteristics

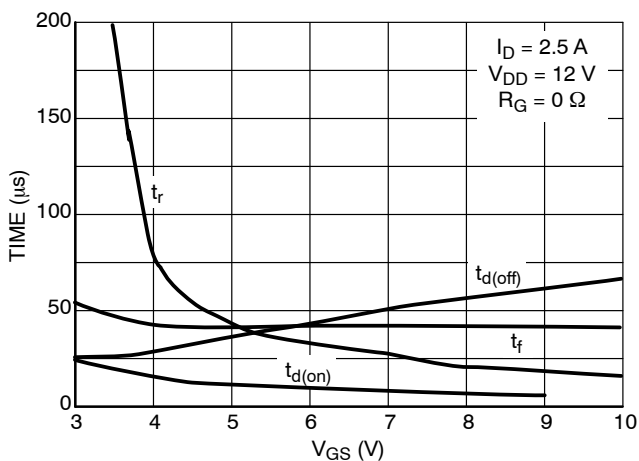


Figure 16. Resistive Load Switching Time vs. Gate-Source Voltage

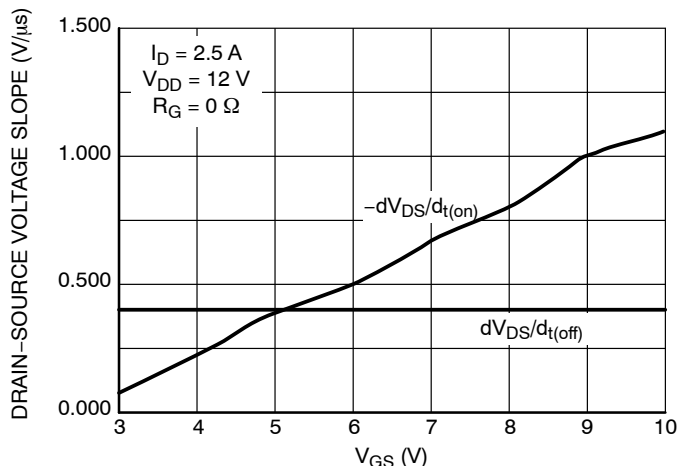


Figure 17. Resistive Load Switching Drain-Source Voltage Slope vs. Gate-Source Voltage

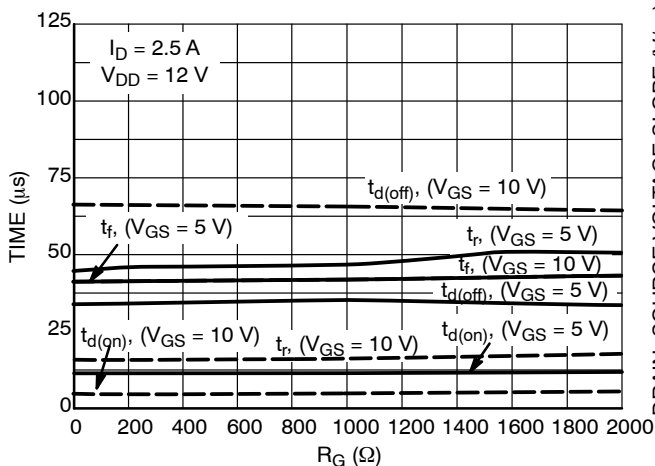


Figure 18. Resistive Load Switching Time vs. Gate Resistance

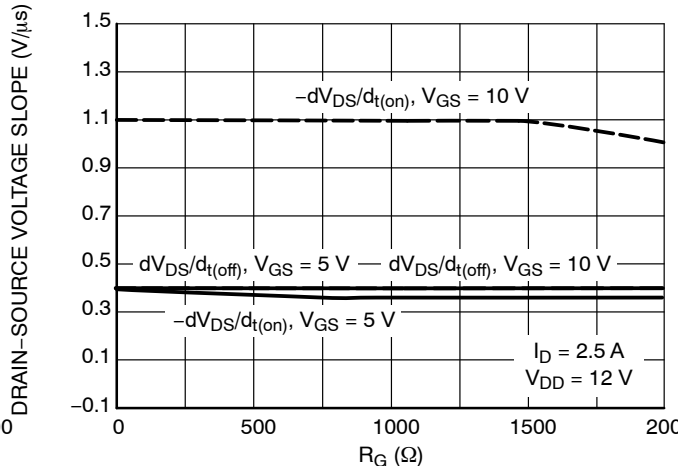


Figure 19. Drain-Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance

NCV8405A, NCV8405B

TYPICAL PERFORMANCE CURVES

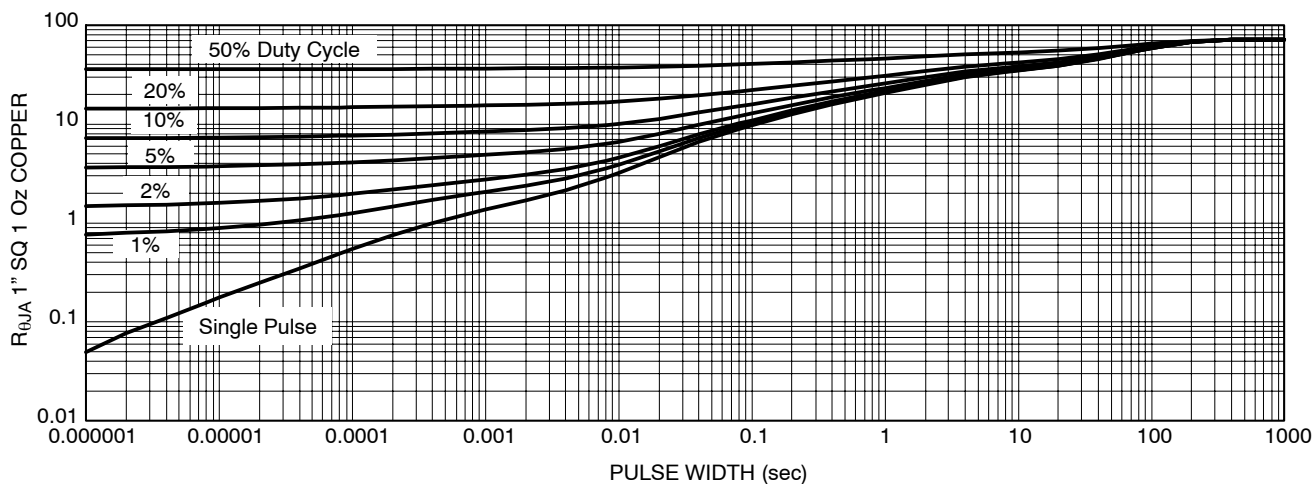


Figure 20. Transient Thermal Resistance

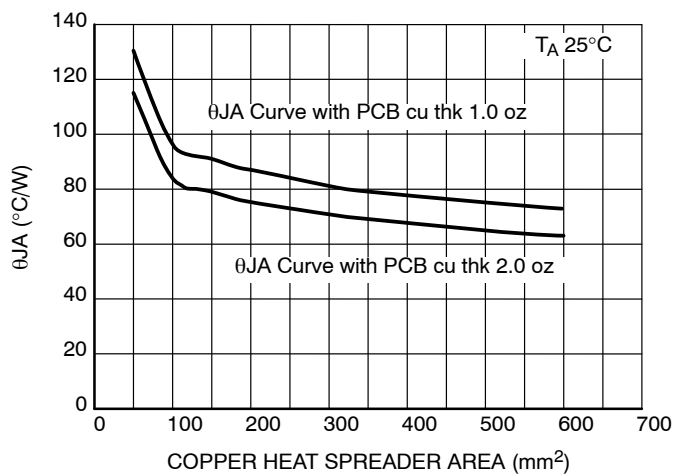


Figure 21. θ_{JA} vs. Copper

NCV8405A, NCV8405B

TEST CIRCUITS AND WAVEFORMS

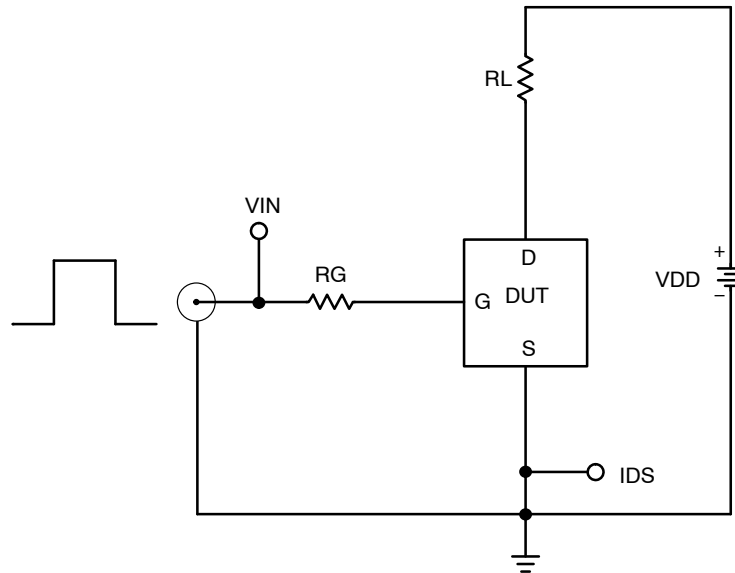


Figure 22. Resistive Load Switching Test Circuit

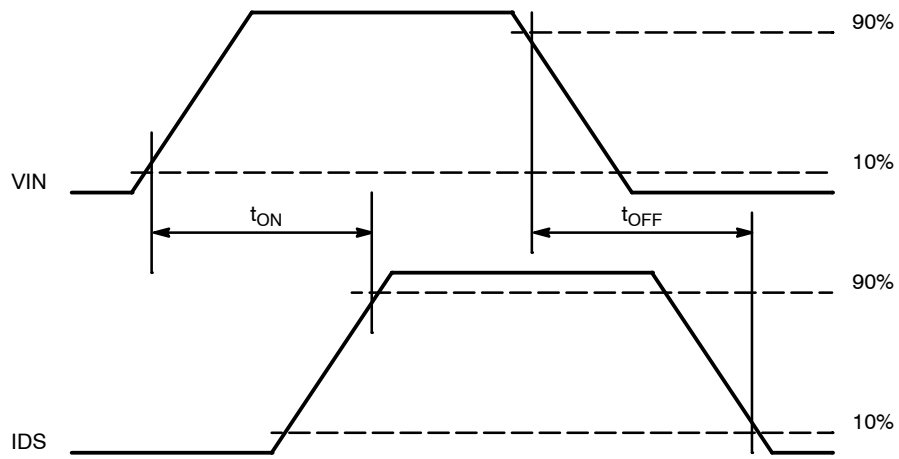


Figure 23. Resistive Load Switching Waveforms

NCV8405A, NCV8405B

TEST CIRCUITS AND WAVEFORMS

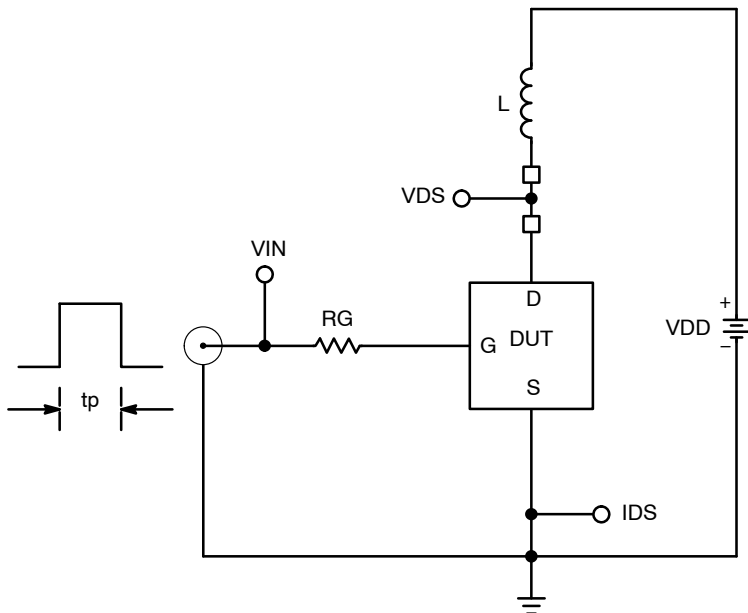


Figure 24. Inductive Load Switching Test Circuit

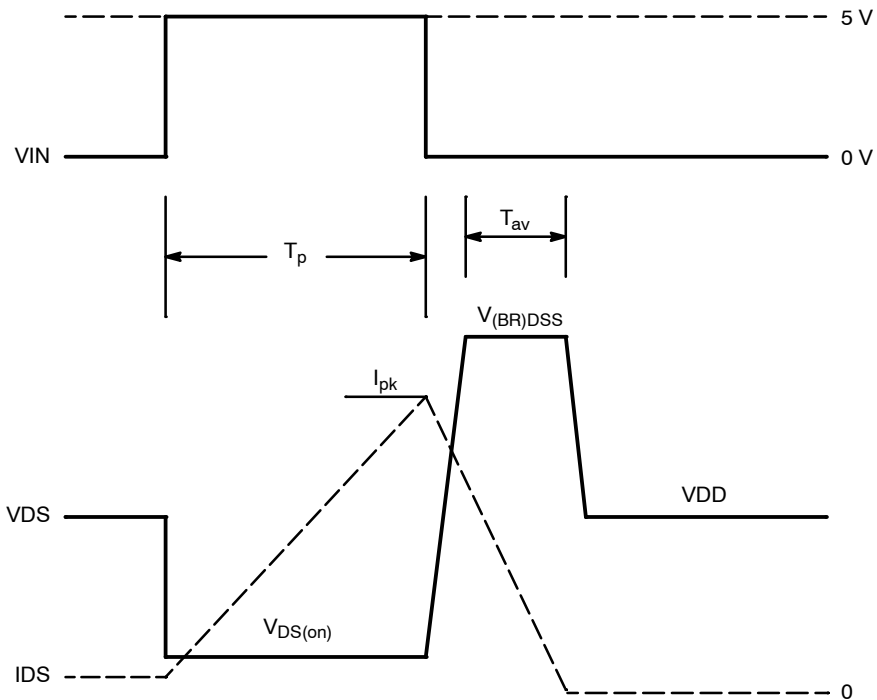


Figure 25. Inductive Load Switching Waveforms

NCV8405A, NCV8405B

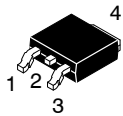
ORDERING INFORMATION

| Device | Package | Shipping† |
|---------------|----------------------|--------------------|
| NCV8405ASTT1G | SOT-223 (Pb-Free) | 1000 / Tape & Reel |
| NCV8405ASTT3G | SOT-223 (Pb-Free) | 4000 / Tape & Reel |
| NCV8405ADTRKG | DPAK (Pb-Free) | 2500 / Tape & Reel |
| NCV8405BDTRKG | DPAK (Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



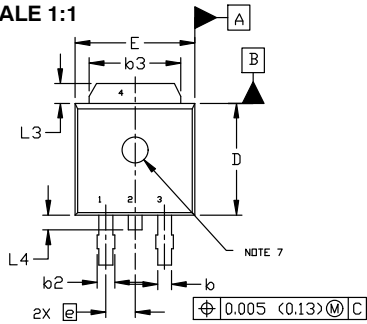
DPAK (SINGLE GAUGE)

CASE 369C

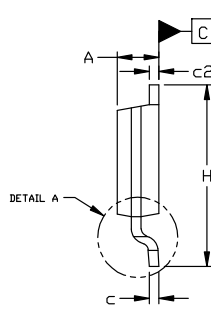
ISSUE G

DATE 31 MAY 2023

SCALE 1:1



TOP VIEW

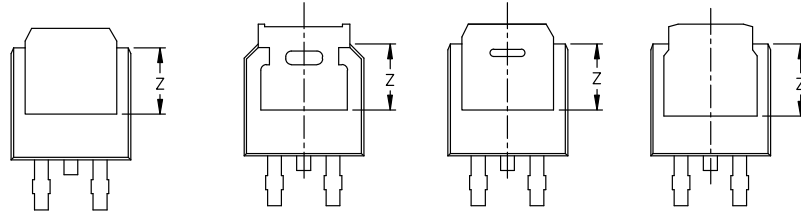


SIDE VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

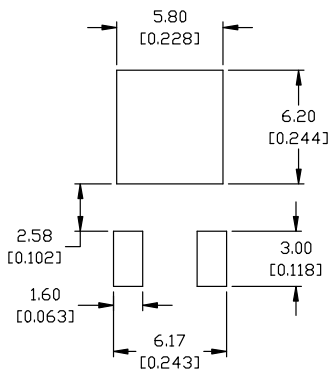
| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-------|-------------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.028 | 0.045 | 0.72 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 | BSC | 2.29 | BSC |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.114 | REF | 2.90 | REF |
| L2 | 0.020 | BSC | 0.51 | BSC |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | --- | 0.040 | --- | 1.01 |
| Z | 0.155 | --- | 3.93 | --- |



BOTTOM VIEW

BOTTOM VIEW

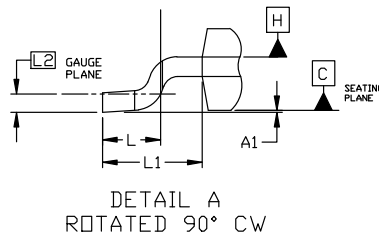
ALTERNATE CONSTRUCTIONS



RECOMMENDED MOUNTING FOOTPRINT*

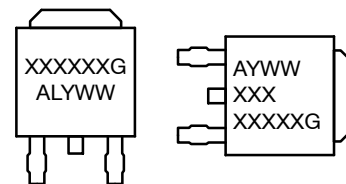
*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

- | | | | | |
|--|--|---|---|--|
| STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR | STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN | STYLE 3: PIN 1. ANODE 2. CATHODE 3. ANODE 4. CATHODE | STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE | STYLE 5: PIN 1. GATE 2. ANODE 3. CATHODE 4. ANODE |
| STYLE 6: PIN 1. MT1 2. MT2 3. GATE 4. MT2 | STYLE 7: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR | STYLE 8: PIN 1. N/C 2. CATHODE 3. ANODE 4. CATHODE | STYLE 9: PIN 1. ANODE 2. CATHODE 3. RESISTOR ADJUST 4. CATHODE | STYLE 10: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. ANODE |



DETAIL A
ROTATED 90° CW

GENERIC MARKING DIAGRAM*



IC

Discrete

- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|-------------------------|----------------------------|--|
| DOCUMENT NUMBER: | 98AON10527D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | DPAK (SINGLE GAUGE) | PAGE 1 OF 1 |

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