Multiple Range, 16-Bit, Bipolar/Unipolar Voltage Output DAC with 7 ppm/°C Reference

Enhanced Product

AD5761R-EP

FEATURES

- 8 software-programmable output ranges: 0 V to 5 V, 0 V to 10 V, 0 V to 16 V, 0 V to 20 V, −2.5 V to +7.5 V, ±3 V, ±5 V, and ±10 V; 5% overrange
- Low drift 2.5 V reference: ±7 ppm/°C typical
- TUE: ±0.1% FSR maximum
- 16-bit relative accuracy (INL): ±8 LSB maximum
- Guaranteed monotonicity (DNL): ±1 LSB maximum
- Single channel, 16-bit DAC
- Output voltage settling time
  - 7.5 µs typical, 10 V step to 1 LSB at 16-bit resolution
- Integrated reference buffers
- Low noise: 35 nV/√Hz (±3 V range)
- Low glitch: 1 nV-sec (0 V to 5 V range)
- 1.7 V to 5.5 V digital supply range (DV_{CC})
- Asynchronous updating via $\overline{LDAC}$
- Asynchronous $\overline{RESET}$ to zero scale/midscale
- DSP-/microcontroller-compatible serial interface
- Robust 4 kV HBM ESD rating
- 16-lead TSSOP package
- Operating temperature range: −55°C to +125°C

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range: −55°C to +125°C
- Controlled manufacturing baseline
- 1 assembly/test site
- 1 fabrication site
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- Industrial automation
- Instrumentation, data acquisition
- Open-/closed-loop servo control, process control
- Programmable logic controllers

GENERAL DESCRIPTION

The AD5761R-EP is a single-channel, 16-bit serial input, voltage output, digital-to-analog converter (DAC). It operates from single-supply voltages from 4.75 V to 30 V V_{DD} or dual supply voltages from −16.5 V to 0 V V_{SS} and 4.75 V to 16.5 V V_{DD}. The integrated output amplifier, reference buffer, and reference provide an easy to use, universal solution.

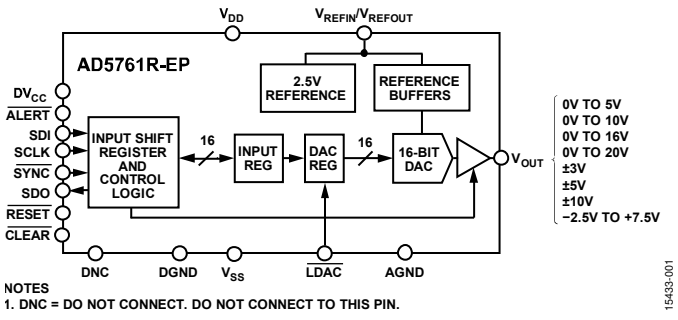
The device offers guaranteed monotonicity, integral nonlinearity (INL) of ±8 LSB maximum, 35 nV/√Hz noise, and a 7.5 µs settling time on selected ranges.

The AD5761R-EP uses a serial interface that operates at clock rates of up to 50 MHz and is compatible with digital signal processor (DSP) and microcontroller interface standards. Double buffering allows the asynchronous updating of the DAC output. The input coding is user selectable, twos complement or straight binary. The asynchronous reset function resets all registers to their default state. The output range is user selectable via the RA[2:0] bits in the control register.

The device is available in a 16-lead TSSOP package, and it offers guaranteed specifications over the −55°C to +125°C military temperature range.

Additional application and technical information can be found in the AD5761R data sheet.

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

Figure 1.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

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REVISION HISTORY

3/2017—Revision 0: Initial Version

SPECIFICATIONS

V_{DD}[1] = 4.75 V to 30 V, V_{SS}[1] = −16.5 V to 0 V, AGND = DGND = 0 V, V_{REFIN}/V_{REFOUT} = 2.5 V external, DV_{CC} = 1.7 V to 5.5 V, R_{LOAD} = 1 kΩ for all ranges except 0 V to 16 V and 0 V to 20 V for which R_{LOAD} = 2 kΩ, C_{LOAD} = 200 pF, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted. Temperature range: −55°C to +125°C, typical at +25°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE					External reference[2] and internal reference, outputs unloaded
Programmable Output Ranges	0		5	V	
	0		10	V	
	0		16	V	
	0		20	V	
	−2.5		+7.5	V	
	−3		+3	V	
	−5		+5	V	
	−10		+10	V	
Resolution	16			Bits	
Relative Accuracy (INL)	−8		+8	LSB	External reference[2] and internal reference
Differential Nonlinearity (DNL)	−1		+1	LSB	
Zero-Scale Error	−6		+6	mV	All ranges except ±10 V and 0 V to 20 V, external reference[2]
	−10		+10	mV	0 V to 20 V, ±10 V ranges, external reference[2]
	−6		+6	mV	All ranges except ±5 V, ±10 V, and 0 V to 20 V, internal reference
	−8		+8	mV	±5 V range, internal reference
	−9		+9	mV	0 V to 20 V range, internal reference
	−13		+13	mV	±10 V range, internal reference
Zero-Scale Temperature Coefficient (TC)[3]		±5		µV/°C	Unipolar ranges, external reference[2] and internal reference
		±15		µV/°C	Bipolar ranges, external reference[2] and internal reference
Bipolar Zero Error	−5		+5	mV	All bipolar ranges except ±10 V
	−7		+7	mV	±10 V output range
Bipolar Zero TC[3]		±2		µV/°C	±3 V range, external reference[2] and internal reference
		±5		µV/°C	All bipolar ranges except ±3 V range, external reference[2] and internal reference
Offset Error	−6		+6	mV	All ranges except ±10 V and 0 V to 20 V, external reference[2]
	−10		+10	mV	0 V to 20 V, ±10 V ranges, external reference[2]
	−6		+6	mV	All ranges except ±5 V, ±10 V, and 0 V to 20 V; internal reference
	−8		+8	mV	±5 V range, internal reference
	−9		+9	mV	0 V to 20 V range, internal reference
	−18		+18	mV	±10 V range, internal reference
Offset Error TC[3]		±5		µV/°C	Unipolar ranges, external reference[2] and internal reference
		±15		µV/°C	Bipolar ranges, external reference[2] and internal reference
Gain Error	−0.1		+0.1	% FSR	External reference[2]
	−0.15		+0.15	% FSR	Internal reference
Gain Error TC[3]		±1.5		ppm FSR/°C	External reference[2] and internal reference
Total Unadjusted Error (TUE)	−0.1		+0.1	% FSR	External reference[2]
	−0.15		+0.15	% FSR	Internal reference

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE INPUT (EXTERNAL)[3]					
Reference Input Voltage (V_{REF})		2.5		V	±1% for specified performance
Input Current	−2	±0.5	+2	µA	
Reference Range	2		3	V	
REFERENCE OUTPUT (INTERNAL)[3]					
Output Voltage		2.5		V	±3 mV, at ambient temperature
Voltage Reference TC		7	25	ppm/°C	
Output Impedance		25		kΩ	
Output Voltage Noise		6		µV p-p	0.1 Hz to 10 Hz
Noise Spectral Density		10		nV/√Hz	At ambient; f = 10 kHz
Line Regulation		6		µV/V	At ambient
Thermal Hysteresis		±80		ppm	First temperature cycle
Start-Up Time		3.5		ms	Coming out of power-down mode with a 10 nF capacitor on the V_{REFIN}/V_{REFOUT} pin improves noise performance; outputs unloaded
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	$-V_{OUT}$		$+V_{OUT}$		Seethe AD5761R data sheet for the different output voltage ranges available
	−10		+10	V	V_{DD}/V_{SS} = ±11 V, ±10 V output range
	−10.5		+10.5	V	V_{DD}/V_{SS} = ±11 V, ±10 V output range with 5% overrange
Capacitive Load Stability			1	nF	
Headroom		0.5	1	V	R_{LOAD} = 1 kΩ for all ranges except 0 V to16 V and 0 V to 20 V ranges (R_{LOAD} = 2 kΩ)
Output Voltage TC		±3		ppm FSR/°C	±10 V range, external reference
Short-Circuit Current		25		mA	Short on the V_{OUT} pin
Resistive Load			1	kΩ	All ranges except 0 V to16 V and 0 V to 20 V
			2	kΩ	0 V to 16 V, 0 V to 20 V ranges
Load Regulation		0.3		mV/mA	Outputs unloaded
DC Output Impedance		0.5		Ω	Outputs unloaded
LOGIC INPUTS[3]					DV_{CC} = 1.7 V to 5.5 V, JEDEC compliant
Input Voltage					
High (V_{IH})	0.7 × DV_{CC}			V	
Low (V_{IL})			0.3 × DV_{CC}	V	
Input Current					
Leakage Current	−1		+1	µA	SDI, SCLK, $\overline{SYNC}$
	−1		+1	µA	$\overline{LDAC}$, $\overline{CLEAR}$, $\overline{RESET}$ pins held high
	−55			µA	$\overline{LDAC}$, $\overline{CLEAR}$, $\overline{RESET}$ pins held low
Pin Capacitance		5		pF	Per pin, outputs unloaded
LOGIC OUTPUTS (SDO, $\overline{ALERT}$)[3]					
Output Voltage					
Low (V_{OL})			0.4	V	DV_{CC} = 1.7 V to 5.5 V, sinking 200 µA
High (V_{OH})	DV_{CC} − 0.5			V	DV_{CC} = 1.7 V to 5.5 V, sourcing 200 µA
High Impedance, SDO Pin					
Leakage Current	−1		+1	µA	
Pin Capacitance		5		pF	
POWER REQUIREMENTS					
Single Supply					
V_{DD}	4.75		30	V	
V_{SS}		0		V	
Dual Supply					
V_{DD}	4.75		16.5	V	
V_{SS}	−16.5		0	V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DV_{CC}	1.7		5.5	V	
I_{DD}		5.1	6.5	mA	Outputs unloaded, external reference
I_{SS}		1	3	mA	Outputs unloaded
DI_{CC}		0.005	1	µA	$V_{IH} = DV_{CC}$, V_{IL} = DGND
Power Dissipation		67.1		mW	±11 V operation, outputs unloaded
DC Power Supply Rejection Ratio (PSRR)[3]		0.1		mV/V	V_{DD} ± 10%, V_{SS} = −15 V
		0.1		mV/V	V_{SS} ±10%, V_{DD} = +15 V
AC PSRR[3]		65		dB	V_{DD} ±200 mV, 50 Hz/60 Hz, V_{SS} = −15 V, internal reference, C_{LOAD} = 100 nF
		65		dB	V_{SS} ±200 mV, 50 Hz/60 Hz, V_{DD} = +15 V, internal reference, C_{LOAD} = 100 nF
		80		dB	V_{DD} ±200 mV, 50 Hz/60 Hz, V_{SS} = −15 V, external reference, C_{LOAD} = unloaded
		80		dB	V_{SS} ±200 mV, 50 Hz/60 Hz, V_{DD} = +15 V, external reference, C_{LOAD} = unloaded

[1] For specified performance, headroom requirement is 1 V. V_{DD} = 4.75 V to 30 V and V_{SS} = 0 V for single-supply operation, and V_{DD} = 4.75 V to 16.5 V and V_{SS} = −16.5 V to 0 V for dual-supply operation.
[2] External reference is 2 V to 2.85 V with overrange and 2 V to 3 V without overrange.
[3] Guaranteed by design and characterization, not production tested.

AC PERFORMANCE CHARACTERISTICS

V_{DD}[1] = 4.75 V to 30 V, V_{SS}[1] = −16.5 V to 0 V, AGND = DGND = 0 V, V_{REFIN}/V_{REFOUT} = 2.5 V external, DV_{CC} = 1.7 V to 5.5 V, R_{LOAD} = 1 kΩ for all ranges except 0 V to 16 V and 0 V to 20 V for which R_{LOAD} = 2 kΩ, C_{LOAD} = 200 pF, all specifications T_{MIN} to T_{MAX}, unless otherwise noted. Temperature range: −55°C to +125°C, typical at +25°C. Guaranteed by design and characterization, not production tested.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Output Voltage Settling Time		9	12.5	µs	20 V step to 1 LSB at 16-bit resolution
		7.5	8.5	µs	10 V step to 1 LSB at 16-bit resolution
			5	µs	512 LSB step to 1 LSB at 16-bit resolution
Digital-to-Analog Glitch Impulse		8		nV-sec	±10 V range
		1		nV-sec	0 V to 5 V range
Glitch Impulse Peak Amplitude		15		mV	±10 V range
		10		mV	0 V to 5 V range
Power-On Glitch		100		mV p-p	
Digital Feedthrough		0.6		nV-sec	
Output Noise					
0.1 Hz to 10 Hz Bandwidth		15		µV p-p	
100 kHz Bandwidth		45		µV rms	0 V to 20 V and 0 V to 16 V ranges, 2.5 V external reference
		35		µV rms	0 V to 10 V, ±10 V, and −2.5 V to +7.5 V ranges, 2.5 V external reference
		25		µV rms	±5 V range, 2.5 V external reference
		15		µV rms	0 V to 5 V and ±3 V ranges, 2.5 V external reference
Output Noise Spectral Density, at 10 kHz		80		nV/√Hz	±10 V range, 2.5 V external reference
		35		nV/√Hz	±3 V range, 2.5 V external reference
		70		nV/√Hz	±5 V, 0 V to 10 V, and −2.5 V to +7.5 V ranges, 2.5 V external reference
		110		nV/√Hz	0 V to 20 V range, 2.5 V external reference
		90		nV/√Hz	0 V to 16 V range, 2.5 V external reference
		45		nV/√Hz	0 V to 5 V range, 2.5 V external reference
Total Harmonic Distortion (THD)[2]		−87		dB	2.5 V external reference, 1 kHz tone
Signal-to-Noise Ratio (SNR)		92		dB	At ambient, 2.5 V external reference, bandwidth (BW) = 20 kHz, f_{OUT} = 1 kHz
Peak Harmonic or Spurious Noise (SFDR)		92		dB	At ambient, 2.5 V external reference, BW = 20 kHz, f_{OUT} = 1 kHz
Signal-to-Noise-and-Distortion (SINAD) Ratio		85		dB	At ambient, 2.5 V external reference, BW = 20 kHz, f_{OUT} = 1 kHz

[1] For specified performance, headroom requirement is 1 V. V_{DD} = 4.75 V to 30 V and V_{SS} = 0 V for single-supply operation, and V_{DD} = 4.75 V to 16.5 V and V_{SS} = −16.5 V to 0 V for dual-supply operation.
[2] Digitally generated sine wave at 1 kHz.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 200 mA do not cause silicon controlled rectifier (SCR) latch-up.

Table 3.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +34 V
V_{SS} to AGND	+0.3 V to −17 V
V_{DD} to V_{SS}	−0.3 V to +34 V
DV_{CC} to DGND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to DV_{CC} + 0.3 V or 7 V (whichever is less)
Digital Outputs to DGND	−0.3 V to DV_{CC} + 0.3 V or 7 V (whichever is less)
V_{REFIN}/V_{REFOUT} to DGND	−0.3 V to +7 V
V_{OUT} to AGND	V_{SS} to V_{DD}
AGND to DGND	−0.3 V to +0.3 V
Military Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature, $T_{J\,MAX}$	150°C
θ_{JA} Thermal Impedance	113°C/W[1]
Power Dissipation	See Figure 2
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020
ESD (Human Body Model)	4 kV

[1] JEDEC 2S2P test board, still air (0 m/sec airflow).

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

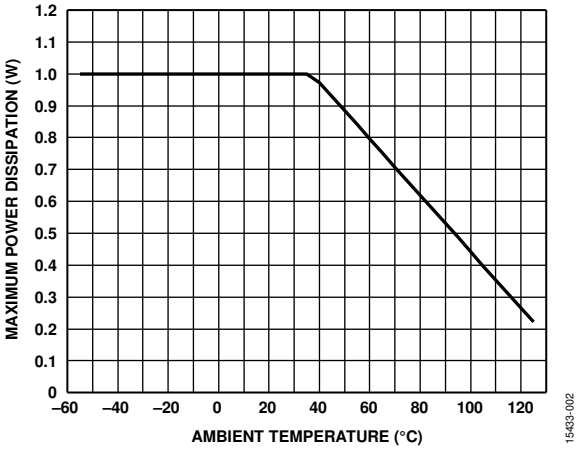

Figure 2. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

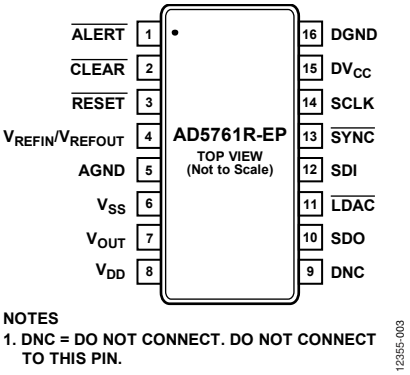

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{ALERT}}$	Active Low Alert. This pin is asserted low when the die temperature exceeds approximately 150°C, or when an output short circuit or a brownout occurs. This pin is also asserted low during power-up, a full software reset, or a hardware reset for which a write to the control register asserts the pin high.
2	$\overline{\text{CLEAR}}$	Falling Edge Clear Input. Asserting this pin sets the DAC register to zero-scale, midscale, or full-scale code (user selectable) and updates the DAC output. This pin can be left floating because there is an internal pull-up resistor.
3	$\overline{\text{RESET}}$	Active Low Reset Input. Asserting this pin returns the AD5761R-EP to its default power-on status where the output is clamped to ground, and the output buffer is powered down. This pin can be left floating because there is an internal pull-up resistor.
4	V_{REFIN}/V_{REFOUT}	Internal Reference Voltage Output and External Reference Voltage Input. For specified performance, V_{REFIN}/V_{REFOUT} = 2.5 V. Connect a 10 nF capacitor with the internal reference to minimize the noise.
5	AGND	Ground Reference Pin for Analog Circuitry.
6	V_{SS}	Negative Analog Supply Connection. A voltage in the range of −16.5 V to 0 V can be connected to this pin. For unipolar output ranges, connect this pin to 0 V. V_{SS} must be decoupled to AGND.
7	V_{OUT}	Analog Output Voltage of the DAC. The output amplifier is capable of directly driving a 2 kΩ, 1 nF load.
8	V_{DD}	Positive Analog Supply Connection. A voltage in the range of 4.75 V to 30 V can be connected to this pin for unipolar output ranges. Bipolar output ranges accept a voltage in the range of 4.75 V to 16.5 V. V_{DD} must be decoupled to AGND.
9	DNC	Do Not Connect. Do not connect to this pin.
10	SDO	Serial Data Output. This pin clocks data from the serial register in daisy-chain or readback mode. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.
11	$\overline{\text{LDAC}}$	Load DAC. This logic input updates the DAC register and, consequently, the analog output. When tied permanently low, the DAC register is updated when the input register is updated. If $\overline{\text{LDAC}}$ is held high during the write to the input register, the DAC output register is not updated, and the DAC output update is held off until the falling edge of $\overline{\text{LDAC}}$. This pin can be left floating because there is an internal pull-up resistor.
12	SDI	Serial Data Input. Data must be valid on the falling edge of SCLK.
13	$\overline{\text{SYNC}}$	Active Low Synchronization Input. This pin is the frame synchronization signal for the serial interface. While $\overline{\text{SYNC}}$ is low, data is transferred in on the falling edge of SCLK. Data is latched on the rising edge of $\overline{\text{SYNC}}$.
14	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of SCLK. This pin operates at clock speeds of up to 50 MHz.
15	DV_{CC}	Digital Supply. The voltage range is from 1.7 V to 5.5 V. The applied voltage sets the voltage at which the digital interface operates.
16	DGND	Digital Ground.

TYPICAL PERFORMANCE CHARACTERSTICS

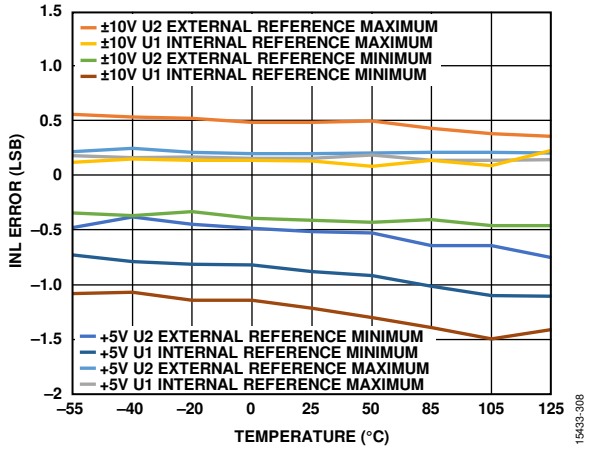

Figure 4. INL Error vs. Temperature

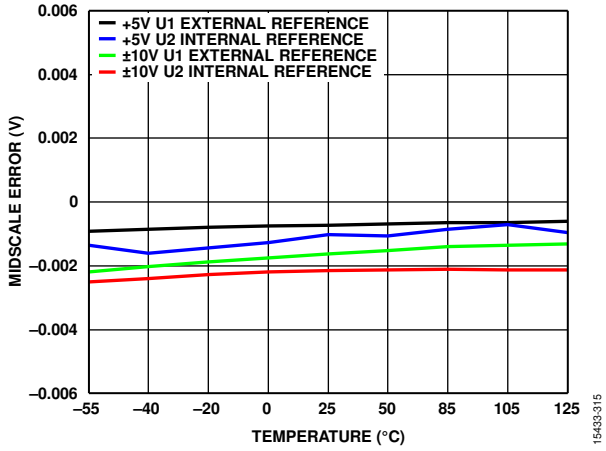

Figure 7. Midscale Error vs. Temperature

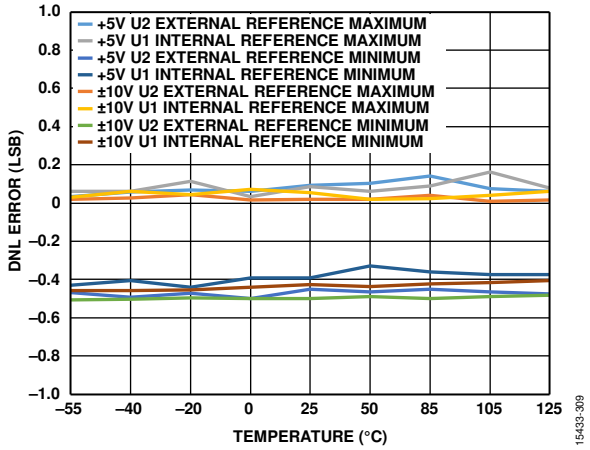

Figure 5. DNL Error vs. Temperature

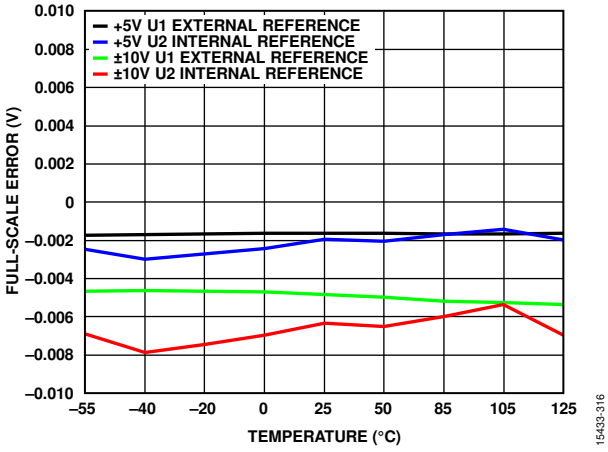

Figure 8. Full-Scale Error vs. Temperature

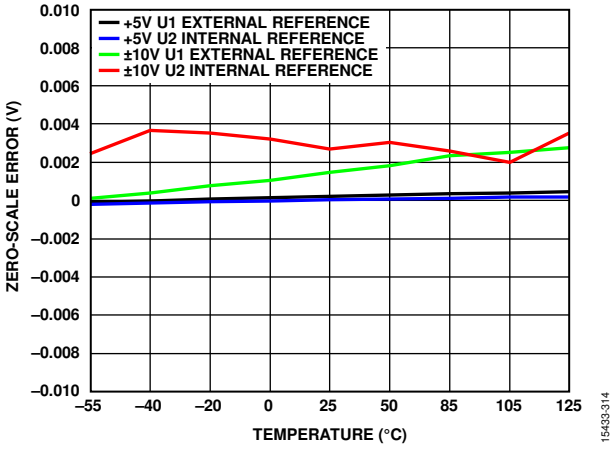

Figure 6. Zero-Scale Error vs. Temperature

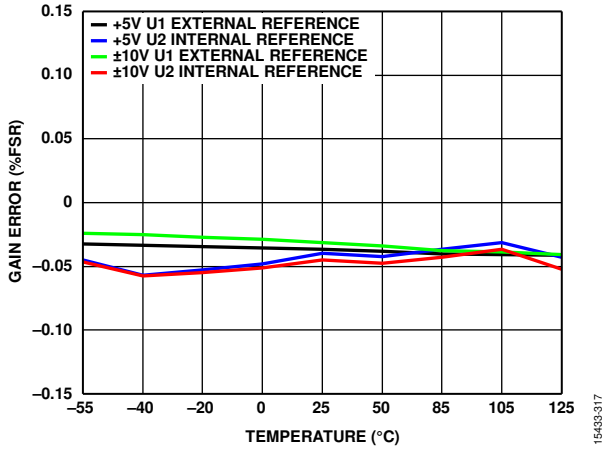

Figure 9. Gain Error vs. Temperature

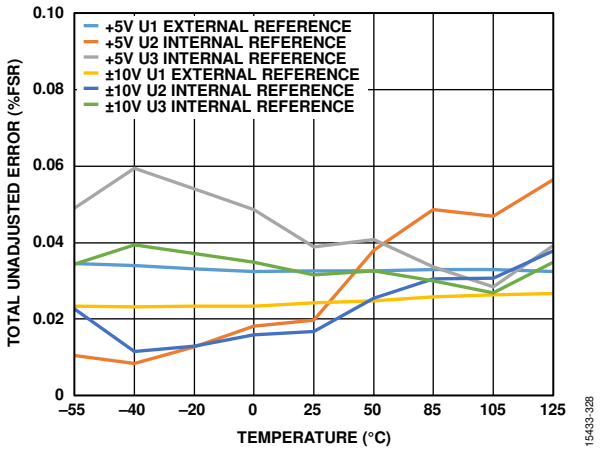

Figure 10. Total Unadjusted Error (TUE) vs. Temperature

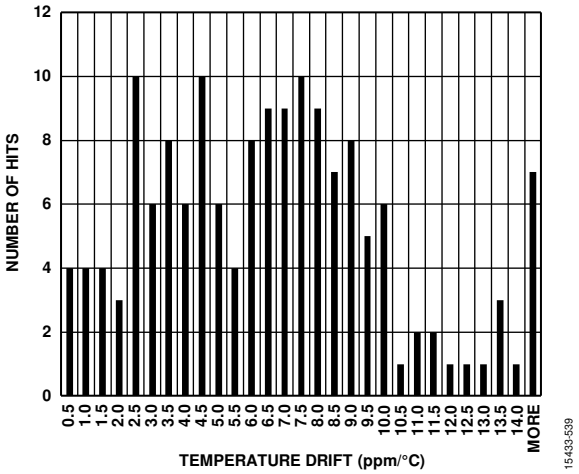

Figure 12. Reference Output TC

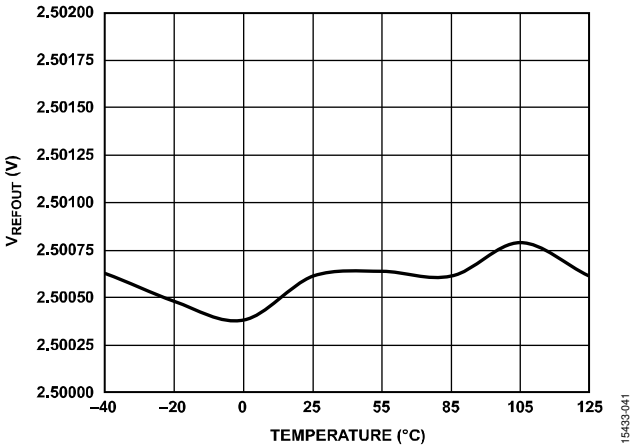

Figure 11. Reference Output Voltage vs. Temperature

OUTLINE DIMENSIONS

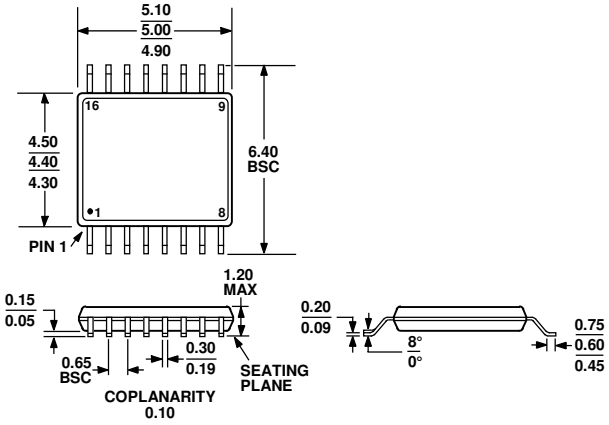

Figure 13. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Resolution (Bits)	Internal Reference (V)	Temperature Range	INL (LSB)	Package Description	Package Option
AD5761RTRUZ-EP	16	2.5	−55°C to +125°C	±8	16-Lead TSSOP	RU-16
AD5761RTRUZ-EP-RL7	16	2.5	−55°C to +125°C	±8	16-Lead TSSOP	RU-16

[1] Z = RoHS Compliant Part.