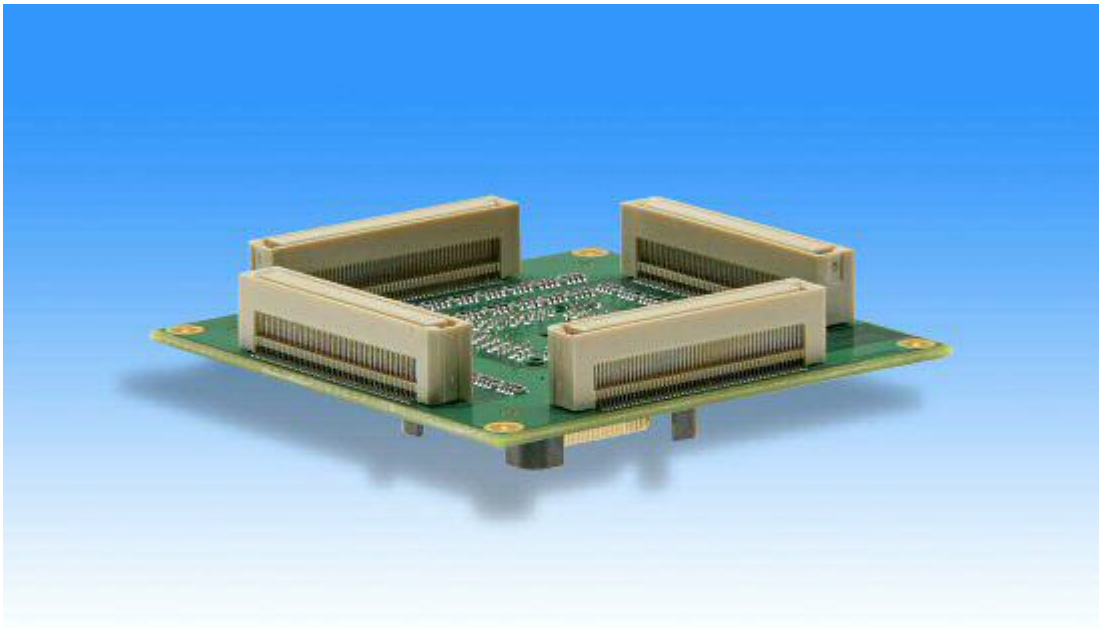


FR60 FAMILY

SOCKET ADAPTER BOARD

EMA-MB91F467D-LS-208M04

USER GUIDE



Revision History

| Date | Issue |
|------------|--|
| 12.09.2006 | V1.00, RH/AW First Release |
| 10.10.2006 | V1.01, AW J490 bug: Do not set J490:2-3 |
| 16.10.2006 | V1.02, AW Jumper description, default settings |
| 09.03.2007 | V1.1, MB/RW New hardware revision |
| 30.03.2007 | V1.2, MB UG-910030-11-EMA-MB91F467D-LS-208M04-corr-x1-00 corrections added |
| 17.04.2007 | A 33 pf capacitor is connected between MCLKO (R438) and GND. |
| 29.05.2007 | V1.3, chapter 1.3 added, amendment to figure 3.1 |
| 30.05.2007 | V1.4, chapter 7 added |
| 08.01.2008 | V1.5, CPLD code changed, chapter 4.2 and chapter 5 changed |
| 11.04.2008 | V1.6, China RoHS note added, new format of CPLD code, S401-9 added |
| 25.04.2008 | V1.7, page 16: "The port P03 and P04..." -> "The port P03 and P02..." and CPLD code comments changed |
| 26.05.2008 | V1.8, CPLD code spelling fixed (identical behaviour) |
| 29.09.2008 | V1.9, CEy Some minor corrections |
| 16.01.2009 | V2.0, CEy Description for EMA-MB91FV460B-001 added |

Latest product revision: 1.1
Schematic version: 2.5
PCB version: 3.0
CPLD version: 7D12

This document contains 34 pages.

Warranty and Disclaimer

To the maximum extent permitted by applicable law, Fujitsu Microelectronics Europe GmbH restricts its warranties and its liability for **the EMA-MB91F467D-LS-208M04 Board and all its deliverables** (e.g. software include or header files, application examples, target boards, evaluation boards, engineering samples of IC's etc.), its performance and any consequential damages, on the use of the Product in accordance with (i) the terms of the License Agreement and the Sale and Purchase Agreement under which agreements the Product has been delivered, (ii) the technical descriptions and (iii) all accompanying written materials. In addition, to the maximum extent permitted by applicable law, Fujitsu Microelectronics Europe GmbH disclaims all warranties and liabilities for the performance of the Product and any consequential damages in cases of unauthorised decompiling and/or reverse engineering and/or disassembling. **Note, the EMA-MB91F467D-LS-208M04 Board and all its deliverables are intended and must only be used in an evaluation laboratory environment.**

1. Fujitsu Microelectronics Europe GmbH warrants that the Product will perform substantially in accordance with the accompanying written materials for a period of 90 days from the date of receipt by the customer. Concerning the hardware components of the Product, Fujitsu Microelectronics Europe GmbH warrants that the Product will be free from defects in material and workmanship under use and service as specified in the accompanying written materials for a duration of 1 year from the date of receipt by the customer.
2. Should a Product turn out to be defect, Fujitsu Microelectronics Europe GmbH's entire liability and the customer's exclusive remedy shall be, at Fujitsu Microelectronics Europe GmbH's sole discretion, either return of the purchase price and the license fee, or replacement of the Product or parts thereof, if the Product is returned to Fujitsu Microelectronics Europe GmbH in original packing and without further defects resulting from the customer's use or the transport. However, this warranty is excluded if the defect has resulted from an accident not attributable to Fujitsu Microelectronics Europe GmbH, or abuse or misapplication attributable to the customer or any other third party not relating to Fujitsu Microelectronics Europe GmbH.
3. To the maximum extent permitted by applicable law Fujitsu Microelectronics Europe GmbH disclaims all other warranties, whether expressed or implied, in particular, but not limited to, warranties of merchantability and fitness for a particular purpose for which the Product is not designated.
4. To the maximum extent permitted by applicable law, Fujitsu Microelectronics Europe GmbH's and its supplier's liability are restricted to intention and gross negligence.

NO LIABILITY FOR CONSEQUENTIAL DAMAGES

To the maximum extent permitted by applicable law, in no event shall Fujitsu Microelectronics Europe GmbH and its suppliers be liable for any damages whatsoever (including but without limitation, consequential and/or indirect damages for personal injury, assets of substantial value, loss of profits, interruption of business operation, loss of information, or any other monetary or pecuniary loss) arising from the use of the Product.

Should one of the above stipulations be or become invalid and/or unenforceable, the remaining stipulations shall stay in full effect

0 Contents

| | |
|---|-----------|
| REVISION HISTORY | 2 |
| WARRANTY AND DISCLAIMER | 3 |
| 0 CONTENTS..... | 4 |
| 1 OVERVIEW..... | 6 |
| 1.1 Abstract..... | 6 |
| 1.2 General Description..... | 7 |
| 1.3 Functional Restrictions | 8 |
| 1.3.1 Valid for EMA-MB91V460A-002B/-80/003 and EMA-MB91FV460B-001.... | 8 |
| 2 INSTALLATION | 9 |
| 3 SWITCHES AND JUMPERS..... | 10 |
| 3.1 Switches and Jumpers overview | 10 |
| 3.1.1 External bus data..... | 10 |
| 3.1.2 Bus control..... | 11 |
| 3.1.3 DMA control..... | 11 |
| 3.1.4 Level Shifter direction / CS / MONCLK | 12 |
| 3.2 Default Jumper Setting | 13 |
| 3.3 MONCLK select (S400-10)..... | 15 |
| 3.4 Level-shifter direction control jumper..... | 15 |
| 3.5 Data bus jumpers (D0-D15)..... | 16 |
| 3.5.1 D0 (P03_0)..... | 16 |
| 3.5.2 D1 (P03_1)..... | 16 |
| 3.5.3 D2 (P03_2)..... | 16 |
| 3.5.4 D3 (P03_3)..... | 16 |
| 3.5.5 D4 (P03_4)..... | 17 |
| 3.5.6 D5 (P03_5)..... | 17 |
| 3.5.7 D6 (P03_6)..... | 17 |
| 3.5.8 D7 (P03_7)..... | 17 |
| 3.5.9 D8 (P02_0)..... | 17 |
| 3.5.10 D9 (P02_1)..... | 18 |
| 3.5.11 D10 (P02_2)..... | 18 |
| 3.5.12 D11 (P02_3)..... | 18 |
| 3.5.13 D12 (P02_4)..... | 19 |
| 3.5.14 D13 (P02_5)..... | 19 |

| | | |
|------------|---|-----------|
| 3.5.15 | D14 (P02_6) | 19 |
| 3.5.16 | D15 (P02_7) | 19 |
| 3.6 | Bus control jumpers | 20 |
| 3.6.1 | CS0# (P09_0) | 20 |
| 3.6.2 | CS1# (P09_1) | 20 |
| 3.6.3 | CS2# (P09_2) | 20 |
| 3.6.4 | CS3# (P09_3) | 20 |
| 3.6.5 | CS6# (P09_6) | 20 |
| 3.6.6 | CS7# (P09_7) | 21 |
| 3.6.7 | AS# (P10_1) | 21 |
| 3.6.8 | RDY (P08_7) | 21 |
| 3.6.9 | BGRNT# (P08_5) | 21 |
| 3.6.10 | BRQ (P08_6) | 21 |
| 3.6.11 | BAA# (P10_2) | 22 |
| 3.6.12 | WE# (P10_3) | 22 |
| 3.7 | DMA jumpers | 22 |
| 3.7.1 | DREQ0 (P13_0) | 22 |
| 3.7.2 | DACK0# (P13_1) | 22 |
| 3.7.3 | DEOP0 (P13_2) | 22 |
| 4 | CPLD | 23 |
| 4.1 | CPLD Verilog Code | 23 |
| 4.2 | CPLD Constraints | 26 |
| 4.3 | CPLD control settings | 27 |
| 4.3.1 | Product revision 1.1 (CPLD revision 7D12) | 27 |
| 4.3.2 | Product revision 1.0 (CPLD revision 7D11) | 28 |
| 4.4 | CPLD programming jumper (J491) | 29 |
| 5 | MECHANICAL DIMENSIONS | 30 |
| 6 | INFORMATION IN THE WWW | 31 |
| 7 | CHINA-ROHS REGULATION | 32 |
| 8 | RECYCLING | 34 |

1 Overview

1.1 Abstract

The EMA-MB91F467D-LS-208M04 in combination with the EMA-MB91V460A-002B/-80/003 or EMA-MB91FV460B-001 is a development system for the Fujitsu FR60 MB91V460 Flash microcontroller.

The EMA-MB91F467D-LS-208M04 is an adapter board with level shifters to support the MB91V460A external bus interface at 3.3V levels.

The development system allows the designer immediately to start with the software development before MB91V460 based silicon samples are available.

**This board must only be used for test applications
in an evaluation laboratory environment.**

Before using the EMA-MB91F467D-LS-208M04 adapter board, make sure that the following packed components have been delivered:

- 1 pcs. EMA-MB91F467D-LS-208M04 socket adapter board
- 1 pcs. YQPACK208SD
- 5 pcs. Screw M2x12
- 5 pcs. Washer M2, Nylon
- 1 pcs. User Guide

Note for SDRAM usage

The EMA-MB91F467D-LS-208M04 supports external SRAM, Flash memory and SDRAM. Please refer to section 4 for further details.

Because of the additional delay of the level shifter the bus clock (CLKT) is limited to 32 MHz while SDRAM is connected to the external bus.

| SDRAM | SRAM | Flash | CLKT restriction |
|-------|------|-------|------------------|
| | | X | No restriction |
| | X | | No restriction |
| | X | X | No restriction |
| X | | X | CLKT <= 32 MHz |
| X | X | | CLKT <= 32 MHz |
| X | X | X | CLKT <= 32 MHz |

1.2 General Description

The EMA-MB91F467D-LS-208M04 in combination with the EMA-MB91V460A-002B/-80/003 or EMA-MB91FV460B-001 replaces a MB91F467D microcontroller. For further details of the EMA-MB91V460A-002B/-80/003 or EMA-MB91FV460B-001 board please refer to the User Guide of the EMA-MB91V460A-002B/-80/003 or EMA-MB91FV460B-001.

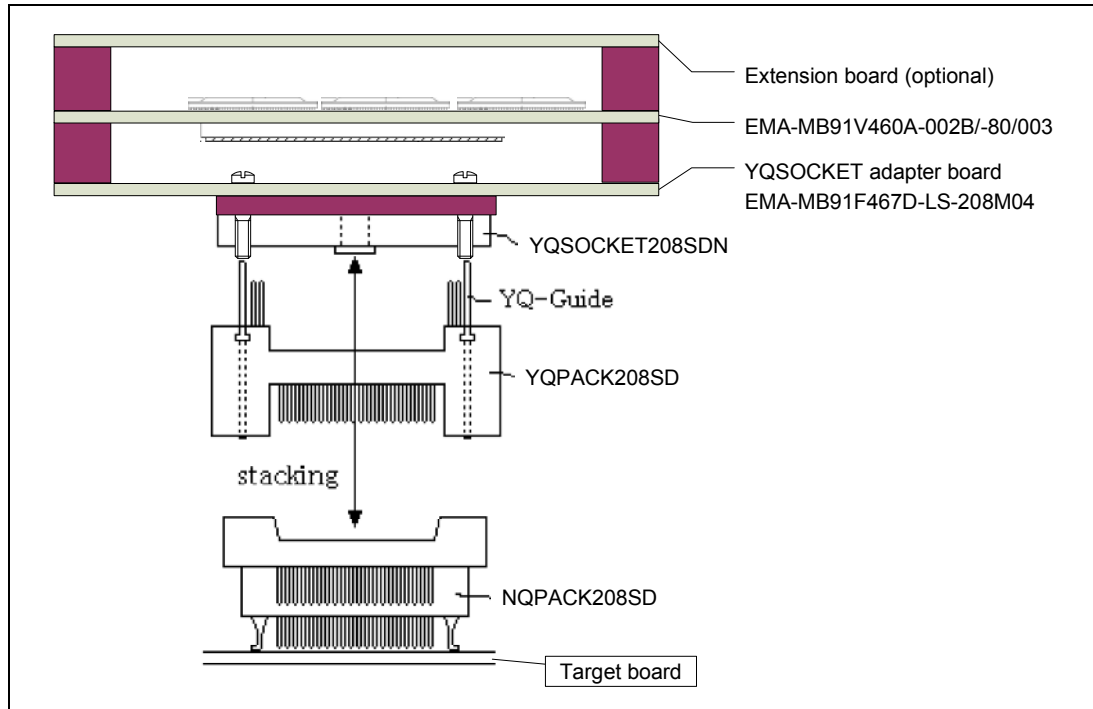


Figure 1-1: System overview

1.3 Functional Restrictions

1.3.1 Valid for EMA-MB91V460A-002B/-80/003 and EMA-MB91FV460B-001

This probe cable can only be used for the following Microcontroller configuration:

1. VDD5 = 5V, VDD35 = 3.3V

The following Microcontroller configurations (2 & 3) are applicable with this probe cable, but it is recommended to use the appropriate MCU "NLS" probe cable!

2. VDD5 = 5V, VDD35 = 5V
3. VDD5 = 3.3V, VDD35 = 3.3V

While using this probe cable, the GPIO functionality on the external bus interface (VDD35 voltage domain) is restricted!

Unused external bus function pins (e.g. address lines) cannot be configured as general purpose in- or output randomly!

The following ports or pin-groups (1-4) can be configured, each as a permanent general purpose input OR output group.

1. P07[0..7]
2. P06[0..7]
3. P05[0..7]
4. P04[0..1], P10.6, P08[0..4]

It is only possible to configure the whole blocks as input OR output!

Configuring each pin of these ports separately as input or output is not applicable!

For details on how to configure the port input and output direction please see chapter 3.4 Level-shifter direction control jumper, chapter 3.5 Data bus jumpers (D0-D7) and chapter 3.6 Data bus jumpers (D8-D15)!

The following pins can be configured as permanent general purpose input OR output separately.

5. P09[0..3], P09[6..7], P10.1, P08.7, P08[5..6], P10[2..3], P13[0..2],
P03[0..7], P02[0..7]

It is possible to configure the pins each as input OR output! Configuring each pin of these ports separately as input or output is applicable by adding or removing certain resistors and jumpers!

For details on how to configure the pins input and output direction please see chapter 3.7 Bus control jumpers and the corresponding schematics.

2 Installation

Remove carefully the EMA-MB91F467D-LS-208M04 board from the shipping carton and check if there are any damages.

Please refer to the attached document “NQPACK/ YQPACK/ HQPACK Technical Information” for installation of the socket adapter.

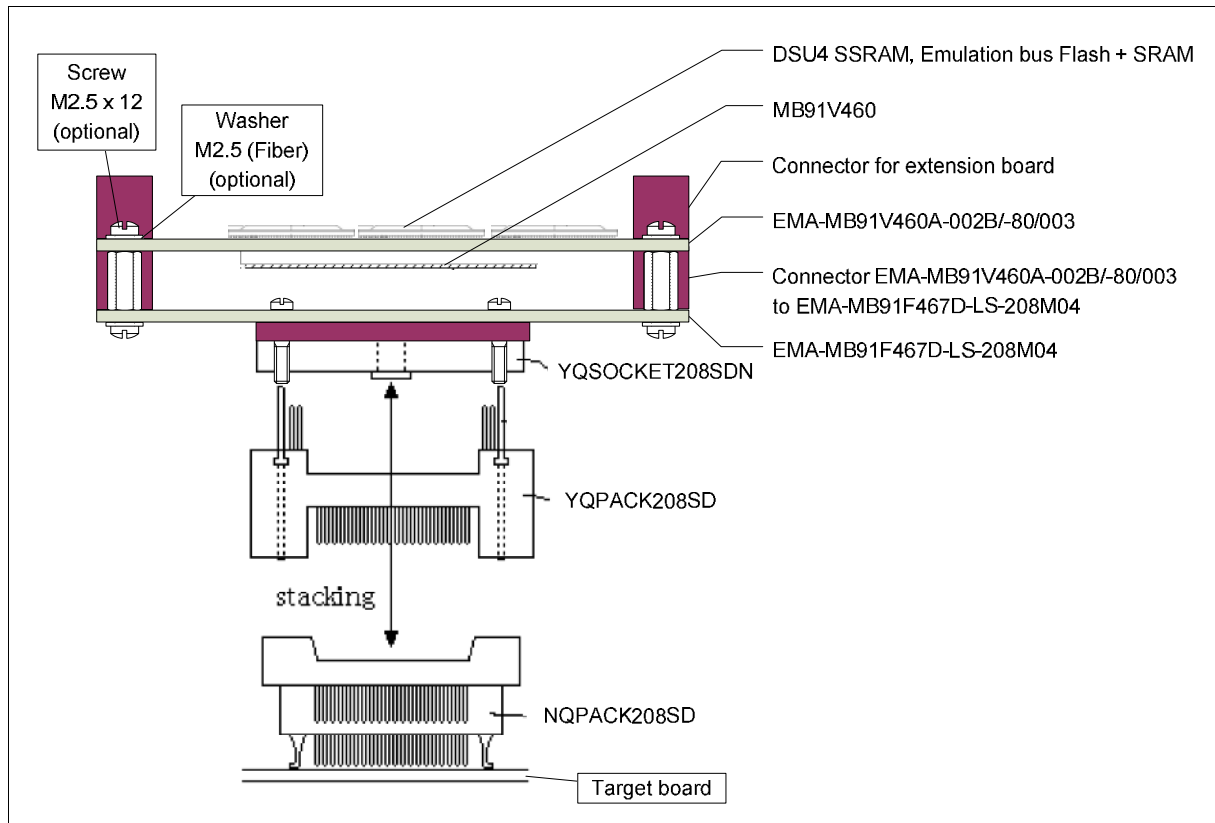


Figure 2-1: Installation

3 Switches and Jumpers

This chapter describes all switches and jumpers that can be modified or accessed on the EMA-MB91F467D-LS-208M04 board. The default setting is shown with a grey shaded area.

3.1 Switches and Jumpers overview

3.1.1 External bus data

| Jumper | Description/ Function | Type | Default |
|--------|-------------------------------------|-------------|---------|
| R400 | P03_0 ⇔ D0, controlled by DIR_U400 | 0603 | Closed |
| R401 | P03_1 ⇔ D1, controlled by DIR_U400 | 0603 | Closed |
| R402 | P03_2 ⇔ D2, controlled by DIR_U400 | 0603 | Closed |
| R403 | P03_3 ⇔ D3, controlled by DIR_U400 | 0603 | Closed |
| R404 | P03_4 ⇔ D4, controlled by DIR_U400 | 0603 | Closed |
| R405 | P03_5 ⇔ D5, controlled by DIR_U400 | 0603 | Closed |
| R406 | P03_6 ⇔ D6, controlled by DIR_U400 | 0603 | Closed |
| R407 | P03_7 ⇔ D7, controlled by DIR_U400 | 0603 | Closed |
| R408 | P02_0 ⇔ D8, controlled by DIR_U401 | 0603 | Closed |
| R409 | P02_1 ⇔ D9, controlled by DIR_U401 | 0603 | Closed |
| R410 | P02_2 ⇔ D10, controlled by DIR_U401 | 0603 | Closed |
| R411 | P02_3 ⇔ D11, controlled by DIR_U401 | 0603 | Closed |
| R412 | P02_4 ⇔ D12, controlled by DIR_U401 | 0603 | Closed |
| R413 | P02_5 ⇔ D13, controlled by DIR_U401 | 0603 | Closed |
| R414 | P02_6 ⇔ D14, controlled by DIR_U401 | 0603 | Closed |
| R415 | P02_7 ⇔ D15, controlled by DIR_U401 | 0603 | Closed |
| J423 | D0 ⇔ P03_0 | Jumper 2pol | Open |
| J422 | D1 ⇔ P03_1 | Jumper 2pol | Open |
| J421 | D2 ⇔ P03_2 | Jumper 2pol | Open |
| J420 | D3 ⇔ P03_3 | Jumper 2pol | Open |
| J419 | D4 ⇔ P03_4 | Jumper 2pol | Open |
| J418 | D5 ⇔ P03_5 | Jumper 2pol | Open |
| J417 | D6 ⇔ P03_6 | Jumper 2pol | Open |
| J416 | D7 ⇔ P03_7 | Jumper 2pol | Open |
| J424 | D8 ⇔ P02_0 | Jumper 2pol | Open |
| J425 | D9 ⇔ P02_1 | Jumper 2pol | Open |
| J426 | D10 ⇔ P02_2 | Jumper 2pol | Open |
| J427 | D11 ⇔ P02_3 | Jumper 2pol | Open |
| J428 | D12 ⇔ P02_4 | Jumper 2pol | Open |
| J429 | D13 ⇔ P02_5 | Jumper 2pol | Open |
| J430 | D14 ⇔ P02_6 | Jumper 2pol | Open |
| J431 | D15 ⇔ P02_7 | Jumper 2pol | Open |

3.1.2 Bus control

| Jumper | Description/ Function | Type | Default |
|--------|-----------------------|-------------|---------|
| R416 | P09_0 ⇔ CS0# | 0603 | Closed |
| R417 | P09_1 ⇔ CS1# | 0603 | Closed |
| R418 | P09_2 ⇔ CS2# | 0603 | Closed |
| R419 | P09_3 ⇔ CS3# | 0603 | Closed |
| R420 | P09_6 ⇔ CS6# | 0603 | Closed |
| R421 | P09_7 ⇔ CS7# | 0603 | Closed |
| R422 | P10_1 ⇔ AS# | 0603 | Closed |
| R423 | P08_7 ⇔ RDY | 0603 | Closed |
| R424 | P08_5 ⇔ BGRNT# | 0603 | Closed |
| R425 | P10_2 ⇔ BAA# | 0603 | Closed |
| R426 | P10_3 ⇔ WE# | 0603 | Closed |
| R427 | P08_6 ⇔ BRQ | 0603 | Closed |
| J439 | P9_0 ⇔ CS0# | Jumper 2pol | Open |
| J440 | P9_1 ⇔ CS1# | Jumper 2pol | Open |
| J441 | P9_2 ⇔ CS2# | Jumper 2pol | Open |
| J442 | P9_3 ⇔ CS3# | Jumper 2pol | Open |
| J443 | P9_6 ⇔ CS6# | Jumper 2pol | Open |
| J444 | P9_7 ⇔ CS7# | Jumper 2pol | Open |
| J445 | P10_1 ⇔ AS# | Jumper 2pol | Open |
| J432 | P08_7 ⇔ RDY | Jumper 2pol | Open |
| J467 | P08_5 ⇔ BGRNT# | Jumper 2pol | Open |
| J469 | P10_2 ⇔ BAA# | Jumper 2pol | Open |
| J470 | P10_3 ⇔ WE# | Jumper 2pol | Open |
| J433 | P08_6 ⇔ BRQ | Jumper 2pol | Open |

3.1.3 DMA control

| Jumper | Description/ Function | Type | Default |
|--------|-----------------------|-------------|---------|
| R456 | P13_1 ⇔ DACK0# | 0603 | Closed |
| R457 | P13_2 ⇔ DEOP0 | 0603 | Closed |
| R458 | P13_0 ⇔ DREQ0 | 0603 | Closed |
| J474 | P13_1 ⇔ DACK0# | Jumper 2pol | Open |
| J475 | P13_2 ⇔ DEOP0 | Jumper 2pol | Open |
| J473 | P13_0 ⇔ DREQ0 | Jumper 2pol | Open |

3.1.4 Level Shifter direction / CS / MONCLK

| Switch | Description/ Function | Type | Default |
|---------|-----------------------|------------|---------|
| S400-1 | Direction U402 | Dip-Switch | On |
| S400-2 | Direction U403 | Dip-Switch | On |
| S400-3 | Direction U406 | Dip-Switch | Off |
| S400-4 | Direction U407 | Dip-Switch | Off |
| S400-5 | Direction U408 | Dip-Switch | Off |
| S400-6 | Direction U409 | Dip-Switch | Off |
| S400-10 | MONCLK | Dip-Switch | On |
| S401-1 | CS select | Dip-Switch | Off |
| S401-2 | | Dip-Switch | Off |
| S401-3 | | Dip-Switch | Off |
| S401-4 | | Dip-Switch | On |
| S401-5 | SDRAM select | Dip-Switch | Off |
| S401-6 | | Dip-Switch | Off |
| S401-7 | | Dip-Switch | Off |
| S401-8 | | Dip-Switch | On |
| S401-9 | Mode U400, U401 | Dip-Switch | Off |

Refer to chapter 4.3 for version differences.

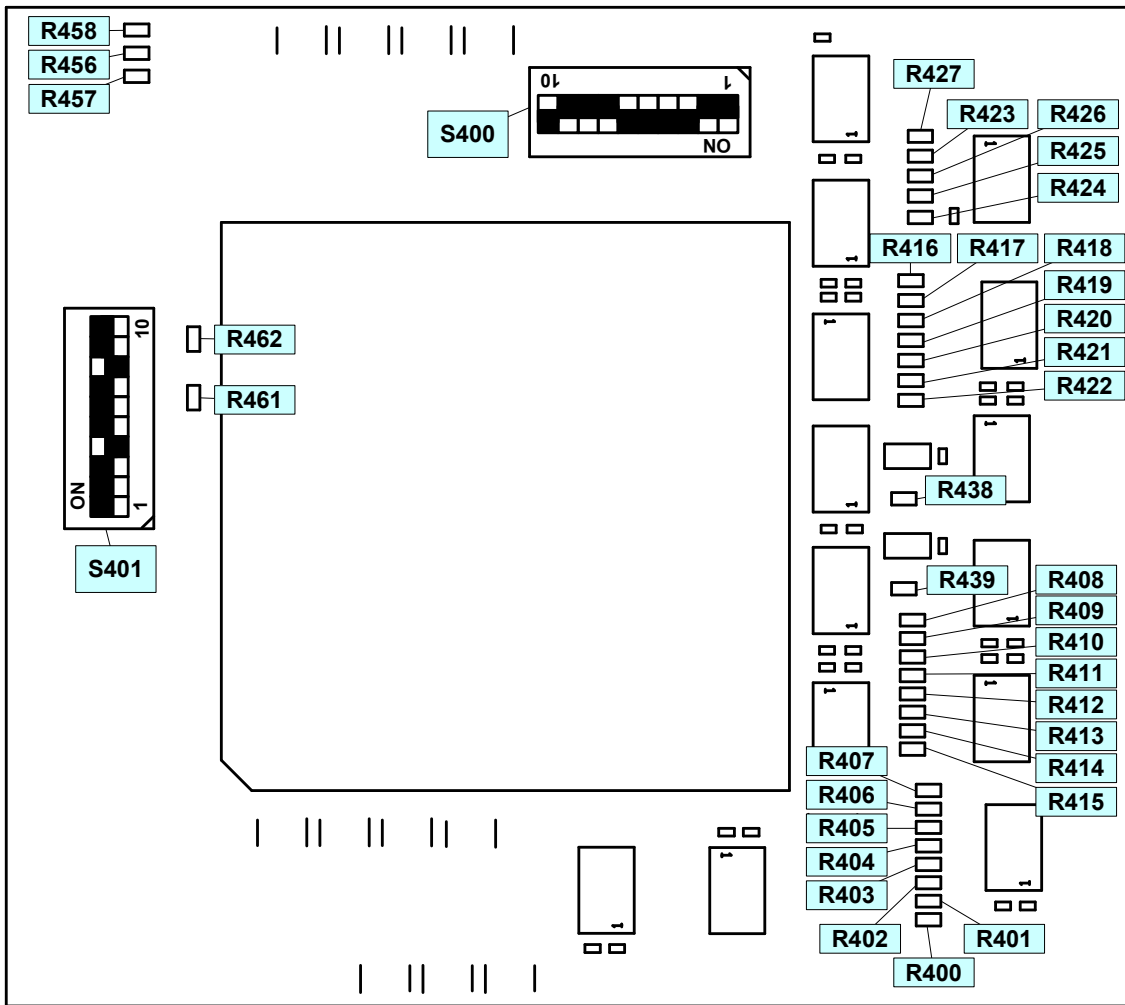


Figure 3-2: Jumper location, bottom. Refer to chapter 4.3 for version differences.

3.3 MONCLK select (S400-10)

| Switch | Setting | Description |
|---------------------|---------|---------------------------------------|
| S400-10 (MONCLK) | OFF | No connection |
| | ON | MONCLK signal connected to the socket |

Default: ON

3.4 Level-shifter direction control jumper

| Jumper | Setting | Description |
|----------------------------|---------|---|
| S400-1 (Direction U402) | ON | Target board D[0..7] ⇔ MB91V460 D[0..7] (check R400..R407 and J416..J423) |
| | OFF | Prohibited |
| S400-2 (Direction U403) | ON | Target board D[8..15] ⇔ MB91V460 D[8..15] (check R408..R415 and J424..J431) |
| | OFF | Prohibited |
| S400-3 (Direction U406) | ON | Target board A[0..7] ⇔ MB91V460 A[0..7] |
| | OFF | Target board A[0..7] ⇐ MB91V460 A[0..7] |
| S400-4 (Direction U407) | ON | Target board A[8..15] ⇔ MB91V460 A[8..15] |
| | OFF | Target board A[8..15] ⇐ MB91V460 A[8..15] |
| S400-5 (Direction U408) | ON | Target board A[16..23] ⇔ MB91V460 A[16..23] |
| | OFF | Target board A[16..23] ⇐ MB91V460 A[16..23] |
| S400-6 (Direction U409) | ON | Target board A[24..25], MCLKE, WR[0..3]#, RD# ⇔ MB91V460 A[24..25], MCLKE, WR[0..3]#, RD# |
| | OFF | Target board A[24..25], MCLKE, WR[0..3]#, RD# ⇐ MB91V460 A[24..25], MCLKE, WR[0..3]#, RD# |

Default: S400-1, S400-2: ON; S400-3 to S400-6: OFF

3.5 Data bus jumpers (D0-D15)

The port P03 and P02 can be used as external bus interface (S401-9: OFF) or as general purpose I/O (S401-9: ON). See chapter 4.3.1.3 for further details.

For the general purpose I/O signals there are different directions selectable by J416 to J431 and R400 to R415.

3.5.1 D0 (P03_0)

| R400 | J423 | Description |
|--------|--------|--------------------------------|
| Closed | Open | P03_0 ⇔ D0 / external bus mode |
| Open | Closed | P03_0 ⇐ D0 |
| Closed | Closed | Prohibited |

Default: R400: Closed, J423: Open

3.5.2 D1 (P03_1)

| R401 | J422 | Description |
|--------|--------|--------------------------------|
| Closed | Open | P03_1 ⇔ D1 / external bus mode |
| Open | Closed | P03_1 ⇐ D1 |
| Closed | Closed | Prohibited |

Default: R401: Closed, J422: Open

3.5.3 D2 (P03_2)

| R402 | J421 | Description |
|--------|--------|--------------------------------|
| Closed | Open | P03_2 ⇔ D2 / external bus mode |
| Open | Closed | P03_2 ⇐ D2 |
| Closed | Closed | Prohibited |

Default: R402: Closed, J421: Open

3.5.4 D3 (P03_3)

| R403 | J420 | Description |
|--------|--------|--------------------------------|
| Closed | Open | P03_3 ⇔ D3 / external bus mode |
| Open | Closed | P03_3 ⇐ D3 |
| Closed | Closed | Prohibited |

Default: R403: Closed, J420: Open

3.5.5 D4 (P03_4)

| R404 | J419 | Description |
|--------|--------|--------------------------------|
| Closed | Open | P03_4 ⇒ D4 / external bus mode |
| Open | Closed | P03_4 ⇐ D4 |
| Closed | Closed | Prohibited |

Default: R404: Closed, J419: Open

3.5.6 D5 (P03_5)

| R405 | J418 | Description |
|--------|--------|--------------------------------|
| Closed | Open | P03_5 ⇒ D5 / external bus mode |
| Open | Closed | P03_5 ⇐ D5 |
| Closed | Closed | Prohibited |

Default: R405: Closed, J418: Open

3.5.7 D6 (P03_6)

| R406 | J417 | Description |
|--------|--------|--------------------------------|
| Closed | Open | P03_6 ⇒ D6 / external bus mode |
| Open | Closed | P03_6 ⇐ D6 |
| Closed | Closed | Prohibited |

Default: R406: Closed, J417: Open

3.5.8 D7 (P03_7)

| R407 | J416 | Description |
|--------|--------|--------------------------------|
| Closed | Open | P03_7 ⇒ D7 / external bus mode |
| Open | Closed | P03_7 ⇐ D7 |
| Closed | Closed | Prohibited |

Default: R407: Closed, J416: Open

3.5.9 D8 (P02_0)

| R408 | J424 | Description |
|--------|--------|--------------------------------|
| Closed | Open | P02_0 ⇒ D8 / external bus mode |
| Open | Closed | P02_0 ⇐ D8 |
| Closed | Closed | Prohibited |

Default: R408: Closed, J424: Open

3.5.10 D9 (P02_1)

| R409 | J425 | Description |
|--------|--------|--------------------------------|
| Closed | Open | P02_1 ⇔ D9 / external bus mode |
| Open | Closed | P02_1 ⇔ D9 |
| Closed | Closed | Prohibited |

Default: R409: Closed, J425: Open

3.5.11 D10 (P02_2)

| R410 | J426 | Description |
|--------|--------|---------------------------------|
| Closed | Open | P02_2 ⇔ D10 / external bus mode |
| Open | Closed | P02_2 ⇔ D10 |
| Closed | Closed | Prohibited |

Default: R410: Closed, J426: Open

3.5.12 D11 (P02_3)

| R411 | J427 | Description |
|--------|--------|---------------------------------|
| Closed | Open | P02_3 ⇔ D11 / external bus mode |
| Open | Closed | P02_3 ⇔ D11 |
| Closed | Closed | Prohibited |

Default: R411: Closed, J427: Open

3.5.13 D12 (P02_4)

| R412 | J428 | Description |
|--------|--------|---------------------------------|
| Closed | Open | P02_4 ⇔ D12 / external bus mode |
| Open | Closed | P02_4 ⇐ D12 |
| Closed | Closed | Prohibited |

Default: R412: Closed, J428: Open

3.5.14 D13 (P02_5)

| R413 | J429 | Description |
|--------|--------|---------------------------------|
| Closed | Open | P02_5 ⇔ D13 / external bus mode |
| Open | Closed | P02_5 ⇐ D13 |
| Closed | Closed | Prohibited |

Default: R413: Closed, J429: Open

3.5.15 D14 (P02_6)

| R414 | J430 | Description |
|--------|--------|---------------------------------|
| Closed | Open | P02_6 ⇔ D14 / external bus mode |
| Open | Closed | P02_6 ⇐ D14 |
| Closed | Closed | Prohibited |

Default: R414: Closed, J430: Open

3.5.16 D15 (P02_7)

| R415 | J431 | Description |
|--------|--------|---------------------------------|
| Closed | Open | P02_7 ⇔ D15 / external bus mode |
| Open | Closed | P02_7 ⇐ D15 |
| Closed | Closed | Prohibited |

Default: R415: Closed, J431: Open

3.6 Bus control jumpers

3.6.1 CS0# (P09_0)

| R416 | J439 | Description |
|--------|--------|--------------|
| Closed | Open | P09_0 ⇒ CS0# |
| Open | Closed | P09_0 ⇐ CS0# |
| Closed | Closed | Prohibited |

Default: R416: Closed, J439: Open

3.6.2 CS1# (P09_1)

| R417 | J440 | Description |
|--------|--------|--------------|
| Closed | Open | P09_1 ⇒ CS1# |
| Open | Closed | P09_1 ⇐ CS1# |
| Closed | Closed | Prohibited |

Default: R417: Closed, J440: Open

3.6.3 CS2# (P09_2)

| R418 | J441 | Description |
|--------|--------|--------------|
| Closed | Open | P09_2 ⇒ CS2# |
| Open | Closed | P09_2 ⇐ CS2# |
| Closed | Closed | Prohibited |

Default: R418: Closed, J441: Open

3.6.4 CS3# (P09_3)

| R419 | J442 | Description |
|--------|--------|--------------|
| Closed | Open | P09_3 ⇒ CS3# |
| Open | Closed | P09_3 ⇐ CS3# |
| Closed | Closed | Prohibited |

Default: R419: Closed, J442: Open

3.6.5 CS6# (P09_6)

| R420 | J443 | Description |
|--------|--------|--------------|
| Closed | Open | P09_6 ⇒ CS6# |
| Open | Closed | P09_6 ⇐ CS6# |
| Closed | Closed | Prohibited |

Default: R420: Closed, J443: Open

3.6.6 CS7# (P09_7)

| R421 | J444 | Description |
|--------|--------|--------------|
| Closed | Open | P09_7 ⇔ CS7# |
| Open | Closed | P09_7 ⇐ CS7# |
| Closed | Closed | Prohibited |

Default: R421: Closed, J444: Open

3.6.7 AS# (P10_1)

| R422 | J445 | Description |
|--------|--------|-------------|
| Closed | Open | P10_1 ⇔ AS# |
| Open | Closed | P10_1 ⇐ AS# |
| Closed | Closed | Prohibited |

Default: R422: Closed, J445: Open

3.6.8 RDY (P08_7)

| R423 | J432 | Description |
|--------|--------|-------------|
| Closed | Open | P08_7 ⇐ RDY |
| Open | Closed | P08_7 ⇔ RDY |
| Closed | Closed | Prohibited |

Default: R423: Closed, J432: Open

3.6.9 BGRNT# (P08_5)

| R424 | J467 | Description |
|--------|--------|----------------|
| Closed | Open | P08_5 ⇔ BGRNT# |
| Open | Closed | P08_5 ⇐ BGRNT# |
| Closed | Closed | Prohibited |

Default: R424: Closed, J467: Open

3.6.10 BRQ (P08_6)

| R427 | J433 | Description |
|--------|--------|-------------|
| Closed | Open | P08_6 ⇐ BRQ |
| Open | Closed | P08_6 ⇔ BRQ |
| Closed | Closed | Prohibited |

Default: R427: Closed, J433: Open

3.6.11 BAA# (P10_2)

| R425 | J469 | Description |
|--------|--------|-------------|
| Closed | Open | P10_2 ⇔ BAA |
| Open | Closed | P10_2 ⇐ BAA |
| Closed | Closed | Prohibited |

Default: R425: Closed, J469: Open

3.6.12 WE# (P10_3)

| R426 | J470 | Description |
|--------|--------|-------------|
| Closed | Open | P10_3 ⇔ WE# |
| Open | Closed | P10_3 ⇐ WE# |
| Closed | Closed | Prohibited |

Default: R426: Closed, J470: Open

3.7 DMA jumpers

3.7.1 DREQ0 (P13_0)

| R458 | J473 | Description |
|--------|--------|---------------|
| Closed | Open | P13_0 ⇐ DREQ0 |
| Open | Closed | P13_0 ⇔ DREQ0 |
| Closed | Closed | Prohibited |

Default: R458: Closed, J473: Open

3.7.2 DACK0# (P13_1)

| R456 | J474 | Description |
|--------|--------|----------------|
| Closed | Open | P13_1 ⇔ DACK0# |
| Open | Closed | P13_1 ⇐ DACK0# |
| Closed | Closed | Prohibited |

Default: R456: Closed, J474: Open

3.7.3 DEOP0 (P13_2)

| R457 | J475 | Description |
|--------|--------|---------------|
| Closed | Open | P13_2 ⇔ DEOP0 |
| Open | Closed | P13_2 ⇐ DEOP0 |
| Closed | Closed | Prohibited |

Default: R457: Closed, J475: Open

4 CPLD

The CPLD Xilinx XC9536XL-5VQL44C controls the direction of the data bus.

4.1 CPLD Verilog Code

```

`timescale 1ns / 1ps
////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
// Company:      Accemic GmbH & Co. KG
// Engineer:     RH / AW
//
// Create Date:  03/03/2007
// Design Name:  EMA-MB91F467D-LS-208M04
// Module Name:  F467D
// Project Name:
// Target Devices: XC9536XL-5VQ44
// Tool versions: ISE 9.2
// Description:
//
// Dependencies:
//
// Revision:
// Revision      1.2
// Additional Comments:
//
// USERCODE:    7D12
//              ||||____ Subversion
//              |||____  Version
//              ||_____ Target 467D
//              **
//
////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////

module EMA_MB91F467D_LS_208M04_V11_cpld_7D12 (
ECSx,
CSx,          // P09_7..P09_0
WRx,          // P08_3..P08_0
RDx,          // P08_4
ASx,          // P10_1
BAAx,         // P10_2
WEx,          // P10_3
IORDx,        // P11_0
IOWRx,        // P11_1
S401,
DIR_U400,
DIR_U401,
DIR_U404,
DIR_U405,
OEx_U400_U401,
OEx_U404_U405);

```

```

input ECSx;
input [7:0] CSx;
input [3:0] WRx;
input RDx;
input ASx;
input BAAx;
input WEx;
input IORDx;
input IOWRx;
input [9:1] S401;
output DIR_U400;
output DIR_U401;
output DIR_U404;
output DIR_U405;
output OEx_U400_U401;
output OEx_U404_U405;

reg OEx_U400_U401, OEx_U404_U405;
reg DIR_U400, DIR_U401, DIR_U404, DIR_U405;

reg SDRAM_SELECTEDx;

always @*
begin
  case (S401[4:1]) // CS_SELECT
    4'hF: // CS0
      OEx_U404_U405 = !ECSx | ( CSx[1] & CSx[2] & CSx[3] & CSx[4]
                               & CSx[5] & CSx[6] & CSx[7]);

    4'hE: // CS1
      OEx_U404_U405 = !ECSx | ( CSx[0] & CSx[2] & CSx[3] & CSx[4]
                               & CSx[5] & CSx[6] & CSx[7]);

    4'hD: // CS2
      OEx_U404_U405 = !ECSx | ( CSx[0] & CSx[1] & CSx[3] & CSx[4]
                               & CSx[5] & CSx[6] & CSx[7]);

    4'hC: // CS3
      OEx_U404_U405 = !ECSx | ( CSx[0] & CSx[1] & CSx[2] & CSx[4]
                               & CSx[5] & CSx[6] & CSx[7]);

    4'hB: // CS4
      OEx_U404_U405 = !ECSx | ( CSx[0] & CSx[1] & CSx[2] & CSx[3]
                               & CSx[5] & CSx[6] & CSx[7]);

    4'hA: // CS5
      OEx_U404_U405 = !ECSx | ( CSx[0] & CSx[1] & CSx[2] & CSx[3]
                               & CSx[5] & CSx[6] & CSx[7]);

    4'h9: // CS6
      OEx_U404_U405 = !ECSx | ( CSx[0] & CSx[1] & CSx[2] & CSx[3]
                               & CSx[4] & CSx[5] & CSx[7]);

    4'h8: // CS7
      OEx_U404_U405 = !ECSx | ( CSx[0] & CSx[1] & CSx[2] & CSx[3]
                               & CSx[4] & CSx[5] & CSx[6]);

    default: // all CS
      OEx_U404_U405 = !ECSx | ( CSx[0] & CSx[1] & CSx[2] & CSx[3]
                               & CSx[4] & CSx[5] & CSx[6] & CSx[7]);

  endcase

  OEx_U400_U401 = OEx_U404_U405 & S401[9];

```



```
case (S401[8:5]) // SDRAM_SELECT
  4'b1111: SDRAM_SELECTEDx = CSx[0];
  4'b1110: SDRAM_SELECTEDx = CSx[1];
  4'b1101: SDRAM_SELECTEDx = CSx[2];
  4'b1100: SDRAM_SELECTEDx = CSx[3];
  4'b1011: SDRAM_SELECTEDx = CSx[4];
  4'b1010: SDRAM_SELECTEDx = CSx[5];
  4'b1001: SDRAM_SELECTEDx = CSx[6];
  4'b1000: SDRAM_SELECTEDx = CSx[7];
  default: SDRAM_SELECTEDx = 1;
endcase

// check schematic for DIR level (different on LS boards)
DIR_U400 = (RDx & (!(SDRAM_SELECTEDx & WEx)) | !S401[9]);
DIR_U401 = (RDx & (!(SDRAM_SELECTEDx & WEx)) | !S401[9]);
DIR_U404 = RDx & (!(SDRAM_SELECTEDx & WEx);
DIR_U405 = RDx & (!(SDRAM_SELECTEDx & WEx);
end
endmodule
```

4.2 CPLD Constraints

```

NET "ASx" LOC = "P13" ;
NET "BAAx" LOC = "P14" ;
NET "CSx<0>" LOC = "P2" ;
NET "CSx<1>" LOC = "P1" ;
NET "CSx<2>" LOC = "P3" ;
NET "CSx<3>" LOC = "P5" ;
NET "CSx<4>" LOC = "P6" ;
NET "CSx<5>" LOC = "P7" ;
NET "CSx<6>" LOC = "P8" ;
NET "CSx<7>" LOC = "P12" ;
NET "DIR_U400" LOC = "P39" | SLEW = FAST ;
NET "DIR_U401" LOC = "P38" | SLEW = FAST ;
NET "DIR_U404" LOC = "P36" | SLEW = FAST ;
NET "DIR_U405" LOC = "P37" | SLEW = FAST ;
NET "ECSx" LOC = "P32" ;
NET "IORDx" LOC = "P18" ;
NET "IOWRx" LOC = "P19" ;
NET "OEx_U400_U401" LOC = "P34" | SLEW = FAST ;
NET "OEx_U404_U405" LOC = "P33" | SLEW = FAST ;
NET "RDx" LOC = "P44" ;
NET "S401<1>" LOC = "P31" ;
NET "S401<2>" LOC = "P30" ;
NET "S401<3>" LOC = "P29" ;
NET "S401<4>" LOC = "P28" ;
NET "S401<5>" LOC = "P27" ;
NET "S401<6>" LOC = "P23" ;
NET "S401<7>" LOC = "P22" ;
NET "S401<8>" LOC = "P21" ;
NET "S401<9>" LOC = "P20" ;
NET "WEx" LOC = "P16" ;
NET "WRx<0>" LOC = "P40" ;
NET "WRx<1>" LOC = "P41" ;
NET "WRx<2>" LOC = "P43" ;
NET "WRx<3>" LOC = "P42" ;

```

4.3 CPLD control settings

Because of the additional delay of the level shifter the bus clock (CLKT) is limited to 32 MHz while SDRAM is connected to the external bus.

4.3.1 Product revision 1.1 (CPLD revision 7D12)

4.3.1.1 CS# mask

Chip select signals, selected by S401-1 to S401-4, will not be routed towards the target hardware! For applications with extension board EMA-MB91V460A-300 or equivalent extension boards, please select and set the corresponding chip select signal (CSx) used for the extension board! Please also refer to the user guide of the extension board and to the settings on the extension board itself.

E.g. EMA-MB91V460A-300 is configured to use chip select CS3, please set S401-4,3,2,1 on EMA-MB91F467D-LS-208M04 to CS3 (OFF, OFF, ON, ON)!

In default setting all chip select signals are routed to the target hardware.

| S401-4 | S401-3 | S401-2 | S401-1 | Description |
|--------|------------|--------|--------|------------------|
| OFF | OFF | OFF | OFF | CS0# is selected |
| OFF | OFF | OFF | ON | CS1# is selected |
| OFF | OFF | ON | OFF | CS2# is selected |
| OFF | OFF | ON | ON | CS3# is selected |
| OFF | ON | OFF | OFF | CS4# is selected |
| OFF | ON | OFF | ON | CS5# is selected |
| OFF | ON | ON | OFF | CS6# is selected |
| OFF | ON | ON | ON | CS7# is selected |
| ON | Don't care | | | None selected |

Default: S401-3..1: OFF, S401-4: ON

4.3.1.2 SDRAM CS select

| S401-8 | S401-7 | S401-6 | S401-5 | Description |
|--------|------------|--------|--------|---------------------------|
| OFF | OFF | OFF | OFF | SDRAM on CS0# is selected |
| OFF | OFF | OFF | ON | SDRAM on CS1# is selected |
| OFF | OFF | ON | OFF | SDRAM on CS2# is selected |
| OFF | OFF | ON | ON | SDRAM on CS3# is selected |
| OFF | ON | OFF | OFF | SDRAM on CS4# is selected |
| OFF | ON | OFF | ON | SDRAM on CS5# is selected |
| OFF | ON | ON | OFF | SDRAM on CS6# is selected |
| OFF | ON | ON | ON | SDRAM on CS7# is selected |
| ON | Don't care | | | No SDRAM |

Default: S401-7..5: OFF, S401-8: ON

Note, the bus clock for SDRAM is limited to 32 MHz.

4.3.1.3 U400, U401 mode

The ports P02 and P03 can be used either as external bus D[15:0] or as bidirectional, general purpose I/Os.

| S401-9 | U400, U401 mode |
|--------|--------------------------|
| ON | General purpose I/O mode |
| OFF | External bus mode |

Default: S401-9: OFF (external bus mode)

4.3.2 Product revision 1.0 (CPLD revision 7D11)

| S401-1 | SDRAM CS# channel |
|--------|--|
| ON | CS6# ⇔ SDRAM, CS7# ⇔ non-SDRAM (SRAM, Flash) |
| OFF | CS7# ⇔ SDRAM, CS6# ⇔ non-SDRAM (SRAM, Flash) |

Default: S401-1: ON (CS6)

4.4 CPLD programming jumper (J491)

The CPLD is re-configurable by programming via J491. Please refer to www.xilinx.com for details and tools for Xilinx CPLD configuration.

| J491 pin | Name |
|----------|------|
| 1 | GND |
| 2 | TDO |
| 3 | TCK |
| 4 | TMS |
| 5 | TDI |
| 6 | VREF |

5 Mechanical dimensions

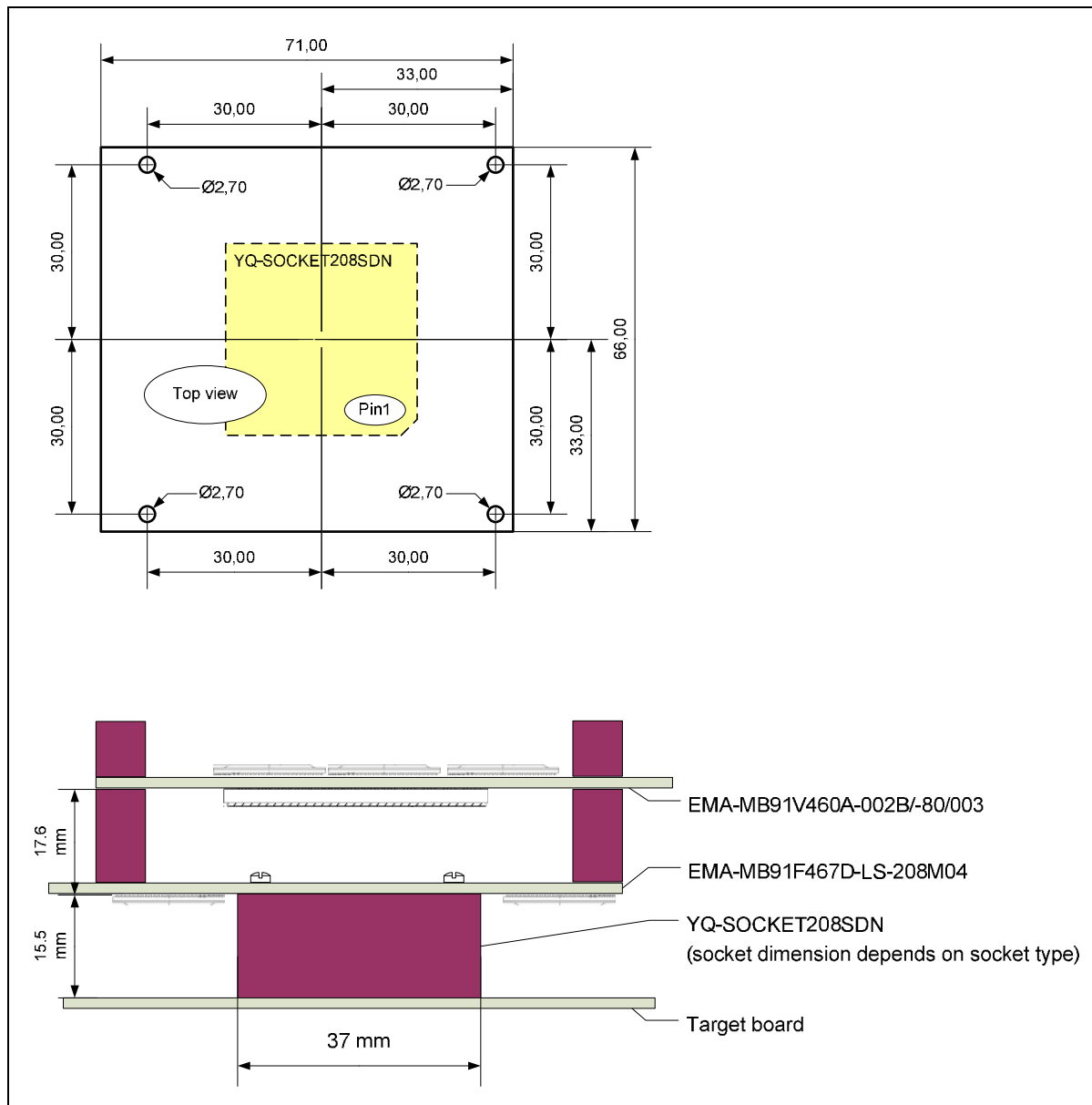


Figure 5-1: Mechanical dimensions

6 Information in the WWW

Information about FUJITSU MICROELECTRONICS Products can be found on the following Internet pages:

Microcontrollers (8-, 16- and 32bit), Graphics Controllers
Datasheets and Hardware Manuals, Support Tools (Hard- and Software)

http://mcu.emea.fujitsu.com/mcu_portal.htm

Linear Products: Power Management, A/D and D/A Converters

<http://www.fujitsu.com/emea/services/microelectronics>

Media Products: SAW filters, acoustic resonators and VCOs

<http://www.fujitsu.com/emea/services/microelectronics/saw>

For more information about FUJITSU MICROELECTRONICS

<http://www.fujitsu.com/emea/services/microelectronics>

7 China-RoHS regulation

Evaluation Board 评估板

Emulation Board 仿真板

根据SJ/T11364-

2006《电子信息产品污染控制标识要求》特提供如下有关污染控制方面的信息。

The following product pollution control information is provided according to SJ/T11364-2006 *Marking for Control of Pollution caused by Electronic Information Products*.

1. 电子信息产品污染控制标志说明 Explanation of Pollution Control Label



该标志表明本产品含有超过中国标准SJ/T11363-

2006《电子信息产品中有毒有害物质的限量要求》中限量的有毒有害物质。标志中的数字为本产品的环保使用期，表明本产品在正常使用的条件下，有毒有害物质不会发生外泄或突变，用户使用本产品不会对环境造成严重污染或对其人身、财产造成严重损害的期限，单位为年。

为保证所声明的环保使用期限，应按产品手册中所规定的环境条件和方法进行正常使用，并严格遵守产品维修手册中规定的定期维修和保养要求。

产品中的消耗件和某些零部件可能有其单独的环保使用期限标志，并且其环保使用期限有可能比整个产品本身的环保使用期限短。应到期按产品维修程序更换那些消耗件和零部件，以保证所声明的整个产品的环保使用期限。

本产品在使用寿命结束时不可作为普通生活垃圾处理，应被单独收集妥善处理。

请注意：环保使用期限50年的指定不是与产品的耐久力，使用期限或任何担保要求等同的。

This symbol to be added to all EIO sold to China, indicates the product contains hazardous materials in excess of the limits established by the Chinese standard SJ/T11363-2006 *Requirements for Concentration Limits for Certain Hazardous Substances in Electronic Information Products*. The number in the symbol is the Environment-friendly Use Period (EFUP), which indicates the period, starting from the manufacturing date, during which the toxic or hazardous substances or elements contained in electronic information products will not leak or mutate under normal operating conditions so that the use of such electronic information products will not result in any severe environmental pollution, any bodily injury or damage to any assets, the unit of the period is "Year".

In order to maintain the declared EFUP, the product shall be operated normally according to the instructions and environmental conditions as defined in the product manual, and periodic maintenance schedules specified in Product Maintenance Procedures shall be followed strictly.

Consumables or certain parts may have their own label with an EFUP value less than the product. Periodic replacement of those consumables or parts to maintain the declared EFUP shall be done in accordance with the Product Maintenance Procedures.

This product must not be disposed of as unsorted municipal waste, and must be collected separately and handled properly after decommissioning.

Please note: The designation of 10 years EFUP is not to be equated with the durability, use-duration or any warranty-claims of the product.

产品中有毒有害物质或元素的名称及含量

Table of hazardous substances name and concentration

| 部件名称 EMA-MB91F467D-LS-208M04 | 有毒有害物质或元素 Hazardous substances name | | | | | |
|---------------------------------|--|-----------|-----------|-----------------|---------------|-----------------|
| | 铅 (Pb) | 汞 (Hg) | 镉 (Cd) | 六价铬 (Cr(VI)) | 多溴联苯 (PBB) | 多溴二苯醚 (PBDE) |
| | x | o | o | o | o | o |

O: 表示该有毒有害物质在该部件所有均质材料中的含量均在SJ/T11363-2006 标准规定的限量要求以下
X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出SJ/T11363-2006 标准规定的限量要求

此表所列数据为发布时所能获得的最佳信息
由于缺少经济上或技术上合理可行的替代物质或方案，此医疗设备运用以上一些有毒有害物质来实现设备的预期临床功能，或给人员或环境提供更好的保护效果。

O: Indicates that this toxic or hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement in SJ/T11363-2006.
X: Indicates that this toxic or hazardous substance contained in at least one of the homogeneous materials used for this part is above the limit requirement in SJ/T11363-2006.
Data listed in the table represents best information available at the time of publication

8 Recycling

Gültig für EU-Länder:

Gemäß der Europäischen WEEE-Richtlinie und deren Umsetzung in landesspezifische Gesetze nehmen wir dieses Gerät wieder zurück.

Zur Entsorgung schicken Sie das Gerät bitte an die folgende Adresse:

Fujitsu Microelectronics Europe GmbH
Warehouse
Monzastraße 4a
63225 Langen

Valid for European Union Countries:

According to the European WEEE-Directive and its implementation into national laws we take this device back.

For disposal please send the device to the following address:

Fujitsu Microelectronics Europe GmbH
Warehouse
Monzastraße 4a
63225 Langen