MAX2839

2.3GHz to 2.7GHz MIMO Wireless Broadband RF Transceiver

General Description

The MAX2839 direct conversion, zero-IF, RF transceiver is designed specifically for 2GHz 802.16e MIMO mobile WiMAX® systems. The device incorporates one transmitter and two receivers, with > 40dB isolation between each receiver. The MAX2839 completely integrates all circuitry required to implement the RF transceiver function, providing RF to baseband receive path, and baseband to RF transmit path, VCO, frequency synthesizer, crystal oscillator, and baseband/control interface. The device includes a fast-settling sigma-delta RF synthesizer with smaller than 40Hz frequency steps and a crystal oscillator that allows the use of a low-cost crystal in place of a TCXO. The transceiver IC also integrates circuits for on-chip DC-offset cancellation, I/Q error, and carrier leakage detection circuits. An internal transmit to receive loopback mode allows for receiver I/Q imbalance calibration. The local oscillator I/Q quadrature phase error can be digitally corrected in approximately 0.125° steps. Only an RF bandpass filter (BPF), crystal, RF switch, PA, and a small number of passive components are needed to form a complete wireless broadband RF radio solution.

The MAX2839 completely eliminates the need for an external SAW filter by implementing on-chip programmable monolithic filters for both the receiver and transmitter, for all 2GHz and 802.16e profiles and WIBRO. The baseband filters along with the Rx and Tx signal paths are optimized to meet the stringent noise figure and linearity specifications. The device supports up to 2048 FFT OFDM and implements programmable channel filters for 3.5MHz to 20MHz RF channel bandwidths. The transceiver requires only 2µs Tx-Rx switching time. The IC is available in a small 56-pin TQFN package measuring 8mm x 8mm x 0.8mm.

Applications

- 802.16e Mobile WiMAX Systems
- Korean WIBRO Systems
- Proprietary Wireless Broadband Systems
- 802.11g or n WLAN with MRC or MIMO Down Link

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Benefits and Features

- 2.3GHz to 2.7GHz Wideband Operation
- Dual Receivers for MIMO, Single Transmitter
- Complete RF Transceiver, PA Driver, and Crystal Oscillator
  - 2.3dB Rx Noise Figure on Each Receiver
  - -35dB Rx EVM for 64QAM Signal
  - 0dBm Linear OFDM Transmit Power (64QAM)
  - -70dBr Tx Spectral Emission Mask
  - -35dBc LO Leakage
  - Automatic Rx DC Offset Correction
  - Monolithic Low-Noise VCO with -39dBc Integrated Phase Noise
  - Programmable Rx I/Q Lowpass Channel Filters
  - Programmable Tx I/Q Lowpass Anti-Aliasing Filters
  - Sigma-Delta Fractional-N PLL with < 40Hz Step
  - 62dB Tx Gain Control Range with 1dB Step Size, Digitally Controlled
  - 95dB Rx Gain Control Range with 1dB Step Size, Digitally Controlled
  - 60dB Analog RSSI Instantaneous Dynamic Range
  - 4-Wire SPI Digital Interface
  - I/Q Analog Baseband Interface
  - Digital Tx/Rx Mode Control
  - Digitally Tuned Crystal Oscillator
  - On-Chip Digital Temperature Sensor Readout
- +2.7V to +3.6V Transceiver Supply
- Low-Power Shutdown Current
- Small, 56-Pin TQFN Package (8mm x 8mm x 0.8mm)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2839ETN+TD	-40°C to +85°C	56 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*
D = Dry pack.

Pin Configuration and Block Diagram/Typical Operating Circuit appear at end of data sheet.

19-3218; Rev 2; 7/15

maxim integrated™

Absolute Maximum Ratings

$V_{CC\_}$ Pins to GND.....-0.3V to +3.6V
RF Inputs: RXINA+, RXINA-, RXINB+, RXINB- to GND.....AC-Coupled Only
RF Outputs: TXOUT+, TXOUT- to GND.....-0.3V to +3.6V
Analog Inputs: TXBBI+, TXBBI-, TXBBQ+, TXBBQ- to GND.....-0.3V to +3.6V
Analog Input: REFCLK, XTAL1.....-0.3V to +3.6V_{P-P}
Analog Outputs: RXBBIA+, RXBBIA-, RXBBQA+, RXBBQA-, RXBBIB+, RXBBIB-, RXBBQB+, RXBBQB-, CPOUT+, CPOUT-, PABIAS, RSSI to GND.....-0.3V to +3.6V
Digital Inputs: RXTX, $\overline{CS}$, SCLK, DIN, B0–B7, LOAD, RXHP, ENABLE to GND.....-0.3V to +3.6V
Digital Outputs: DOUT, CLKOUT .....-0.3V to +3.6V
Bias Voltages: VCOBYP .....-0.3V to +3.6V
Short-Circuit Duration on All Output Pins.....10s
RF Input Power: All RXIN_.....+15dBm
RF Output Differential Load VSWR: All TXOUT.....6:1
Continuous Power Dissipation (T_A = +70°C)
56-Pin TQFN (derate 31.3mW/°C above +70°C).....2500mW
Operating Temperature Range.....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range.....-65°C to +160°C
Lead Temperature (soldering, 10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

DC Electrical Characteristics Table

(MAX2839 Evaluation Kit, $V_{CC\_}$ = 2.7V to 3.6V, T_A = -40°C to +85°C, Rx set to the maximum gain. RXTX set according to operating mode, ENABLE = $\overline{CS}$ = high, SCLK = DIN = low, no input signal at RF inputs, all RF inputs and outputs terminated into 50Ω. 90mV_{RMS} differential I and Q signals (1MHz) applied to I, Q baseband inputs of transmitter in transmit mode, all registers set to recommended settings and corresponding test mode, unless otherwise noted. Typical values are at $V_{CC\_}$ = 2.8V, f_{LO} = 2.5GHz and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	$V_{CC\_}$		2.7		3.6	V
Supply Current	Shutdown mode, T_A = +25°C			2		µA
	Clock-out only mode			1.4	3.5	mA
	Standby mode			32	45	
	Rx mode	One receiver ON		76	95	
		Both receivers ON		117	145	
	Tx mode	16 QAM		116		
		64 QAM (Note 4)		140	170	
	Rx calibration mode, both receivers ON			153	195	
	Tx calibration mode			102	135	
Rx I/Q Output Common-Mode Voltage	D9:D8 = 00 in A4:A0 = 00100		0.85	1.0	1.2	V
	D9:D8 = 01 in A4:A0 = 00100			1.1		
	D9:D8 = 10 in A4:A0 = 00100			1.2		
	D9:D8 = 11 in A4:A0 = 00100			1.35		
Tx Baseband Input Common-Mode Voltage Operating Range	DC-coupled		0.5		1.2	V
Tx Baseband Input Bias Current	Source current			10	20	µA
LOGIC INPUTS: RXTX, ENABLE, SCLK, DIN, $\overline{CS}$, B7:B0, LOAD, RXHP						
Digital Input Voltage High, V_{IH}			V_{CC} - 0.4			V
Digital Input Voltage Low, V_{IL}					0.4	V
Digital Input Current High, I_{IH}			-1		+1	µA

DC Electrical Characteristics Table (continued)

(MAX2839 Evaluation Kit, $V_{CC\_}$ = 2.7V to 3.6V, T_A = -40°C to +85°C, Rx set to the maximum gain. RXTX set according to operating mode, ENABLE = $\overline{CS}$ = high, SCLK = DIN = low, no input signal at RF inputs, all RF inputs and outputs terminated into 50Ω. 90mV_{RMS} differential I and Q signals (1MHz) applied to I, Q baseband inputs of transmitter in transmit mode, all registers set to recommended settings and corresponding test mode, unless otherwise noted. Typical values are at $V_{CC\_}$ = 2.8V, f_{LO} = 2.5GHz and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Input Current Low, I_{IL}		-1		+1	µA
LOGIC OUTPUTS: DOUT, CLKOUT					
Digital Output Voltage High, V_{OH}	Sourcing 100µA	V_{CC} - 0.4			V
Digital Output Voltage Low, V_{OL}	Sinking 100µA			0.4	V

AC Electrical Characteristics Table—Rx MODE

(MAX2839 Evaluation Kit, $V_{CC\_}$ = 2.8V, T_A = +25°C, f_{RF} = 2.4999GHz, f_{LO} = 2.5GHz; baseband output signal frequency = 100kHz, f_{REF} = 40MHz, ENABLE = RXTX = $\overline{CS}$ = high, SCLK = DIN = low, with power matching for the differential RF pins using the typical applications circuit and registers set to default settings and corresponding test mode, unless otherwise noted. Lowpass filter is set to 10MHz RF channel BW. Unmodulated single tone RF input signal is used with specifications which normally apply over the entire operating conditions, unless otherwise indicated.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RF INPUT TO I, Q BASEBAND-LOADED OUTPUT						
RF Input Frequency Range			2.3		2.7	GHz
Peak-to-Peak Gain Variation over RF Input Frequency Range	Tested at band edges and band center			0.8		dB
RF Input Return Loss	All LNA settings			12		dB
Total Voltage Gain	T_A = -40°C to +85°C	Maximum gain, B7:B0 = 0000000	90	99		dB
		Minimum gain, B7:B0 = 1111111		5	13	
RF Gain Steps	From max RF gain to max RF gain - 8dB			8		dB
	From max RF gain to max RF gain - 16dB			16		
	From max RF gain to max RF gain - 32dB			32		
Gain Change Settling Time	Any RF or baseband gain change; gain settling to within ±1dB of steady state; RXHP = 1			200		ns
	Any RF or baseband gain change; gain settling to within ±0.1dB of steady state; RXHP = 1			2000		
Baseband Gain Range	From maximum baseband gain (B5:B0 = 000000) to minimum gain (B5:B0 = 111111), T_A = -40°C to +85°C		58	63	66	dB
Baseband Gain Minimum Step Size				1		dB
DSB Noise Figure	Voltage gain = 65dB with max RF gain (B7:B6 = 00)			2.3		dB
	Voltage gain = 50dB with max RF gain - 8dB (B7:B6 = 01)			5.5		
	Voltage gain = 45dB with max RF gain - 16dB (B7:B6 = 10)			13		
	Voltage gain = 15dB with max RF gain - 32dB (B7:B6 = 11)			27		

AC Electrical Characteristics Table—Rx MODE (continued)

(MAX2839 Evaluation Kit, $V_{CC\_}$ = 2.8V, T_A = +25°C, f_{RF} = 2.4999GHz, f_{LO} = 2.5GHz; baseband output signal frequency = 100kHz, f_{REF} = 40MHz, ENABLE = RXTX = $\overline{CS}$ = high, SCLK = DIN = low, with power matching for the differential RF pins using the typical applications circuit and registers set to default settings and corresponding test mode, unless otherwise noted. Lowpass filter is set to 10MHz RF channel BW. Unmodulated single tone RF input signal is used with specifications which normally apply over the entire operating conditions, unless otherwise indicated.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Out-of-Band Input IP3 (Note 2)	AGC set for -65dBm wanted signal, max RF gain (B7:B6 = 00)			-13		dBm
	AGC set for -55dBm wanted signal, max RF gain - 8dB (B7:B6 = 01)			-9		
	AGC set for -40dBm wanted signal, max RF gain - 16dB (B7:B6 = 10)			-7		
	AGC set for -30dBm wanted signal, max RF gain - 32dB (B7:B6 = 11)			+16		
Inband Input P-1dB	Max RF gain (B7:B6 = 00)			-37		dBm
	Max RF gain - 8dB (B7:B6 = 01)			-29		
	Max RF gain - 16dB (B7:B6 = 01)			-21		
	Max RF gain - 32dB (B7:B6 = 11)			-4		
Maximum Output Signal Level	Over passband frequency range; at any gain setting; 1dB compression point			1.5		V_{P-P}
I/Q Gain Imbalance	100kHz IQ baseband output; 1 σ variation			0.1		dB
I/Q Phase Error	100kHz IQ baseband output; 1 σ variation			0.125		Degrees
Rx I/Q Output Load Impedance (R || C)	Minimum differential resistance		10			kΩ
	Maximum differential capacitance				5	pF
Loopback Gain (for Receiver I/Q Calibration)	Transmitter I/Q input to receiver I/Q output; transmitter B6:B1 = 000011, receiver B5:B0 = 101000 programmed through SPI		-5	0	+5	dB
I/Q Output DC Droop	After switching RXHP to 0; average over 1µs after any gain change, or 2µs after receive enabled with 100Hz AC-coupling			1		V/s
I/Q Static DC Offset	No RF input signal; measure at 3µs after receive enable; RXHP = 1 for 0 to 2µs and set to 0 after 2µs, 1σ variation			2		mV
Isolation Between Rx Channels A and B	Any RF gain settings			40		dB
RECEIVER BASEBAND FILTERS						
Baseband Filter Rejection	At 15MHz			57		dB
	At 20MHz			75		
	At > 40MHz			90		
Baseband Highpass Filter Corner Frequency	RXHP = 1 (used before AGC completion)			650		kHz
	RXHP = 0 (used after AGC completion) address A4:A0 = 01110	D5:D4 = 00		0.1		
		D5:D4 = 01		1		
		D5:D4 = 10		30		
		D5:D4 = 11		100		

AC Electrical Characteristics Table—Rx MODE (continued)

(MAX2839 Evaluation Kit, $V_{CC\_}$ = 2.8V, T_A = +25°C, f_{RF} = 2.4999GHz, f_{LO} = 2.5GHz; baseband output signal frequency = 100kHz, f_{REF} = 40MHz, ENABLE = RXTX = $\overline{CS}$ = high, SCLK = DIN = low, with power matching for the differential RF pins using the typical applications circuit and registers set to default settings and corresponding test mode, unless otherwise noted. Lowpass filter is set to 10MHz RF channel BW. Unmodulated single tone RF input signal is used with specifications which normally apply over the entire operating conditions, unless otherwise indicated.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RF Channel BW Supported by Baseband Filter	A4:A0 = 00100 serial bits D9:D6 = 0000			1.75		MHz
	A4:A0 = 00100 serial bits D9:D6 = 0001			2.25		
	A4:A0 = 00100 serial bits D9:D6 = 0010			3.5		
	A4:A0 = 00100 serial bits D9:D6 = 0011			5.0		
	A4:A0 = 00100 serial bits D9:D6 = 0100			5.5		
	A4:A0 = 00100 serial bits D9:D6 = 0101			6.0		
	A4:A0 = 00100 serial bits D9:D6 = 0110			7.0		
	A4:A0 = 00100 serial bits D9:D6 = 0111			8.0		
	A4:A0 = 00100 serial bits D9:D6 = 1000			9.0		
	A4:A0 = 00100 serial bits D9:D6 = 1001			10.0		
	A4:A0 = 00100 serial bits D9:D6 = 1010			12.0		
	A4:A0 = 00100 serial bits D9:D6 = 1011			14.0		
	A4:A0 = 00100 serial bits D9:D6 = 1100			15.0		
	A4:A0 = 00100 serial bits D9:D6 = 1101			20.0		
	A4:A0 = 00100 serial bits D9:D6 = 1110			24.0		
	A4:A0 = 00100 serial bits D9:D6 = 1111			28.0		
Baseband Gain Ripple	0 to 2.3MHz for BW = 5MHz			1.3		dB_{P-P}
	0 to 4.6MHz for BW = 10MHz			1.3		
Baseband Group Delay Ripple	0 to 2.3MHz for BW = 5MHz			90		ns_{P-P}
	0 to 4.6MHz for BW = 10MHz			50		
Baseband Filter Rejection for 5MHz RF Channel BW	At 3.3MHz			6		dB
	At > 21MHz			85		
Baseband Filter Rejection for 10MHz RF Channel BW	At 6.7MHz			6		dB
	At > 41.6MHz			85		
RSSI						
RSSI Minimum Output Voltage	R_{LOAD} ≥ 10kΩ			0.4		V
RSSI Maximum Output Voltage	R_{LOAD} ≥ 10kΩ			2.2		V
RSSI Slope				30		mV/dB
RSSI Output Settling Time	To within 3dB of steady state	+32dB signal step		200		ns
		-32dB signal step		800		

AC Electrical Characteristics Table—Tx MODE

(MAX2839 Evaluation Kit, $V_{CC\_}$ = 2.8V, T_A = +25°C, f_{RF} = 2.501GHz, f_{LO} = 2.5GHz, f_{REF} = 40MHz, ENABLE = $\overline{CS}$ = high, RXTX = SCLK = DIN = low, with power matching for the differential RF pins using the typical applications and registers set to default settings and corresponding test mode, unless otherwise noted. Lowpass filter is set to 10MHz RF channel BW. 1MHz 90mV_{RMS} cosine and sine signals applied to I/Q baseband inputs of transmitter (differential DC coupled)). (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Tx BASEBAND I/Q INPUTS TO RF OUTPUTS					
RF Output Frequency Range		2.3		2.7	GHz
Peak-to-Peak Peak Gain Variation over RF Band	Output optimally matched over 200MHz RF BW		2.5		dB
Total Voltage Gain	Max gain -3dB; at unbalanced 50Ω matched output		12		dB
Max Output Power over Frequency for Any Given 200MHz Band	64 QAM OFDM signal conforming to spectral emission mask and -36dB EVM after I/Q imbalance calibration by modem (Note 3)		0		dBm
RF Output Return Loss	Given 200MHz band in the 2.3GHz to 2.7GHz range, for which the matching has been optimized		8		dB
RF Gain Control Range	B6:B1 = 000000 to 111111		62		dB
Unwanted Sideband Suppression	Without calibration by modem, and excludes modem I/Q imbalance; P_{OUT} = 0dBm		45		dBc
RF Gain Control Binary Weights	B1		1		
	B2		2		
	B3		4		
	B4		8		
	B5		16		
	B6		32		
Carrier Leakage	Relative to 0dBm output power; without calibration by modern		-35		dBc
Tx I/Q Input Impedance (R||C)	Differential resistance		100		kΩ
	Differential capacitance		0.5		pF
Baseband Frequency Response for 5MHz RF Channel BW	0 to 2.3MHz		0.2		dB
	At > 25MHz		80		
Baseband Frequency Response for 10MHz RF Channel BW	0 to 4.6MHz		0.2		dB
	At > 41.6MHz		80		
Baseband Group Delay Ripple	0 to 2.3MHz (BW = 5MHz)		20		ns
	0 to 4.6MHz (BW = 10MHz)		12		

AC Electrical Characteristics Table—Frequency Synthesis

(MAX2839 Evaluation Kit, $V_{CC\_}$ = 2.8V, T_A = +25°C, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, PLL 3dB loop noise bandwidth = 120kHz. VCO and RF synthesis enabled, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RF Channel Center Frequency Range		2.3		2.7	GHz
Channel Center Frequency Programming Minimum Step Size			39		Hz
Charge-Pump Comparison Frequency		11	40		MHz
Reference Frequency Range		11	40	80	MHz
Reference Frequency Input Levels	AC-coupled to REFCLK pin	0.8			V_{P-P}
Reference Frequency Input Impedance (R||C)	Resistance (REFCLK pin)		10		kΩ
	Capacitance (REFCLK pin)		1		pF
Programmable Reference Divider Values		1	2	4	
Closed-Loop Integrated Phase Noise	Integrate phase noise from 200Hz to 5MHz; charge-pump comparison frequency = 40MHz		-39		dBc
Charge-Pump Output Current	On each differential side		0.8		mA
Close-In Spur Level	f_{OFFSET} = 0 to 1.8MHz		-40		dBc
	f_{OFFSET} = 1.8MHz to 7MHz		-70		
	f_{OFFSET} > 7MHz		-80		
Reference Spur Level			-85		dBc
Turnaround LO Frequency Error	Relative to steady state; measured 35µs after Tx-Rx or Rx-Tx switching instant, and 4µs after any receiver gain changes		±50		Hz
Temperature Range Over Which VCO Maintains Lock	Relative to the ambient temperature T_A, as long as the VCO lock temperature range is within operating temperature range		T_A ±40		°C
Reference Output Clock Divider Values			2		
Output Clock Drive Level	20MHz output, 1x drive setting		1.5		V_{P-P}
Output Clock Load Impedance (R||C)	Resistance		10		kΩ
	Capacitance		2		pF

AC Electrical Characteristics Table—Miscellaneous Blocks

(MAX2839 Evaluation Kit, V_{CC} = 2.8V, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PA BIAS DAC: VOLTAGE MODE						
Output High level	10mA source current			V_{CC} - 0.1		V
Output Low level	100µA sink current			0.1		V
Turn-On Time	Excludes programmable delay of 0 to 7µs in steps of 0.5µs			200		ns
CRYSTAL OSCILLATOR						
On-Chip Tuning Capacitance Range	Maximum capacitance, A4:A0 = 11000, D6:D0 = 1111111			15.5		pF
	Minimum capacitance, A4:A0 = 11000, D6:D0 = 0000000			0.5		
On-Chip Tuning Capacitance Step Size				0.12		pF
ON-CHIP TEMPERATURE SENSOR						
Digital Output Code	Readout at DOUT pin through SPI A4:A0 = 01011, D4:D0	T_A = +25°C		01111		
		T_A = +85°C		11101		
		T_A = -40°C		00001		

AC Electrical Characteristics Table—Timing

(MAX2839 Evaluation Kit, $V_{CC\_}$ = 2.8V, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, 3dB PLL noise bandwidth = 120kHz, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SYSTEM TIMING							
Turnaround Time		Measured from Tx or Rx enable edge; signal settling to within 2dB of steady state	Rx to Tx		2		µs
			Tx to Rx, RXHP = 1		2		
Tx Turn-On Time (from Standby Mode)		Measured from Tx-enable edge; signal settling to within 2dB of steady state			2		µs
Tx Turn-Off Time (to Standby Mode)		From Tx-disable edge			0.1		µs
Rx Turn-On Time (from Standby Mode)		Measured from Rx-enable edge; signal settling to within 2dB of steady state			2		µs
Rx Turn-Off Time (to Standby Mode)		From Rx-disable edge			0.1		µs
TRANSMITTER AND RECEIVER PARALLEL GAIN CONTROL							
LOAD Rising Edge Setup Time		B7:B0 stable to LOAD rising edge			10		ns
LOAD Rising Edge Hold Time		LOAD rising edge to B7:B0 stable			10		ns

AC Electrical Characteristics Table—Timing (continued)

(MAX2839 Evaluation Kit, $V_{CC\_}$ = 2.8V, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, 3dB PLL noise bandwidth = 120kHz, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOAD Falling Edge Setup Time		B7:B0 stable to LOAD falling edge		10		ns
LOAD Falling Edge Hold Time		LOAD falling edge to B7:B0 stable		10		ns
LOAD Rise and Fall Time		Between 10% and 90% of static levels		100		ns
4-WIRE SERIAL PARALLEL INTERFACE TIMING (see Figure 1)						
SCLK Rising Edge to $\overline{CS}$ Falling Edge Wait Time	t_{CSO}			6		ns
Falling Edge of $\overline{CS}$ to Rising Edge of First SCLK Time	t_{CSS}			6		ns
DIN to SCLK Setup Time	t_{DS}			6		ns
DIN to SCLK Hold Time	t_{DH}			6		ns
SCLK Pulse-Width High	t_{CH}			6		ns
SCLK Pulse-Width Low	t_{CL}			6		ns
Last Rising Edge of SCLK to Rising Edge of $\overline{CS}$ or Clock to Load Enable Setup Time	t_{CSH}			6		ns
$\overline{CS}$ High Pulse Width	t_{CSW}			20		ns
Time Between Rising Edge of $\overline{CS}$ and the Next Rising Edge of SCLK	t_{CS1}			6		ns
Clock Frequency	f_{CLK}				45	MHz
Rise Time	t_R			$0.1/f_{CLK}$		ns
Fall Time	t_F			$0.1/f_{CLK}$		ns
SCLK Falling Edge to Valid DOUT	t_D			12.5		ns

Note 1: Min/max limits are production tested at T_A = +85°C. Min/max limits at T_A = -40°C and T_A = +25°C are guaranteed by design and characterization. The power-on register settings are not production tested. Load register setting 500ns after V_{CC} is applied.

Note 2: Two tones at +20MHz and +39MHz offset with -35dBm/tone. Measure IM3 at 1MHz.

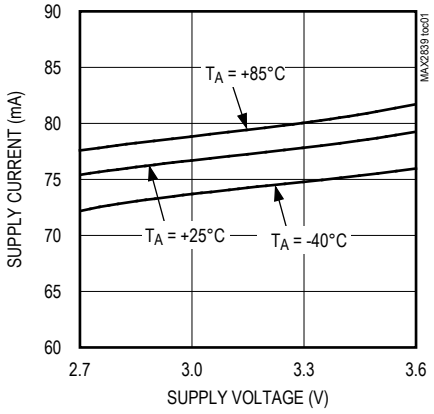
Note 3: Gain adjusted over max gain and max gain -3dB. Optimally matched over given 200MHz band.

Note 4: Tx mode supply current is specified for 64 QAM while achieving the Tx output spectrum mask shown in the *Typical Operating Characteristics*. The supply current can be reduced for 16 QAM signal by adjusting the Tx bias settings through the SPI.

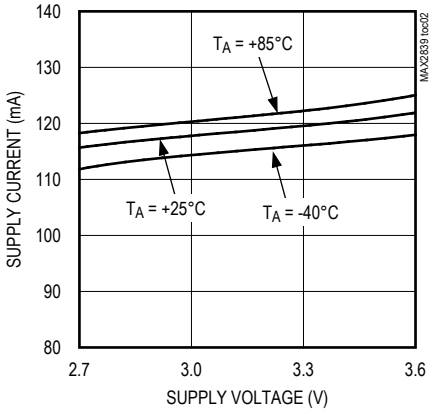
Typical Operating Characteristics

(V_{CC} = 2.8V, T_A = +25°C, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2839 Evaluation Kit.)

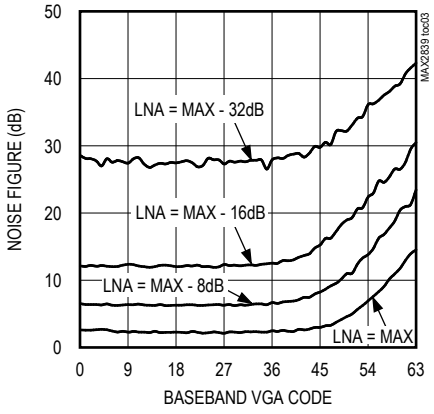
SINGLE RX SUPPLY CURRENT vs. SUPPLY VOLTAGE



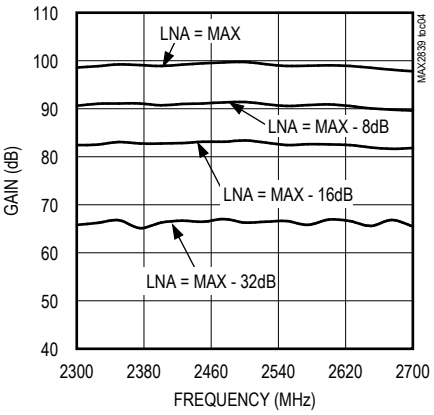
DUAL RX SUPPLY CURRENT vs. SUPPLY VOLTAGE



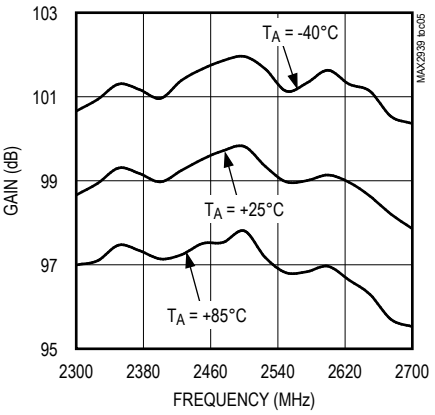
NOISE FIGURE vs. BASEBAND GAIN SETTING



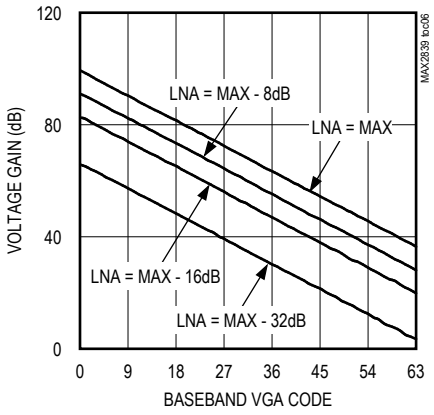
RX VOLTAGE GAIN vs. FREQUENCY



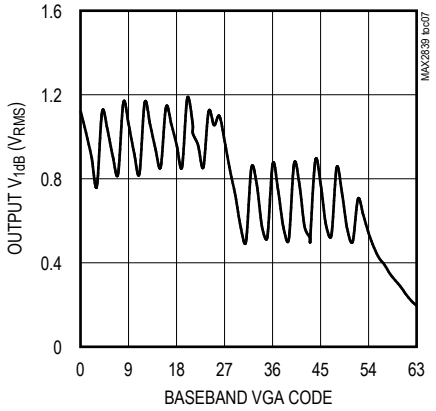
RX VOLTAGE GAIN vs. FREQUENCY (MAXIMUM LNA GAIN)



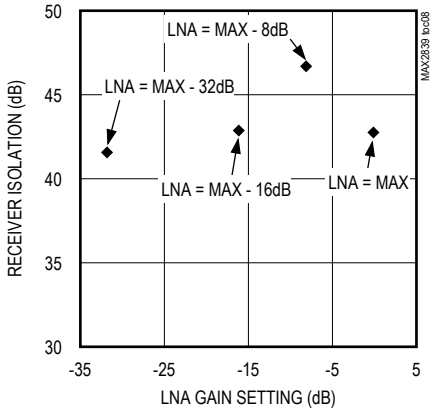
RX VOLTAGE GAIN vs. BASEBAND GAIN SETTING



RX OUTPUT V_{1dB} vs. GAIN SETTING



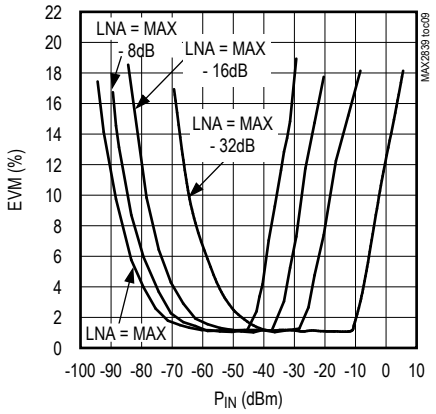
RX ISOLATION vs. LNA GAIN SETTING



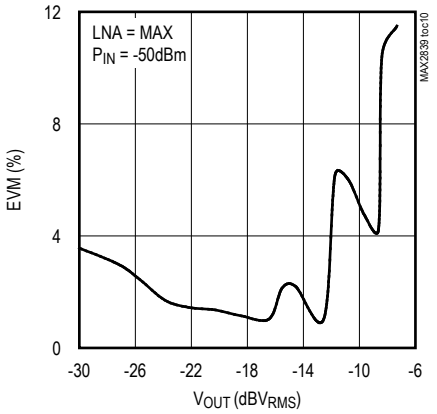
Typical Operating Characteristics (continued)

(V_{CC} = 2.8V, T_A = +25°C, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2839 Evaluation Kit.)

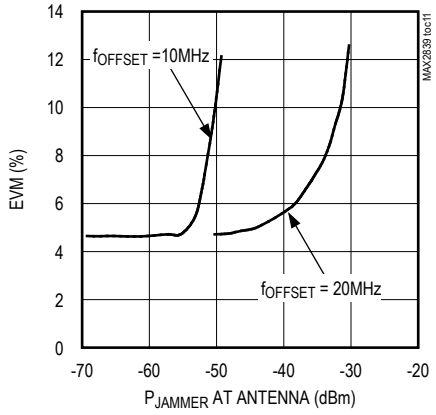
RX EVM vs. P_{IN} (CHANNEL BANDWIDTH = 10MHz, 64 QAM FUSC)



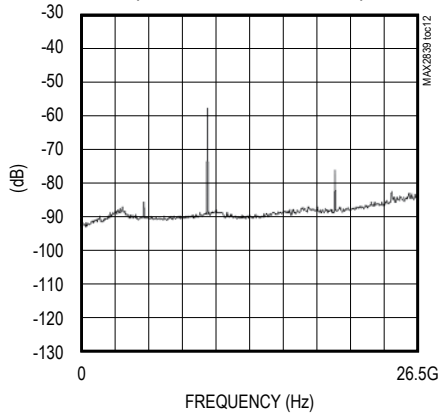
RX EVM vs. V_{OUT} (CHANNEL BANDWIDTH = 10MHz, 64 QAM FUSC)



WiMAX EVM vs. OFDM JAMMER (10MHz CHANNEL BANDWIDTH, 64 QAM FUSC) P_{WANTED} = $P_{SENSITIVITY}$ + 3dB = -70.3dBm AT ANTENNA (INCLUDING 4dB FRONT-END LOSS). EVM AT $P_{SENSITIVITY}$ = 6.37%, WITHOUT JAMMER.



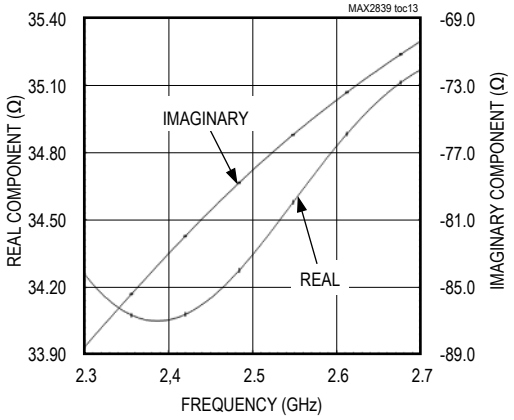
RX EMISSION SPECTRUM AT LNA INPUT (TX OFF, LNA GAIN = MAX)



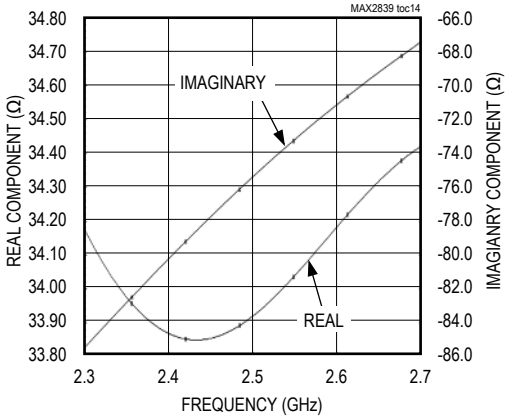
Typical Operating Characteristics (continued)

(V_{CC} = 2.8V, T_A = +25°C, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2839 Evaluation Kit.)

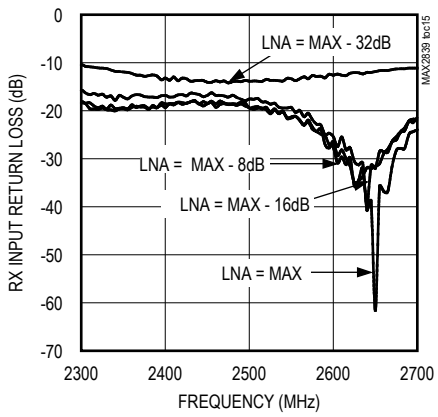
RX A INPUT DIFFERENTIAL IMPEDANCE vs. FREQUENCY



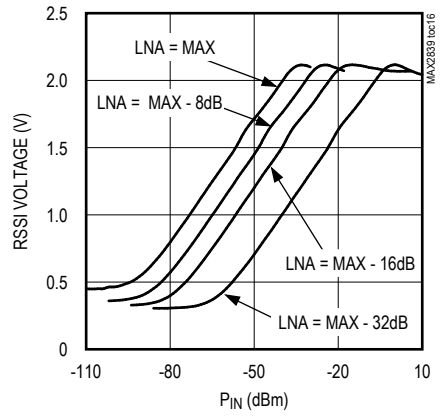
RX B INPUT DIFFERENTIAL IMPEDANCE vs. FREQUENCY



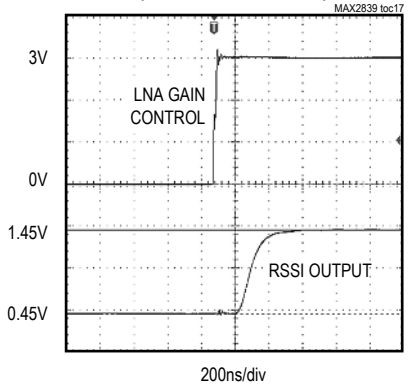
RX INPUT RETURN LOSS vs. FREQUENCY



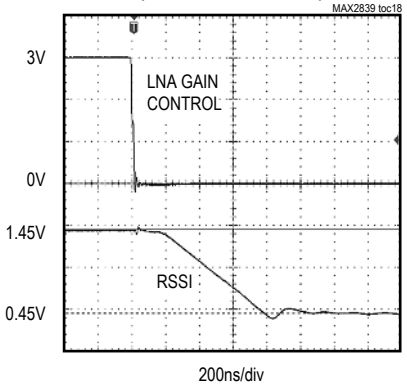
RSSI VOLTAGE vs. INPUT POWER



RX RSSI STEP RESPONSE (+32dB SIGNAL STEP)



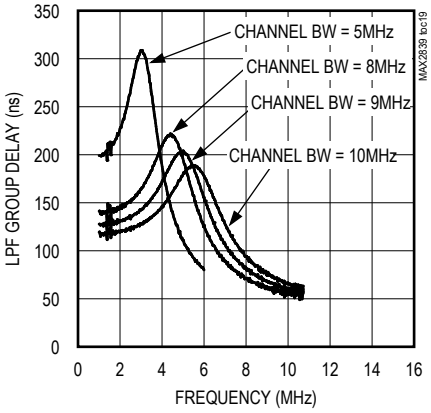
RX RSSI STEP RESPONSE (-32dB SIGNAL STEP)



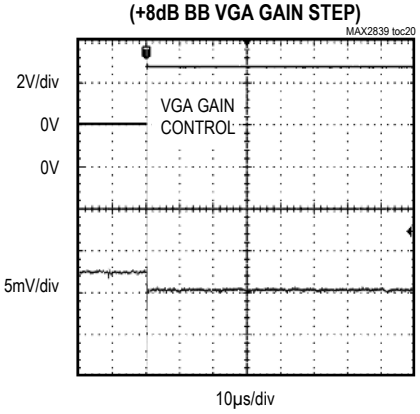
Typical Operating Characteristics (continued)

(V_{CC} = 2.8V, T_A = +25°C, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2839 Evaluation Kit.)

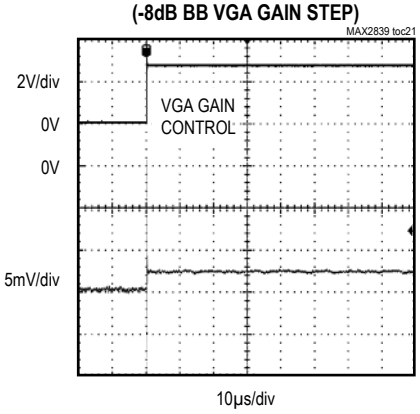
RX LPF GROUP DELAY vs. FREQUENCY



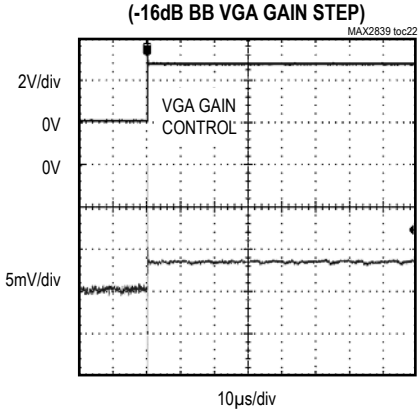
RX DC OFFSET SETTLING RESPONSE (+8dB BB VGA GAIN STEP)



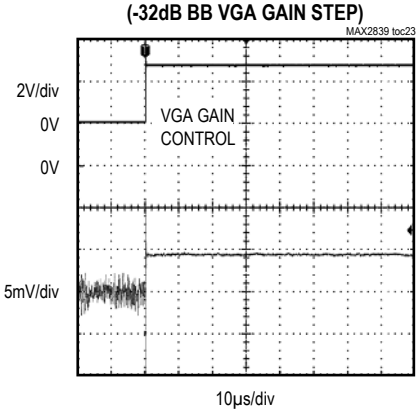
RX DC OFFSET SETTLING RESPONSE (-8dB BB VGA GAIN STEP)



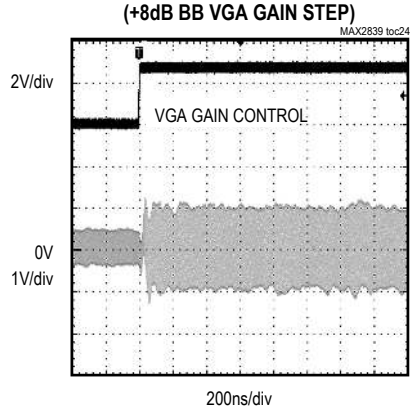
RX DC OFFSET SETTLING RESPONSE (-16dB BB VGA GAIN STEP)



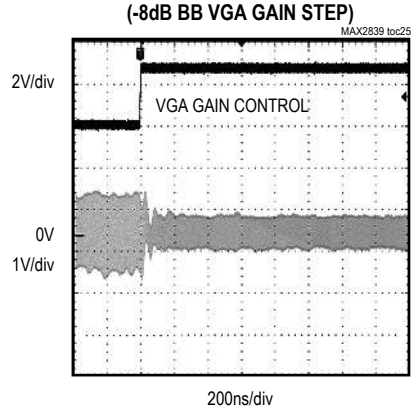
RX DC OFFSET SETTLING RESPONSE (-32dB BB VGA GAIN STEP)



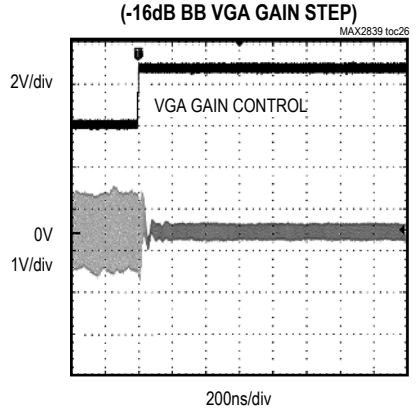
RX BB VGA SETTLING RESPONSE (+8dB BB VGA GAIN STEP)



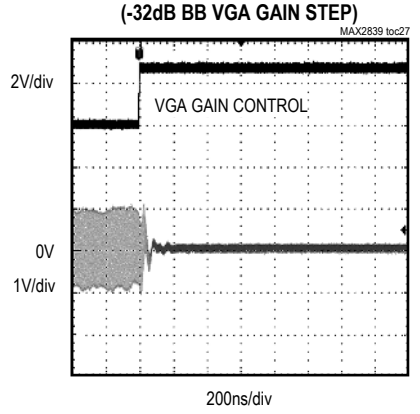
RX BB VGA SETTLING RESPONSE (-8dB BB VGA GAIN STEP)



RX BB VGA SETTLING RESPONSE (-16dB BB VGA GAIN STEP)



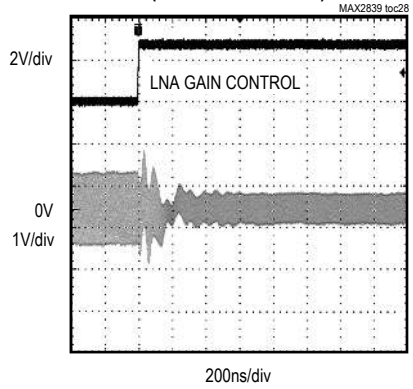
RX BB VGA SETTLING RESPONSE (-32dB BB VGA GAIN STEP)



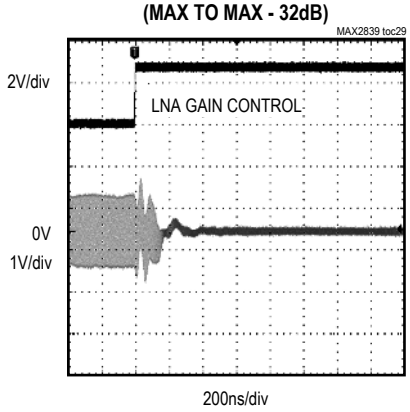
Typical Operating Characteristics (continued)

(V_{CC} = 2.8V, T_A = +25°C, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2839 Evaluation Kit.)

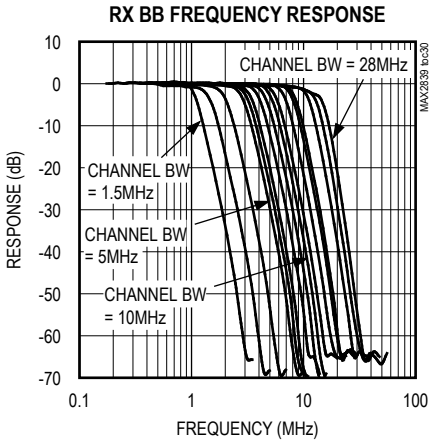
RX LNA SETTLING RESPONSE (MAX TO MAX - 8dB)



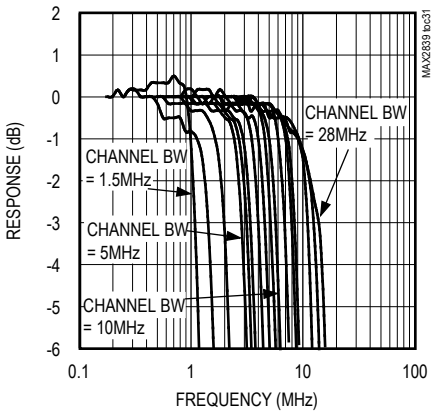
RX LNA SETTLING RESPONSE (MAX TO MAX - 32dB)



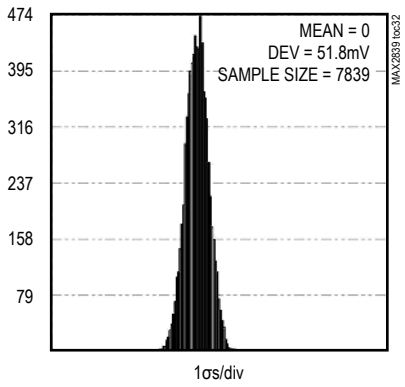
RX BB FREQUENCY RESPONSE



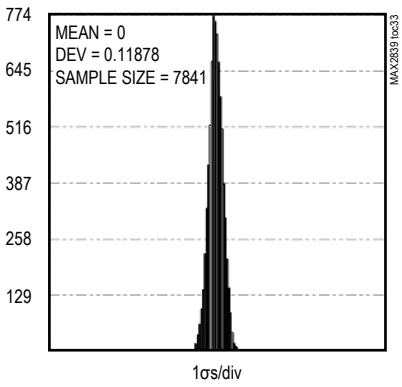
RX BB FREQUENCY RESPONSE



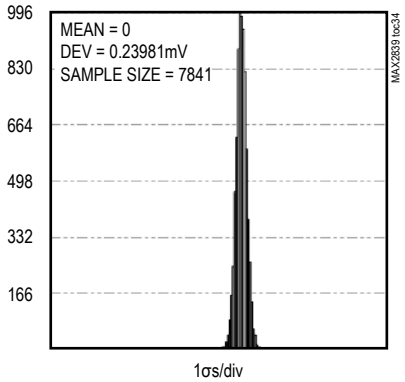
HISTOGRAM: IQ GAIN IMBALANCE



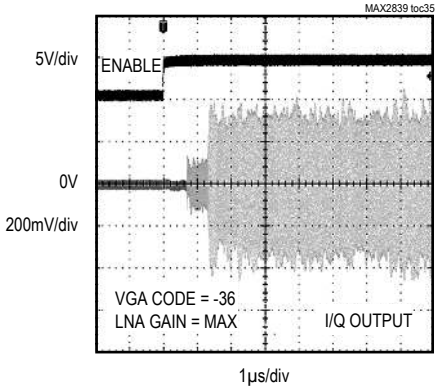
HISTOGRAM: RX PHASE IMBALANCE



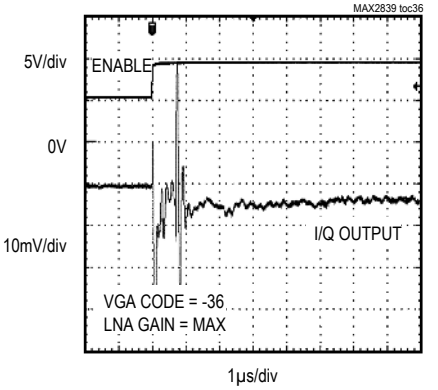
HISTOGRAM: RX STATIC DC OFFSET



POWER-ON DC OFFSET CANCELLATION WITH INPUT SIGNAL



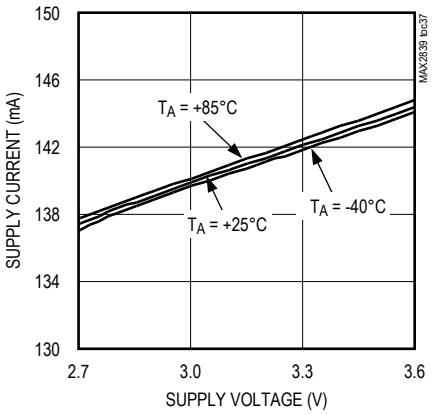
POWER-ON DC OFFSET CANCELLATION WITHOUT INPUT SIGNAL



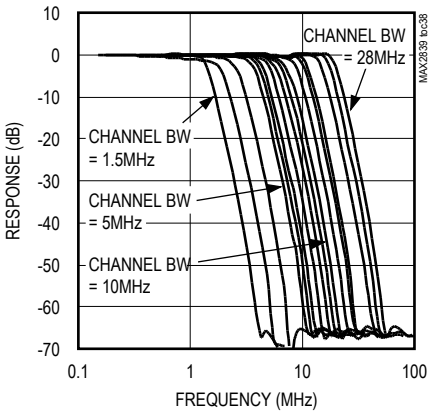
Typical Operating Characteristics (continued)

(V_{CC} = 2.8V, T_A = +25°C, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2839 Evaluation Kit.)

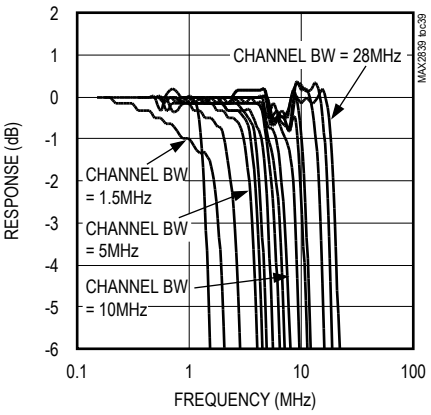
TX SUPPLY CURRENT vs. SUPPLY VOLTAGE



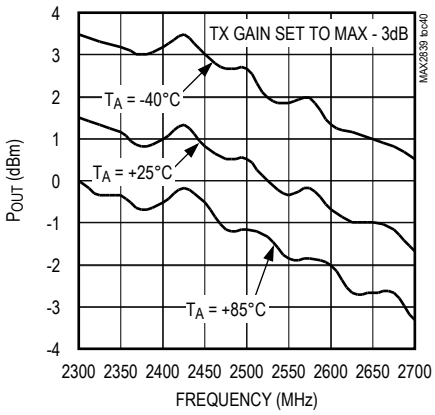
TX BASEBAND FREQUENCY RESPONSE



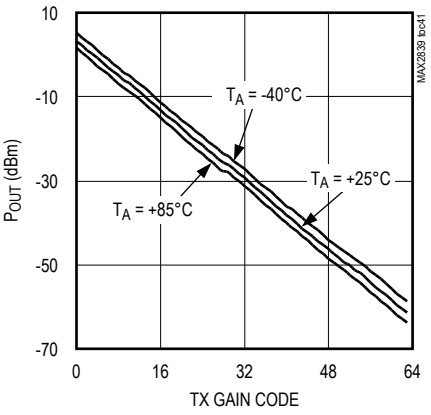
TX BASEBAND FREQUENCY RESPONSE



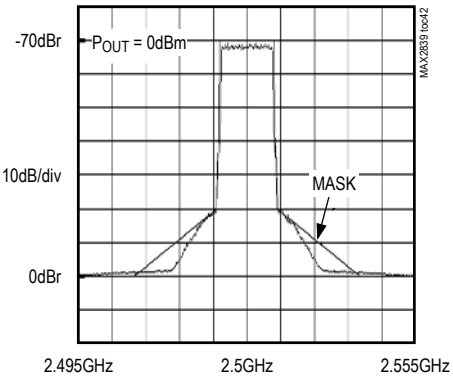
TX OUTPUT POWER vs. FREQUENCY



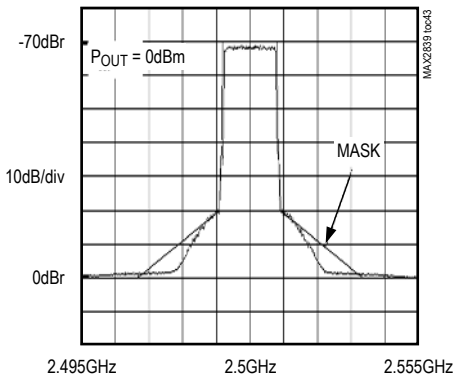
TX OUTPUT POWER vs. GAIN SETTING



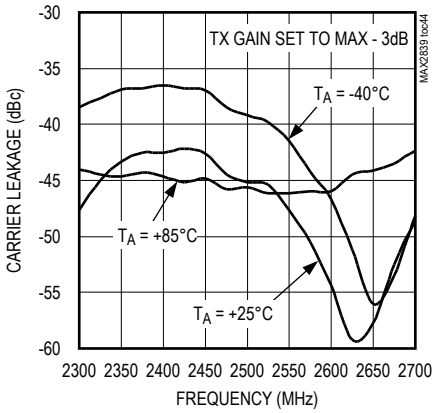
TX OUTPUT SPECTRUM (10MHz CHANNEL BANDWIDTH, 16 QAM FUSC)



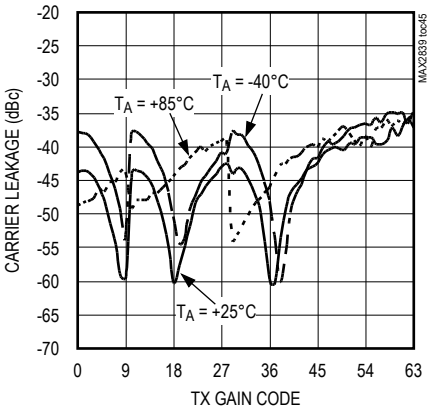
TX OUTPUT SPECTRUM (10MHz CHANNEL BANDWIDTH, 64 QAM FUSC)



TX CARRIER LEAKAGE vs. FREQUENCY



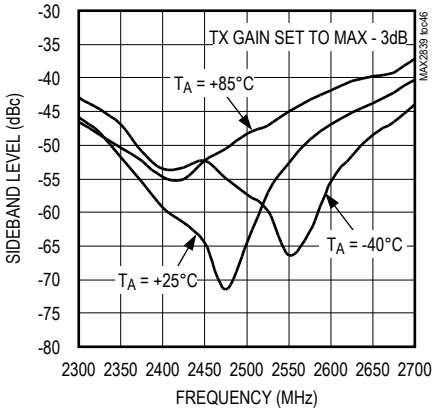
TX CARRIER LEAKAGE vs. GAIN SETTING



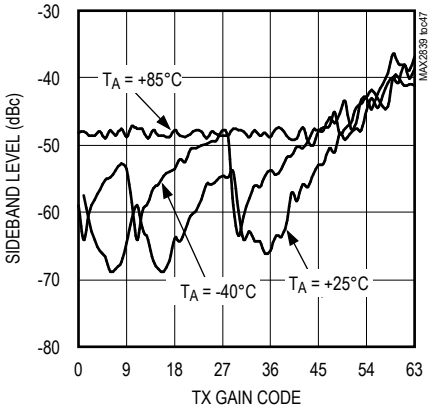
Typical Operating Characteristics (continued)

(V_{CC} = 2.8V, T_A = +25°C, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2839 Evaluation Kit.)

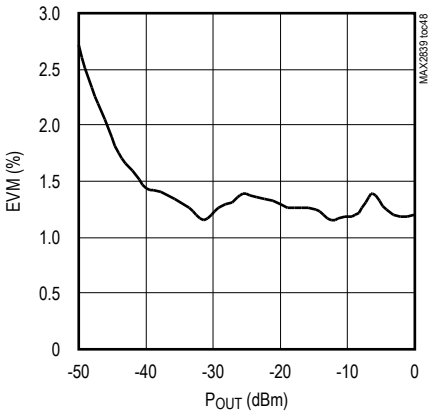
TX SIDEBAND LEVEL vs. FREQUENCY



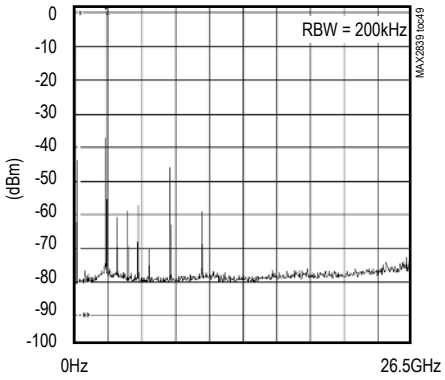
TX SIDEBAND LEVEL vs. GAIN SETTING



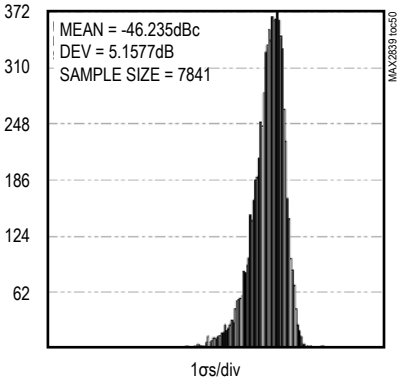
EVM vs. TX OUTPUT POWER (64 QAM FUSC, 10MHz CHANNEL BANDWIDTH)



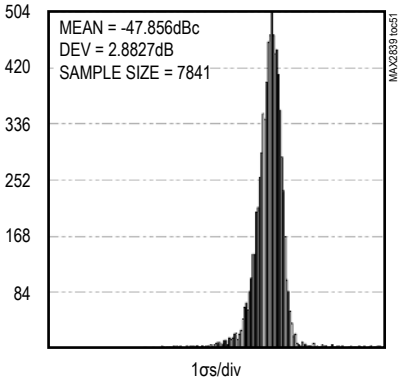
TX OUTPUT EMISSION SPECTRUM



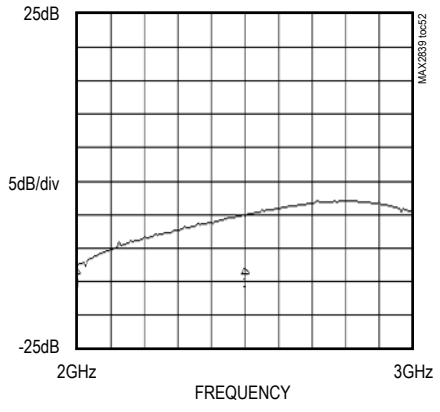
HISTOGRAM: TX LO LEAKAGE



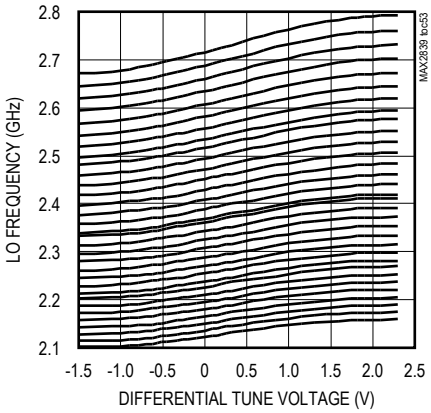
HISTOGRAM: TX SIDEBAND SUPPRESSION



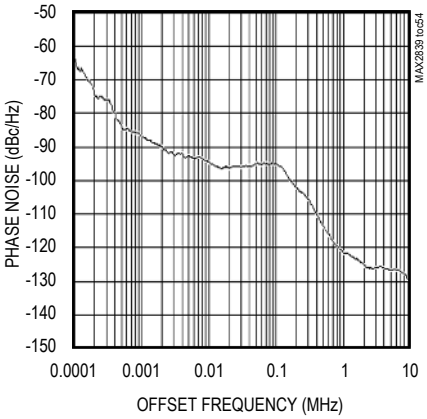
TX OUTPUT RETURN LOSS vs. FREQUENCY



LO FREQUENCY vs. DIFFERENTIAL TUNE VOLTAGE



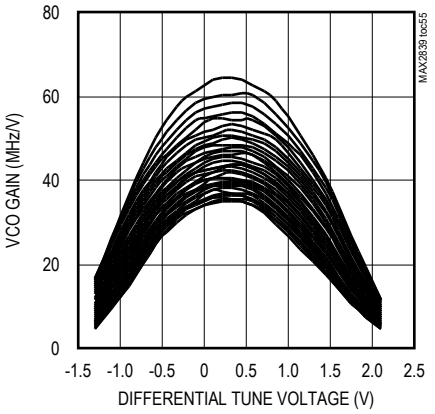
PHASE NOISE vs. OFFSET FREQUENCY



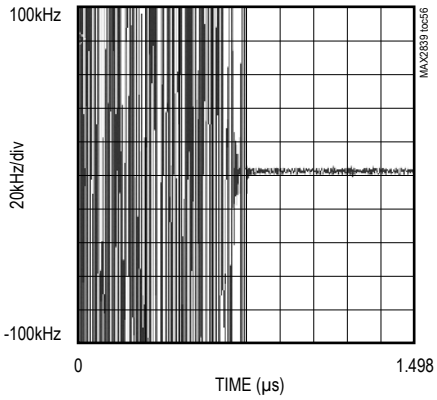
Typical Operating Characteristics (continued)

(V_{CC} = 2.8V, T_A = +25°C, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2839 Evaluation Kit.)

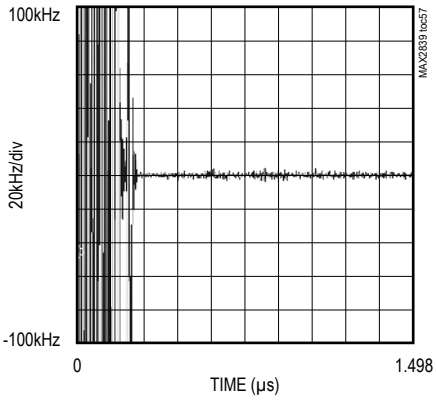
VCO GAIN vs. DIFFERENTIAL TUNE VOLTAGE



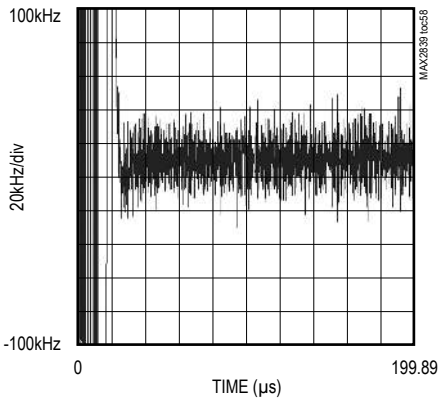
CHANNEL-SWITCHING FREQUENCY SETTLING (2.3GHz TO 2.7GHz, AUTOMATIC VCO SUB-BAND SELECTION)



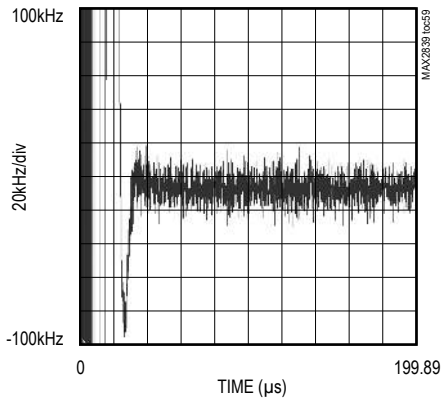
CHANNEL-SWITCHING FREQUENCY SETTLING (2.7GHz TO 2.3GHz, AUTOMATIC VCO SUB-BAND SELECTION)



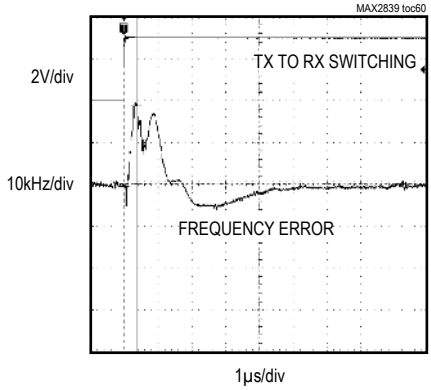
CHANNEL-SWITCHING FREQUENCY SETTLING (2.3GHz TO 2.7GHz, MANUAL VCO SUB-BAND SELECTION)



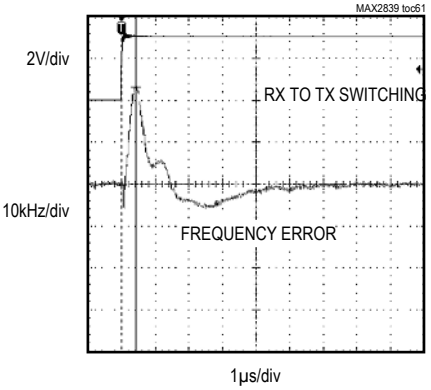
CHANNEL-SWITCHING FREQUENCY SETTLING (2.7GHz TO 2.3GHz, MANUAL VCO SUB-BAND SELECTION)



TX-TO-RX TURNAROUND FREQUENCY GLITCH SETTLING



RX-TO-TX TURNAROUND FREQUENCY GLITCHING SETTLING



Pin Description

PIN	NAME	FUNCTION
1	GNDRXLNA_A	Receiver A LNA Ground
2	VCCRXLNA_A	Receiver A LNA Supply Voltage. Bypass with a 22pF capacitor as close as possible to the pin.
3	B0	Receiver Gain-Control Logic Input Bit 0
4	LOAD	Receiver Gain Select. Positive edge trigger latches digital gain inputs B0–B7 to receive A. Negative edge trigger latches digital gain inputs B0–B7 to receive B.
5	VCCRXLNA_B	Receiver B LNA Supply Voltage. Bypass with a 22pF capacitor as close as possible to the pin.
6	GNDRXLNA_B	Receiver B LNA Ground
7	RXINB+	Receiver B LNA Differential Input. Input is internally DC-coupled.
8	RXINB-	
9	B4	Receiver and Transmitter Gain-Control Logic Input Bit 4
10	B3	Receiver and Transmitter Gain-Control Logic Input Bit 3
11	VCCTXPAD	Supply Voltage for Transmitter PA Driver. Bypass with a 22pF capacitor as close as possible to the pin.
12	B2	Receiver and Transmitter Gain-Control Logic Input Bit 2
13	TXOUT+	Power Amplifier Driver Differential Output. The pins have internal AC blocking capacitors.
14	TXOUT-	
15	B1	Receiver and Transmitter Gain-Control Logic Input Bit 1
16	B5	Receiver and Transmitter Gain-Control Logic Input Bit 5
17	PABIAS	Transmit External PA Bias DAC Output
18	VCCTXMX	Transmitter Upconverter Supply Voltage. Bypass with a 22pF capacitor as close as possible to the pin.
19	SCLK	Serial-Clock Logic Input of 4-Wire Serial Interface
20	ENABLE	Transceiver Enable
21	CLKOUT	Reference Clock Buffer Output
22	REFCLK	Crystal or Reference Clock Input. AC-couple a crystal or a reference clock to this analog input.
23	XTAL1	XTAL Input. Connect the other terminal of the XTAL to this pin.
24	VCCXTAL	Crystal Oscillator Supply Voltage. Bypass with a 100nF capacitor as close as possible to the pin.
25	VCCCP	PLL Charge-Pump Supply Voltage. Bypass with a 100nF capacitor as close as possible to the pin.
26	GNDCP	Charge-Pump Circuit Ground
27	CPOUT+	Differential Charge-Pump Output. Connect the frequency synthesizer's loop filter between these pins (see the *Typical Operating Circuit*).
28	CPOUT-	
29	GNDVCO	VCO Ground
30	VCOBYP	On-Chip VCO Regulator Output Bypass. Bypass with a 1µF capacitor to GND. Do not connect other circuitry to this pin.
31	VCCVCO	VCO Supply Voltage. Bypass with a 22nF capacitor as close as possible to the pin.
32	$\overline{CS}$	Chip-Select Logic Input of 4-Wire Serial Interface
33	DOUT	Data Logic Output of 4-Wire Serial Interface
34	DIN	Data Logic Input of 4-Wire Serial Interface
35	RXBBIB-	Receiver B Baseband I-Channel Differential Outputs
36	RXBBIB+	

Pin Description (continued)

PIN	NAME	FUNCTION
37	RXBBQB-	Receiver B Baseband Q-Channel Differential Outputs
38	RXBBQB+	
39	RSSI	Receiver Signal Strength Output
40	B7	Receiver Gain-Control Logic Input Bit 7
41	B6	Receiver and Transmitter Gain-Control Logic Input Bit 6
42	RXHP	Receiver Baseband AC-Coupling Highpass Corner Frequency Control Logic Input. For typical WiMAX application, connect pin to ground.
43	RXBBQA-	Receiver Baseband Q-Channel Differential Outputs
44	RXBBQA+	
45	RXBBIA-	Receiver A Baseband I-Channel Differential Outputs
46	RXBBIA+	
47	VCCRXVGA	Receiver VGA Supply Voltage. Bypass with a 100nF capacitor as close as possible to the pin.
48	VCCRXFL	Receiver Baseband Filter Supply Voltage. Bypass with a 100nF capacitor as close as possible to the pin.
49	TXBBI-	Transmitter Baseband I-Channel Differential Inputs
50	TXBBI+	
51	TXBBQ+	Transmitter Baseband Q-Channel Differential Inputs
52	TXBBQ-	
53	VCCRXMX	Receiver Downconverters Supply Voltage. Bypass with a 22pF capacitor as close as possible to the pin.
54	RXTX	Receive/Transmit Mode Enable
55	RXINA-	Receiver A LNA Differential Input. Input is internally DC-coupled.
56	RXINA+	
—	EP	Exposed Paddle. Internally connected to GND. Connect to a large ground plane for optimum RF performance and enhanced thermal dissipation. Not intended as an electrical connection point.

Table 1. Operating Mode

	MODE CONTROL LOGIC INPUTS				CIRCUIT BLOCK STATES				
MODE	ENABLE PIN	RXTX PIN	SPI REG1 D<3>	SPI REG16 D<1:0>	Rx PATH	Tx PATH	PLL, VCO, LO GEN	CALIBRATION SECTIONS ON	CLOCK OUTPUT
Shutdown	0	0	X	XX	Off	Off	Off	None	Off
Clock-Out Only	1	X	X	X0	Off	Off	Off	None	On
Clock-Out Only	X	1	X	X0	Off	Off	Off	None	On
Standby	0	1	X	01	Off	Off	On or Off	None	On
Rx (1x2 MIMO)	1	1	1	01	On	Off	On	None	On
Rx (1x1 SISO)	1	1	0	01	On (RxA)	Off	On	None	On
Tx	1	0	X	01	Off	On	On	None	On
Tx Calibration	1	0	X	11	Off	On (except PA driver)	On	AM detector + Rx I, Q buffers	On
RxA Calibration (Loopback)	1	1	0	11	On (except LNA)	On (except PA driver)	On	Loopback	On
RxB Calibration (Loopback)	1	1	1	11	On (except LNA)	On (except PA driver)	On	Loopback	On

Detailed Description

Modes of Operation

The modes of operation for the MAX2839 are shutdown, clock-out only, standby, receive, transmit, transmitter calibration and receiver calibration. See Table 1 for a summary of the modes of operation. When the parts are active, various blocks can be shutdown individually by programming different SPI registers.

Shutdown Mode

The MAX2839 features a low-power shutdown mode. In shutdown mode, all circuit blocks are powered down, except the 4-wire serial bus and its internal programmable registers.

Clock-Out Only

In clock-out mode, the entire transceiver is off except the divided reference clock output on the CLKOUT pin and the clock divider, which remains on.

Standby Mode

The standby mode is used to enable the frequency synthesizer block while the rest of the device is powered down. In this mode, PLL, VCO, and LO generator are on so that Tx or Rx modes can be quickly enabled from this mode. These and other blocks can be selectively enabled in this mode by programming different SPI registers.

Receive (Rx) Mode

In receive mode, all Rx circuit blocks are powered on and active. Antenna signal is applied; RF is downconverted, filtered, and buffered at Rx BB I and Q outputs. Either receiver A or both receivers can be enabled. Receiver B cannot be enabled by itself.

Transmit (Tx) Mode

In transmit mode, all Tx circuit blocks are powered on. The external PA is powered on after a programmable delay using the on-chip PA bias DAC.

Transmitter (Tx) Calibration Mode

All Tx circuit blocks except PA driver and external PA are powered on and active. The AM detector and receiver I/Q channel buffers are also ON, along with multiplexers in receiver side to route this AM detector's signal to each I and Q differential outputs.

Receiver (Rx) Calibration or Loopback

Part of Rx and Tx circuit blocks except LNA and PA driver are powered on and active. The transmitter I/Q input signals are upconverted to RF, and the output of the Tx gain control block (VGA) is fed to the receiver at the input of the downconverter. Either receiver A or both receivers can be connected to the transmitter and powered on. The I/Q lowpass filters are not present in the transmitter signal path (they are bypassed).

Temperature Sensor ReadOut Through DOUT Pin

To estimate chip temperature, on-chip temperature sensor is enabled by programming Address 9 D<1> = 1. The procedure is as follows:

1) Enable temp sensor by setting Address 9 D<1> = 1. Roughly 100µs to 1ms time is needed to let the temperature sensor output settle to within 5 to 1 degrees.
2) To trigger temperature sensor ADC, program Address 9 D<0> from “0” to “1”. The ADC will acquire the 5-bit logic output in 2µs, temperature sensor needs to be ON (Address 9 D<1> = 1) to maintain the ADC logic output. Note that the ADC trigger should happen AFTER the temp sensor is enabled to get correct result. Therefore, step 1 and step 2 of this procedure should be carried out on two separate SPI programming events separated by the temp sensor settling time.
3) Note that after the ADC latches its output and you desire to retake another temp sensor temperature reading value, the ADC has to be re-triggered to reacquire a new temp sensor value (assuming temp sensor is already enabled). To do so, program Address 9 D<0> from “1” to “0” then from “0” to “1”. After the ADC latches it digital output in 2µs it shuts off.
4) To read the 5-bit logic output through DOUT pin, apply 4-wire SPI readout programming sequence to Address 11.

VAS Operating Procedure

After power-up, program Address 22 D<1>=”0” such that VAS frequency acquisition starts from VCO band#15, it reduces the worst-case acquisition time by half. VAS acquisition starts after Address 17 is programmed (i.e. rising edge of CSB), it takes the worst-case 896µs to acquire lock.

Wireless LAN or MAN system do not switch channel frequency often, die temperature may change quite a bit over time and make PLL out of lock. To relock PLL as soon as possible, user can program Address 22 D<1> = “1” after the 1st power-up frequency acquisition. VAS starts from the previous frequency subband and should relock PLL within 112µs.

VAS Readout

The selected VCO subband, Vtune ADC output and VAS accomplished (VASA) signal can be read out through DOUT pin by programming Address 9 D<7:5>=”010” and corresponding Address 26 D<9:6>.

VCO Subband Selection Through SPI

For very fast band selection operation, user can characterize the mapping between VCO frequencies and corresponding subbands during factory calibration. After programming Address 22 D<0>=”0”, the VCO subband can be selected by Address 23 D<4:0>.

Programmable Registers and 4-Wire SPI Interface

The MAX2839 includes 32 programmable 16-bit registers. The most significant bit (MSB) is the read/write selection bit. The next 5 bits are register address. The 10 least significant bits (LSBs) are register data. Register data is loaded through the 4-wire SPI/MICROWIRE®-compatible serial interface. Data at DIN is shifted in MSB first and is framed by $\overline{CS}$. When $\overline{CS}$ is low, the clock is active, and input data is shifted at the rising edge of the clock. During the read mode, register data selected by address bits is shifted out to DOUT at the falling edges of the clock. At the $\overline{CS}$ rising edge, the 10-bit data bits are latched into the register selected by address bits. See Figure 1. The register values are preserved in shutdown mode as long as the power-supply voltage is maintained. However, every time the power-supply voltage is turned on, the registers are reset to the default values.

MICROWIRE is a registered trademark of National Semiconductor Corp.

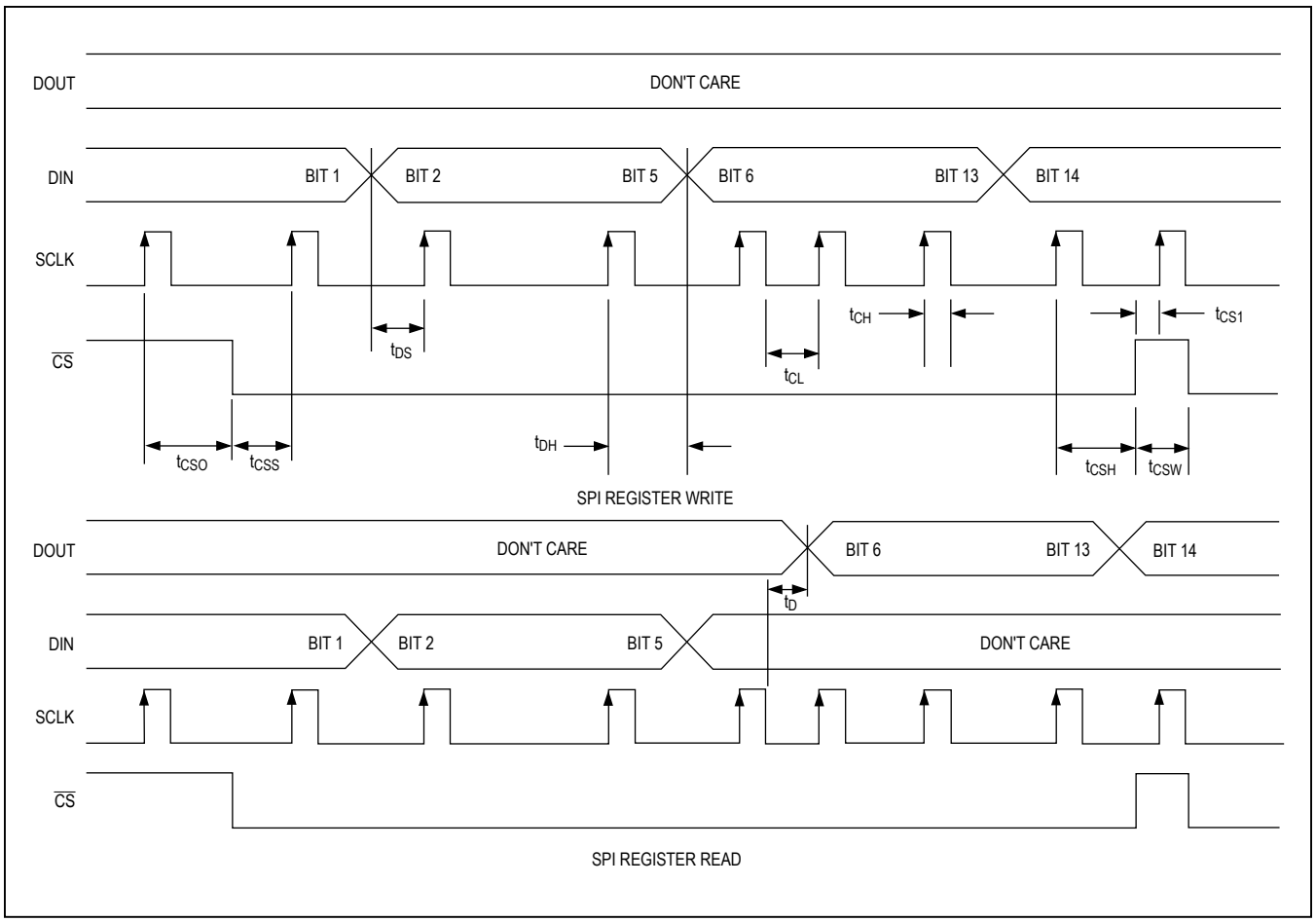


Figure 1. 4-Wire SPI Serial-Interface Timing Diagram

Table 2. Recommended Register Settings

ADDRESS	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	0	0	0	0	0	0	0	0	0	000
1	0	0	0	0	0	0	1	1	0	0	00C
2	0	0	1	0	0	0	0	0	0	0	080
3	0	1	1	0	1	1	1	0	0	1	1B9
4	1	1	1	1	1	0	0	1	1	0	3E6
5	0	1	0	0	0	0	0	0	0	0	100
6	0	0	0	0	0	0	0	0	0	0	000
7	1	0	0	0	0	0	1	0	0	0	208
8	1	0	0	0	1	0	0	0	0	0	220
9	0	0	0	0	0	1	1	0	0	0	018
10	0	0	0	0	0	0	1	1	0	0	00C
11	0	0	0	0	0	0	0	1	0	0	004
12	1	0	0	1	0	0	1	1	1	1	24F
13	0	1	0	1	0	1	0	0	0	0	150
14	1	1	1	1	0	0	0	1	0	1	3C5
15	1	0	0	0	0	0	0	0	0	1	201
16	0	0	0	0	0	1	1	1	0	0	01C
17	0	1	0	1	0	1	0	1	0	1	155
18	0	1	0	1	0	1	0	1	0	1	155
19	0	1	0	1	0	1	0	0	1	1	153
20	1	0	0	1	0	0	1	0	0	1	249
21	0	0	0	0	1	0	1	1	0	1	02D
22	0	1	1	0	1	0	1	0	0	1	1A9
23	1	0	0	1	0	0	1	1	1	1	24F
24	0	1	1	0	0	0	0	0	0	0	180
25	0	0	0	0	0	0	0	0	0	0	000
26	1	1	1	1	0	0	0	0	0	0	3C0
27	1	0	0	0	0	0	0	0	0	0	200
28	0	0	1	1	0	0	0	0	0	0	0C0
29	0	0	0	0	1	1	1	1	1	1	03F
30	1	1	1	0	0	0	0	0	0	0	380
31	1	1	0	1	0	0	0	0	0	0	340

Table 3. Address 0, RXENABLE Register (Default = 000_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D0	0000000000	Set to recommended value.

Table 4. Address 1, RXRF Register 1 (Default = $00C_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9:D4	00000	RX LO IQ calibration SPI control. Active when Address 2 D<2> = 1. As trim word of fuse links independent of Address 3 D<2>. 00000 = +4.0° phase error (default) (Q lags I signal by 94°) … 011111= 0.0° phase error … 11111 = -4.0° deg phase error (Q lags I signal by 86°)
D3	1	1*2 MIMO mode selection. 0 = 1*1 1= 1*2 MIMO (default)
D2	1	Set to recommended value.
D1:D0	0	**Selects center frequency of LNA output LC tank.** **0 = Band 2.3~2.5GHz (default)** **1 = Band 2.5~2.7GHz.**

Table 5. Address 2, RXRF Register 2 (Default = 080_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D3	0010000	Set to recommended value.
D2	0	RX IQ calibration DAC MUX between trim word and SPI. 0 = Mux trim word (default) 1 = Mux SPI
D1	0	Set to recommended value.
D0	0	Mux LNA gain control bits from SPI. 0 = LNA gain controlled by external pins (default) 1 = LNA gain controlled by SPI

Table 6. Address 3, RXRF and LPF (Default = $1B9_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9:D0	0110111001	Set to recommended value.

Table 7. Address 4, LPF (Default = $3E6_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9:D6	1111	LPF RF Bandwidth. 0000 = 1.75MHz 0001 = 2.5MHz 0010 = 3.5MHz 0011 = 5.0MHz 0100 = 5.5MHz 0101 = 6.0MHz 0110 = 7.0MHz 0111 = 8.0MHz 1000 = 9.0MHz 1001 = 10.0MHz 1010 = 12.0MHz 1011 = 14.0MHz 1100 = 15.0MHz 1101 = 20.0MHz 1110 = 24.0MHz 1111 = 28.0MHz (default)
D5:D4	10	Set to recommended value.
D3:D2	01	Fine tune the LPF cutoff frequency. 00: -10% 01: Nominal (default) 10: Nominal 11: +10%
D1:D0	10	Set to recommended value.

Table 8. Address 5, LPF and VGA Register 1 (Default = 100_{HEX})

	DEFAULT	DESCRIPTION
D9:D8	01	Mode of the lowpass filter block. Active when Address 8 D<2> = 1. 00 = Rx Calibration 01 = Rx LPF (default) 10 = Tx LPF 11 = LPF Trim
D7:D2	000000	Set attenuation in Rx1 VGA. Active when Address 8 D<1> = 1. 000000 = Maximum gain (default) 000001 = Max gain - 1dB … 111111 = Minimum gain
D1:D0	00	LNA1 gain setting SPI controls. Active when Address 2 D0 = 1. 00 = MAX gain (default) 01 = MAX -8dB 10 = MAX -16dB 11 = MAX -32dB

Table 9. Address 6, LPF and VGA Register 2 (Default = 000_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D8	00	Set RX VGA output common mode. 00 = 1.0V (default) 01 = 1.1V 10 = 1.2V 11 = 1.35V
D7:D2	000000	Set attenuation in Rx2 VGA. Active when Address 8 D<1> = 1. 000000 = MAX gain (default) 000001 = MAX gain - 1dB … 11111 = MIN gain
D1:D0	00	LNA2 gain setting SPI controls. Active when Address 2 D<0> = 1. 00 = MAX gain (default) 01 = MAX -8dB 10 = MAX -16dB 11 = MAX -32dB

Table 10. Address 7, RSSI and VGA Register (Default = 208_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9	1	Select RSSI input. 0 = Select input from RX2 1 = Select input from RX1 (default)
D8	0	Set to recommended value.
D7	0	RXBBI_P/M and RXBBQ_P/M pin output select. 0 = Select RXVGA output (default) 1 = Select TX AM detector output
D6:D3	0001	Set to recommended value.
D2	0	RSSI operating mode during RX mode. 0 = Off when RXHP = 0 (default) 1 = Independent of RXHP
D1	0	RSSI pin output MUX. 0 = RSSI (default) 1 = Temperature sensor
D0	0	Set to recommended value.

Table 11. Address 8, RX_TOP SPI Bits (Default = 220_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D3	1000100	Set to recommended value.
D2	0	LPF mode mux, LPF_MODE_SEL = 1. 0 = Normal operation (default) 1 = Operating mode is programmed Address 5 D<9:8>
D1	0	Mux VGA gain control bits from SPI. 0 = VGA gain controlled by external pins (default) 1 = VGA gain controlled by SPI
D0	0	Set to recommended value.

Table 12. Address 9, RX_TOP SPI Bits (Default = 018_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D8	00	Set to recommended value.
D7:D5	000	DOUT pin output MUX select. 000 = SPI output (default) 001 = PLL lock detect and test output by Address 21 D<9:7>. Set Address 21 D<9:7> = 000 for lock detect output. 010 = VAS test output by Address 26 D<9:6> 011 = HPFSM test output by Address 15 D<5:1> 100 = LOGEN trim divider output 101 = RX fuse burnt 110 = TX fuse burnt 111 = SET 0
D4	0	DOUT pin three-state control. 0 = DOUT pin is independent on CSB pin 1 = DOUT pin is Tri-state when CSB is Hi (default)
D3	0	DOUT pint output drive select. 0 = 1x (dly<4.4ns) 1 = 4x (dly<3.1ns, default)
D2	0	Set to recommended value.
D1	0	Temp sensor comparator and clock enable. 0 = Disable (default) 1 = Enable
D0	0	Temp sensor ADC trigger. 0 = Not trigger ADC readout (default) 1 = Trigger ADC readout, ADC is disabled automatically after readout finishes. See Detailed Description, section “Temperature Sensor ReadOut Through DOUT Pin.”

Table 13. Address 10, TX_TOP SPI Register 1 (Default = $00C_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9:D5	00000	Set to recommended value.
D4:D2	011	Adjust the bandwidth of TX AM detector baseband filter. 000 = Default +12% … 011 = Default bandwidth … 111 = Default – 16%
D1:D0	00	TX AM detector baseband gain control. 00 = Default minimum gain 01 = +10dB 10 = +20dB 11 = +30dB

Table 14. Address 11, Temperature Sensor 5-Bit ADC Outputs (Default = 004_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D0	0000000100	Set to recommended value.

Table 15. Address 12, HPFSM Register 1 Bits (Default = $24F_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9:D7	100	RXVGA 600kHz highpass corner duration triggered by B7 and B6 switching. 000 = 0µs 001 = 0.8µs 010 = 1.6µs 011 = 2.4µs 100 = 3.2µs (default) 101 = 4.0µs 110 = 4.8µs 111 = stay “1”
D6:D4	100	RXVGA 600kHz highpass corner duration triggered by RXEN rising edge. 000 = 0µs 001 = 0.8µs 010 = 1.6µs 011 = 2.4µs 100 = 3.2µs (default) 101 = 4.0µs 110 = 4.8µs 111 = stay “1”
D3:D2	11	RXVGA 10MHz highpass corner duration triggered by B7 and B6 switching. 00 = 0µs 01 = 0.4µs 10 = 0.8µs 11 = 1.2µs (default)
D1:D0	11	RXVGA 10MHz highpass corner duration triggered by RXEN rising edge. 00 = 0µs 01 = 0.4µs 10 = 0.8µs 11 = 1.2µs (default)

Table 16. Address 13, HPFSM Register 2 Bits (Default = 150_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D8	01	RXVGA 1kHz highpass corner duration triggered by RXEN rising edge. 00 = 0µs 01 = 3.2µs (default) 10 = 6.4µs 11 = 9.6µs
D7:D6	01	RXVGA 30kHz highpass corner duration triggered by B7 and B6 switching. 00 = 0µs 01 = 3.2µs (default) 10 = 6.4µs 11 = 9.6µs
D5:D4	01	RXVGA 30kHz highpass corner duration triggered by RXEN rising edge. 00 = 0µs 01 = 3.2µs (default) 10 = 6.4µs 11 = 9.6µs
D3:D2	00	RXVGA 100kHz highpass corner duration triggered by B7 and B6 switching. 00 = 0µs (default) 01 = 3.2µs 10 = 6.4µs 11 = 9.6µs
D1:D0	00	RXVGA 100kHz highpass corner duration triggered by RXEN rising edge. 00 = 0µs (default) 01 = 3.2µs 10 = 6.4µs 11 = 9.6µs

Table 17. Address 14, HPFSM Register 3 Bits (Default = $3C5_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9	1	PA DRV/DAC On/Off Gating by VAS TXOOL and PLL LD. 0 = Independent of TXOOL and LD 1 = Relock when TXOOL = 1 or LD = 0 (default)
D8	1	RXVGA HPFSM re-triggered by B7 and B6. 0 = Disable 1 = Enable (default)
D7:D6	11	RXVGA highpass corner on-hold selection only during MODE2 when RXHP = 1. 00 = 1kHz 01 = 30kHz 10 = 100kHz 11 = 600kHz (default)
D5:D4	00	RXVGA final highpass corner selection. 00 = 100Hz (default) 01 = 1kHz 10 = 30kHz 11 = 100kHz
D3:D2	01	**RXVGA HPCa and HPCd rising edge delay for 100k/30k/1k/100Hz highpass corner.** 00 = 0µs 01 = 0.2µs (default) 10 = 0.4µs 11 = 0.6µs
D1:D0	01	RXVGA 1kHz highpass corner duration triggered by B7 and B6 switching. 00 = 0µs 01 = 3.2µs (default) 10 = 6.4µs 11 = 9.6µs

Table 18. Address 15, HPFSM Register 4 Bits (Default = 201_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9	1	Highpass corner use of RXHP. 0 = Mode #1 does not require RXHP 1 = Mode #2 requires use of RXHP (default)
D8:D7	00	Set to recommended value.
D6	0	Sequence bypass during RXHP 1-->0 transition. 0 = Switch from HPC_STOP_M2<1:0> and programmed sequence (default) 1 = Switch from HPC_STOP_M2<1:0> directly to HPC_STOP<1:0>
D5:D1	00000	Set to recommended value.
D0	1	RXVGA HPFSM Clock Divider. 0 = For 20MHz crystal 1 = For 40MHz crystal (default)

Table 19. Address 16, Building Block SPI Enable Control (Default = $01C_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9:D8	00	Set to recommended value.
D7	0	PA Bias DAC TX Mode Enable. Enable PA Bias DAC only in TX mode. Turn on delay is controlled by Address 28<9:6>. 0 = Disable (default) 1 = Enable when pin TXENABLE = 1
D6	0	PA Bias DAC SPI Enable. Enable PA Bias DAC in all modes except shut down. Turn-on delay is controlled by Address 27<9:6>. 0 = Disable (default) 1 = Enable except during shut down mode
D5:D2	0111	Set to recommended value.
D1	0	RX/TX Calibration Mode Enable. RX or TX mode is selected by pin RXEN or TXEN. 0 = Normal operation (default) 1 = Calibration mode
D0	0	Chip-Enable Bit. Logic AND with pin ENABLE to enable/disable the whole chip except crystal oscillator and CLKOUT pin buffer. 0 = Disable (default) 1 = Enable

Table 20. Address 17, Synthesizer Fractional Divide Ratio #1 (Default = 155_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D0	0101010101	Synthesizer 20-bit Fractional Divide Ratio Bit<9:0>, combine with Address 18 D<9:0> to form the whole fractional word.

Table 21. Address 18, Synthesizer Fractional Divide Ratio #2 (Default = 155_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D0	0101010101	Synthesizer 20-bit Fractional Divide Ratio Bit<19:10>, combine with Address 17 D<9:0> to form the whole fractional word

Table 22. Address 19, Synthesizer Integer Divide Ratio (Default = 153_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D8	01	LO Generation Band Switch Control for Optimal TX Spur. 00 = 2300~2399.99MHz 01 = 2400~2499.99MHz (default) 10 = 2500~2599.99MHz 11 = 2600~2700MHz
D7:D0	01010011	Synthesizer 8-bit Integer Divide Ratio

Table 23. Address 20, Synthesizer Configuration#1 (Default = 249_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D6	1001	Set to recommended value.
D5	0	CLKOUT Buffer drive. 0 = 1x drive, default 1 = 4x drive
D4:D3	01	Set to recommended value.
D2:D1	00	Reference Divider Ratio. 00 = Divide-by-1 (default) 01 = Divide-by-2 10 = Divide-by-4 11 = Divide-by-8
D0	1	Set to recommended value.

Table 24. Address 21, Synthesizer Configuration#2 (Default = $02D_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9:D0	0000101101	Set to recommended value.

Table 25. Address 22, VCO Auto-Select (VAS) Configuration (Default = $1A9_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9:D8	01	Set to recommended value.
D7	1	VAS Triggering by Address 17 Enable. See Address 17 definitions for details. 0 = Disable for small frequency adjustment (i.e.~100kHz). 1 = Enable for channel switching (default)
D6:D5	01	VAS Delay Counter Ratio. Delay = Txtal * VAS_DIV<2:0> * VAS_DLY<1:0> * 7. 00 = 16 01 = 32 (default) 10 = 64 11 = 128
D4:D2	010	VAS Clock Divide Ratio. 000 = 8 001 = 9 010 = 10 (default) … 110 = 14 111 = 2
D1	0	VAS Relock Mode Select. 0 = Relock starting at subband 15 (default) 1 = Relock starting at present subband for short acquisition time.
D0	1	VAS Operating Mode Select. 0 = Select VCO subband by SPI Address 23 D<4:0> (VAS_SPI<4:0>) 1 = Select VCO subband by VAS (default)

Table 26. Address 23, LO Miscellaneous Configuration (Default = $24F_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9:D7	100	Set to recommended value.
D6:D5	10	Crystal Oscillator Bias Select. 00 = 240µA for 20MHz 01 = 420µA for 20MHz 10 = 600µA for 40MHz (default) 11 = 780µA for 40MHz
D4:D0	01111	VAS Subband SPI Overwrite. Active when Address 22 D<0> (VAS_MODE) = 0. 00000 = Minimum frequency … 01111 = 15 (default) … 11111 = Maximum frequency

Table 27. Address 24, Crystal Oscillator Configuration (Default = 180_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9	0	Crystal Oscillator Core Enable. Enable except for shut down mode. 0 = Disable (default) 1 = Enable
D8	1	CLKOUT Divide Ratio. 0 = Divide-by-1 1 = Divide-by-2 (default)
D7	1	Set to recommended value.
D6:D0	0000000	Crystal Oscillator Frequency Tuning. 0000000 = Maximum frequency (default) … 1111111 = Minimum frequency

Table 28. Address 25, Voltage-Controlled Oscillator (VCO) Configuration (Default = 000_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9:D0	0000000000	Set to recommended value.

Table 29. Address 26, LO Generation (LOGEN) Configuration (Default = $3C0_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9:D6	1111	VAS Test Signal Select. Delivered to DOUT output MUX and selected by Address 9 D<7:5> (DOUT_SEL<2:0>). 0000 = VCO_BSW<0> 0001 = VCO_BSW<1> 0010 = VCO_BSW<2> 0011 = VCO_BSW<3> 0100 = VCO_BSW<4> 0101 = Vtune_ADC<0> 0110 = Vtune_ADC<1> 0111 = Vtune_ADC<2> 1000 = VASA 1001 = VASE 1010 = VASA 1011 = VASE 11xx = “0” 1111 = “0” (default) VCO_BSW<4:0> = VCO 5-bit frequency band switch determined by VAS. Vtune_ADC<2:0> = VCO Vtune (i.e. Vcpoutp) ADC output.
D5:D4	00	Set to recommended value.
D3	0	LOGEN RX/TX Gm Enable 0 = Depends on RX/TX ENABLE pins (default) 1 = Enable both RX/TX output (required for Rx loop-back calibration)
D2:D0	000	Set to recommended value.

Table 30. Address 27, PA Driver Configuration (Default = 200_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9	1	Set to recommended value.
D8	0	TX DC Offset SPI Adjust Enable. 0 = By fuse (default) 1 = By SPI
D7	0	TX VGA Gain SPI Control Enable. 0 = By pin (default) 1 = By SPI Address 29 D<5:0>
D6	0	TX LO I/Q Phase SPI Adjust Enable. 0 = By trim (default) 1 = By Address 27 D<5:0>
D5:D0	000000	TX LO I/Q Phase SPI Adjust. Active when Address 27 D<6> (TXLO_IQ_SPI_EN) = 1. As trim word for fuse trim. 000000 = +4deg (Q lags I by 94degs, default) … 011111 = +0deg … 111111 = -4deg (Q lags I by 86degs)

Table 31. Address 28, PA Bias DAC (PADAC) Configuration (Default = $0C0_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9:D6	0011	PADAC Turn-On Delay Control. 0000 = 0µs 0001 = 0µs 0010 = 0.5µs … 0011 = 1.0µs (default) … 1111 = 7.0µs
D5:D0	000000	PADAC Output Current Control. Active when Address 27 D<5> = 1 (PADAC_IV). 000000 = 0µA (default) 000001 = 5µA … 111111 = 315µA

Table 32. Address 29, TX Gain Configuration (Default = $03F_{HEX}$)

DATA BITS	DEFAULT	DESCRIPTION
D9:D6	0000	Set to recommended value.
D5:D0	111111	TX VGA SPI Gain Control. Active when Address 27 D<7> (TXVGA_GAIN_SPI_EN) = 1. 000000 = Min attenuation … 111111 = Max attenuation (default)

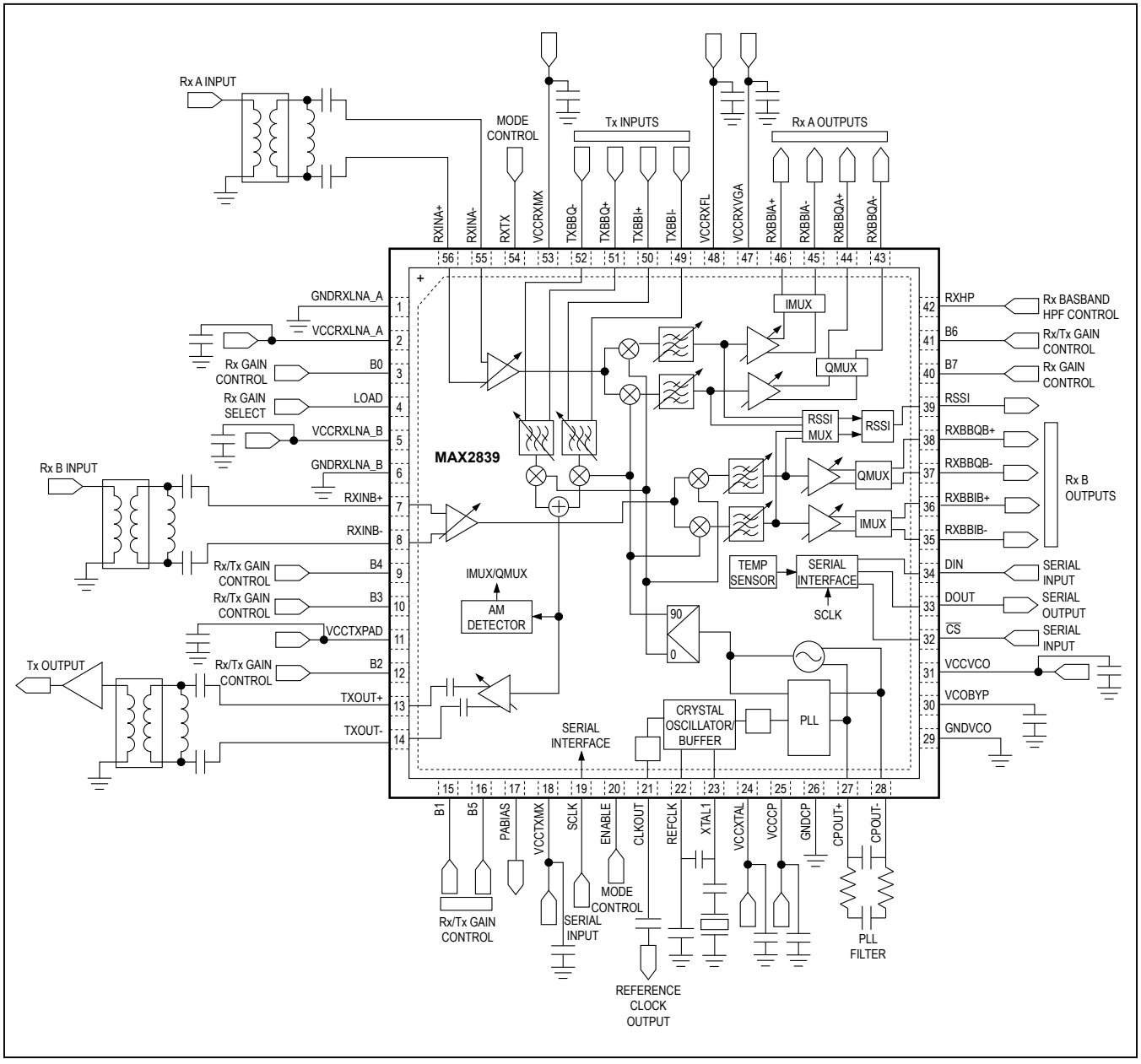
Table 33. Address 30, TX LO I/Q Correction (Default = 380_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9	1	PA DAC Voltage Mode Output Select. Active when Address 30 D<8> (PADAC_IV) = 0. 0 = Logic “0” output 1 = Logic “1” output (default)
D8	1	PA DAC I/V Output Select. 0 = Voltage output 1 = Current output (default)
D7:D6	00	Set to recommended value.
D5:D0	000000	TX DC Offset Correction for I-Channel. Active when Address 27 D<8> (TX_DCCORR_SPI_EN) = 1. As trim word for fuse trim. 000000 = 992/0µA (+/-ve offset current, default) 000001 = 960/32µA 000010 = 928/64µA … 011111 = 512/480µA … 111111 = 0/992µA

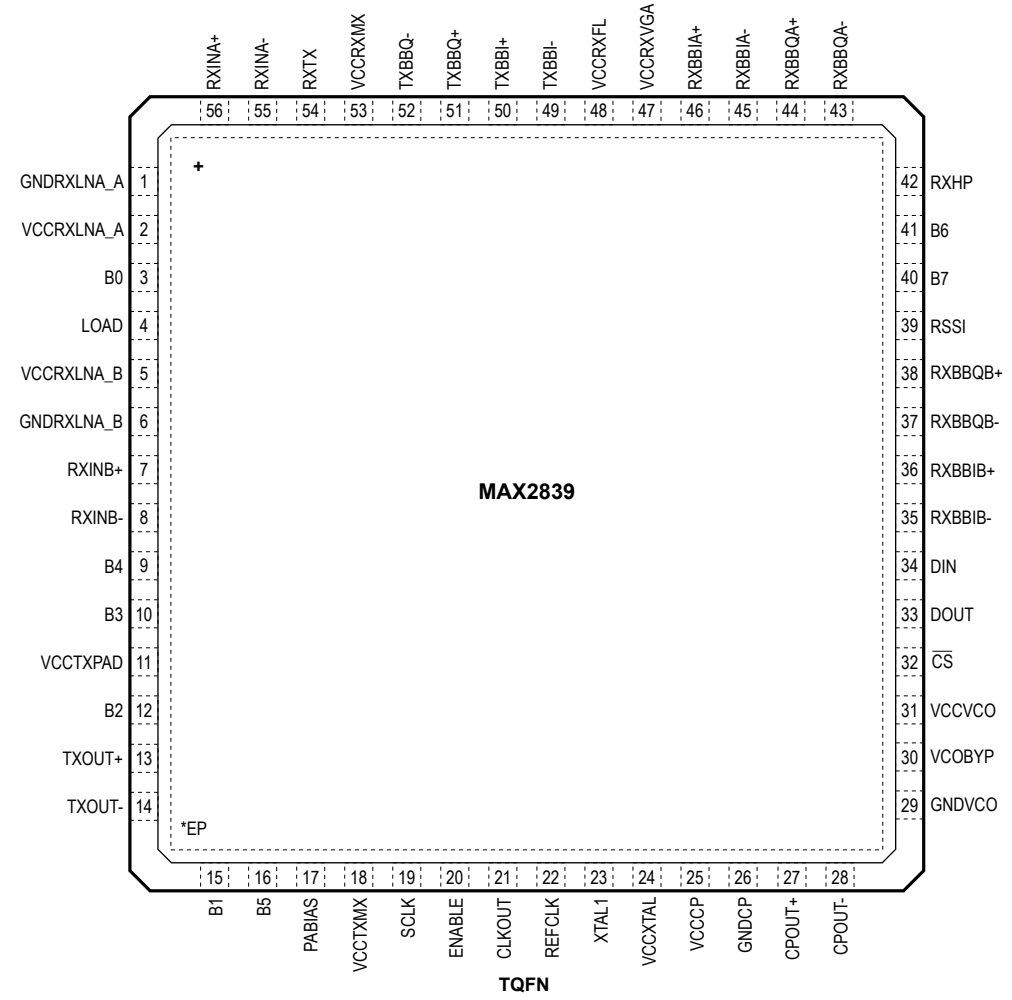
Table 34. Address 31, TX DC Correction Configuration (Default = 340_{HEX})

DATA BITS	DEFAULT	DESCRIPTION
D9	1	PA DAC Clock Divide Ratio. 0 = for 20MHz crystal clock 1 = for 40MHz crystal clock (default)
D8:D6	101	Set to recommended value.
D5:D0	000000	TX DC Offset Correction for Q-Channel. Active when Address 27 D<8> (TX_DCCORR_SPI_EN) = 1. As trim word for fuse trim. 000000 = 992/0µA (+/-ve offset current, default) 000001 = 960/32µA 000010 = 928/64µA … 011111 = 512/480µA … 111111 = 0/992µA

Block Diagram/Typical Operating Circuit



Pin Configuration



*EP = EXPOSED PAD.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.	LAND PATTERN NO.
56 TQFN-EP	T5688+2	21-0135	90-0046

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/08	Initial release	—
1	3/08	Corrected *Ordering Information* and pin 42 in *Pin Description*	1, 19
2	7/15	Added new *Temperature Sensor Readout Through DOUT Pin*, *VAS Operating Procedure*, *VAS Readout*, and *VCO Subband Selection Through SPI* sections. Added Register and Bit Descriptions.	20–36