EVALSTGAP2SICD

Data brief

Demonstration board for EVALSTGAP2SICD isolated 4 A half-bridge gate driver

Features

- **Board**
  - High voltage rail up to 1200 V
  - Negative gate driving
  - On-board isolated DC-DC converters to supply high-side and low-side gate drivers, fed by VAUX = 5 V, with 5.2 kV maximum isolation
  - VDD logic supplied by on-board generated 3.3 V or VAUX = 5V
  - Easy jumper selection of driving voltage configuration: +17/0 V; +17/-3 V; +19/0 V; +19/-3 V;
- **Device**
  - Driver current capability: 4 A source/sink @ 25°C
  - 4 A Miller CLAMP
  - Short propagation delay: 75 ns
  - UVLO function
  - Configurable interlocking function
  - Dedicated SD and BRAKE pins
  - Gate driving voltage up to 26 V
  - 3.3 V, 5 V TTL/CMOS inputs with hysteresis
  - Temperature shutdown protection
  - Standby function

Product status link
EVALSTGAP2SICD

Description

The EVALSTGAP2SICD is an half bridge evaluation board designed to evaluate the STGAP2SiCD isolated dual gate driver.

The gate driver is characterized by 4 A current capability and rail-to-rail outputs, making the device suitable also for high power applications such as motor drivers in industrial applications equipped with SiC power switches.

The device integrates protection functions: dedicated SD and BRAKE pins are available, UVLO and thermal shutdown are included to easily design high reliability systems, and the interlocking function prevents outputs from being high at the same time.

The device allows implementing negative gate driving, and the on-board isolated DC-DC converters allows working with optimized driving voltage for SiC MOSFETs.

The EVALSTGAP2SICD board allows evaluating all the STGAP2SICD features while driving a half-bridge power stage with voltage rating up to 1200 V in TO-220 or TO-247 package.

The board allows easily selecting and modifying the values of relevant external components in order to ease driver performance evaluation under different applicative conditions and fine pre-tuning of final application components.

1 Schematic diagram

Figure 1. **EVALSTGAP2SICD schematic – gate driver**

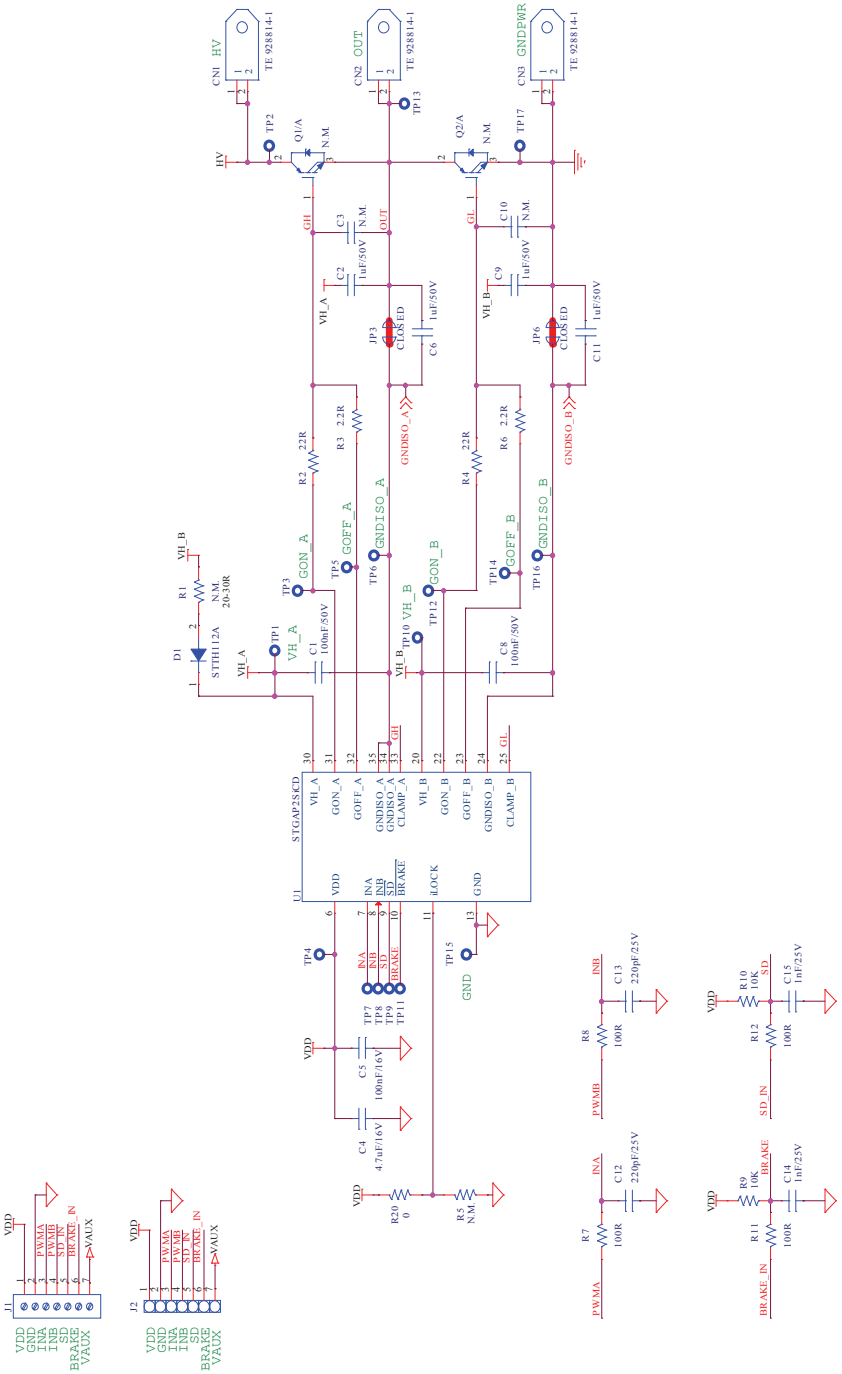
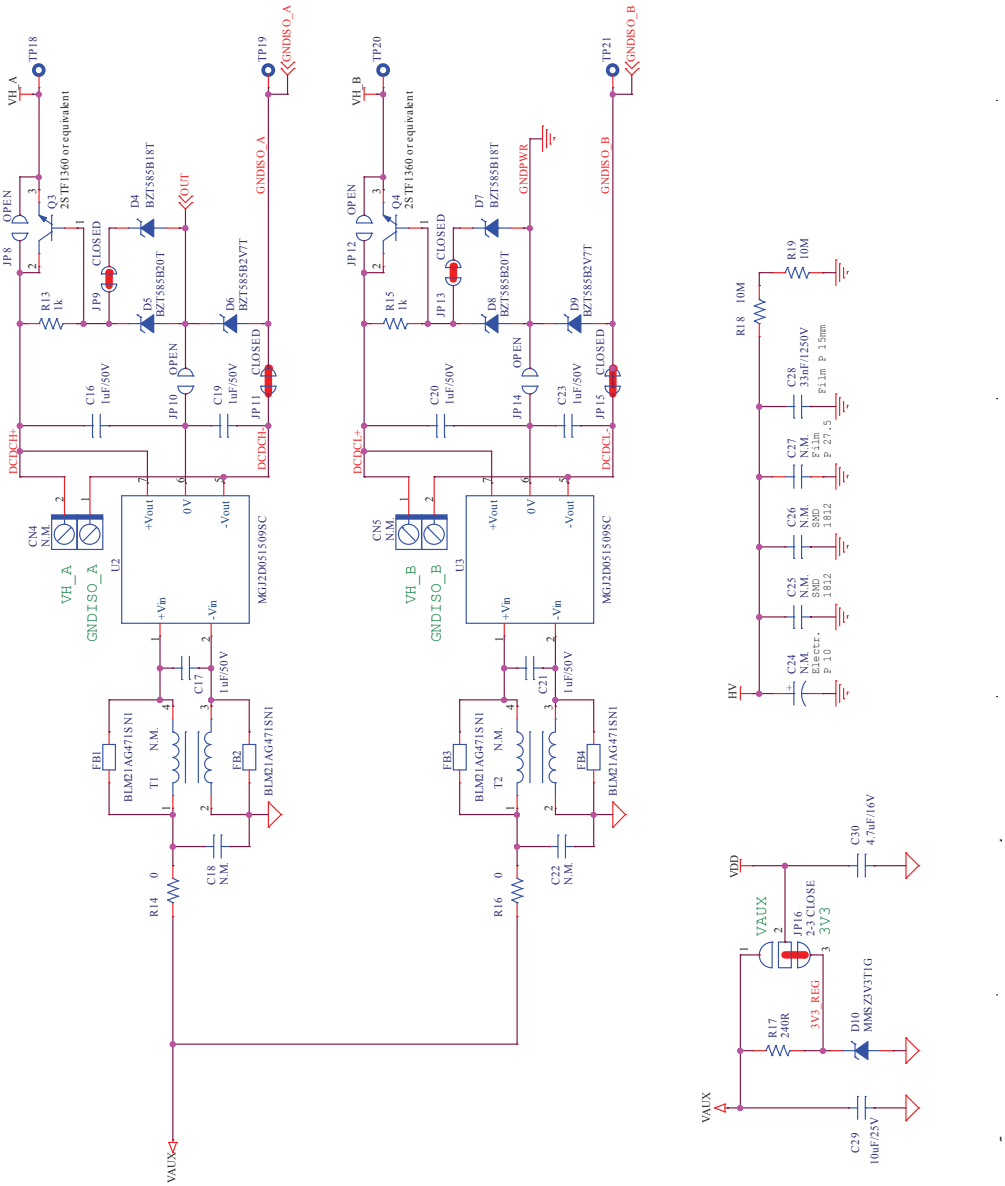


Figure 2. EVALSTGAP2SICD circuit schematic – supply, connectors and decoupling



2 Bill of material

Table 1. **EVALSTGAP2SICD - Bill of Material**

Part Reference	Part value	Part description
CN1, CN2, CN3	TE 928814-1	Tab FASTON 250 Horizontal, 5.08 mm
CN4, CN5	N.M.	Connector terminal block T.H. 2 POS 5.08 mm
C1, C8	100 nF / 50 V	Ceramic capacitor, SMT 1206
C2, C6, C9, C11	1 µF / 50 V	Ceramic capacitor, SMT 0805
C3, C10, C18, C22	N.M.	Ceramic capacitor, SMT 0603
C4, C30	4.7 µF / 16 V	Ceramic capacitor, SMT 0603
C5	100 nF / 16 V	Ceramic capacitor, SMT 0603
C12, C13	220 pF / 25 V	Ceramic capacitor, SMT 0603
C14, C15	1 nF / 25 V	Ceramic capacitor, SMT 0603
C16, C17, C19, C20, C21, C23	1 µF / 50 V	Ceramic capacitor, SMT 0603
C24	N.M.	THT electrolytic capacitor, P 10 mm
C25, C26	N.M.	Ceramic capacitor, SMT 1812
C27	N.M.	Film capacitor, P 27.5 mm
C28	33 nF / 1250 V	Film capacitor, P 15 mm
C29	10 µF / 25 V	Ceramic capacitor, SMT 0805
D1	STTH112A	High voltage ultrafast rectifier, SMA
D4, D7	BTZT585B18T	Surface mount precision Zener diode, SOD523
D5, D8	BZT585B20T	Surface mount precision Zener diode, SOD523
D6, D9	BZT585B2V7T	Surface mount precision Zener diode, SOD523
D10	MMSZ3V3T1G	Zener voltage regulator 500 mW, SOD-123
FB1, FB2, FB3, FB4	BLM21AG471SN1	Ferrite beads, SMT 0805
JP3, JP6, JP9, JP11, JP13, JP15	Closed	SMT jumper
JP8, JP10, JP12, JP14	Open	SMT jumper
JP16	Closed 2-3	SMT jumper
J1	WE691243110007 or similar	Connector terminal block T.H. 7 POS 3.5 mm
J2	Pin strip	Strip connector 7 pos, 2.54 mm
Q1, Q2	N.M.	N-channel IGBT or MOSFET up to 1700 V, TO-247
Q1A, Q2A	N.M.	N-channel IGBT or MOSFET up to 1700 V, TO-220
Q3, Q4	2STF1360	Low voltage fast-switching NPN power transistors, SOT-89
R1	N.M.	Chip resistor, SMT 1206
R2, R4	22 Ω	Chip resistor, SMT 1210
R3, R6	2.2 Ω	Chip resistor, SMT 1210
R5	N.M.	Chip resistor, SMT 0603
R7, R8, R11, R12	100 Ω	Chip resistor, SMT 0603
R9, R10	10 kΩ	Chip resistor, SMT 0603
R13, R15	1 kΩ	Chip resistor, SMT 0603
R14, R16, R20	0 Ω	Chip resistor, SMT 0603
R17	240 Ω	Chip resistor, SMT 0805
R18,R19	10 MΩ	Chip resistor, SMT 1206

Part Reference	Part value	Part description
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17	N.M.	Loop test point, THT
TP18, TP19, TP20, TP21	N.M.	Pad test point, SMD 1.5 mm
T1, T2	N.M.	Common mode choke, SMD 4.7x4.5 mm
U1	STGAP2SICD	Galvanically isolated 4 A dual gate driver for SiC MOSFETs, SO-36W
U2, U3	MGJ2D051509SC	Murata 5.2 kVDC Isolated 2W Gate Drive DC/DC converters

3 Layout and component placements

Figure 3. **EVALSTGAP2SICD – Layout (component placement top view)**

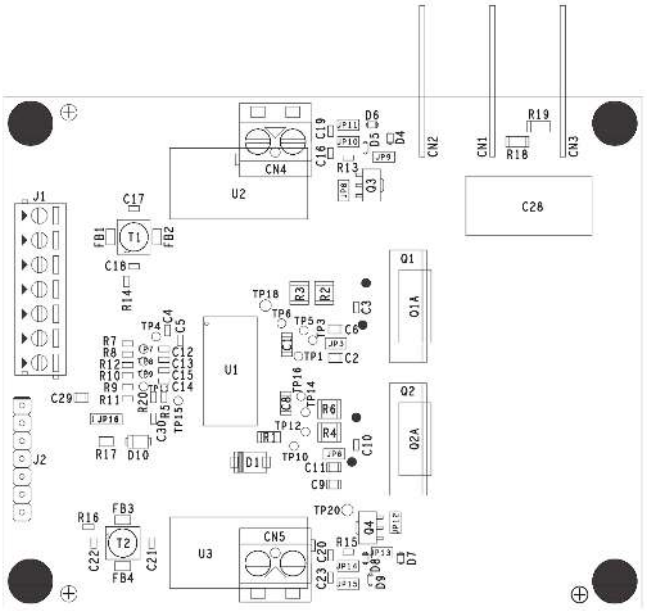


Figure 4. **EVALSTGAP2SICD – Layout (component placement bottom view)**

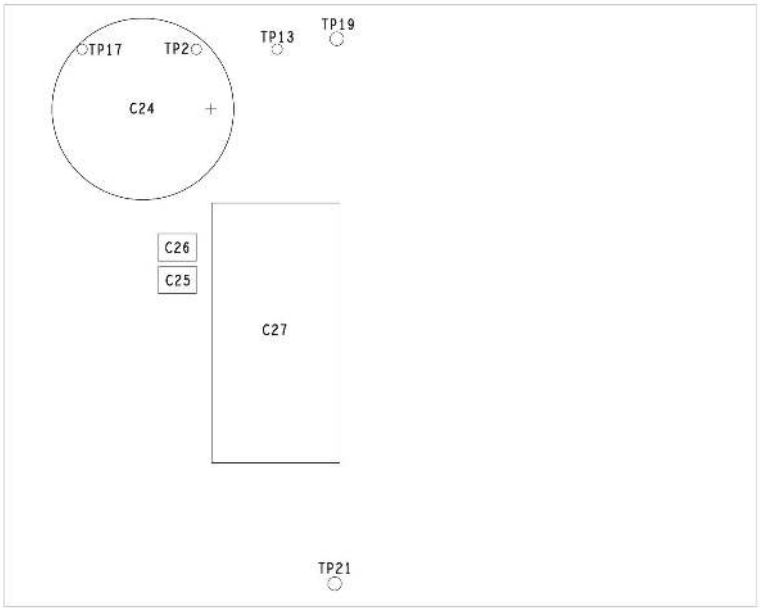


Figure 5. **EVALSTGAP2SICD – Layout (top layer)**

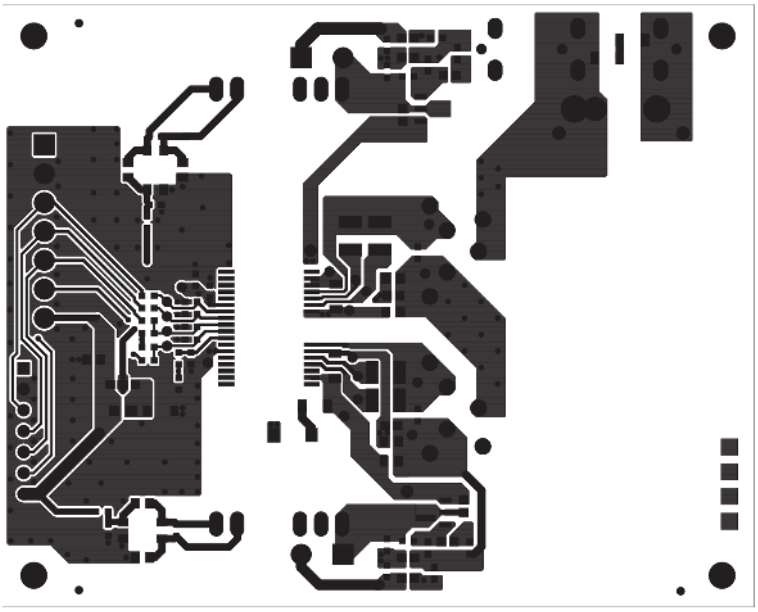
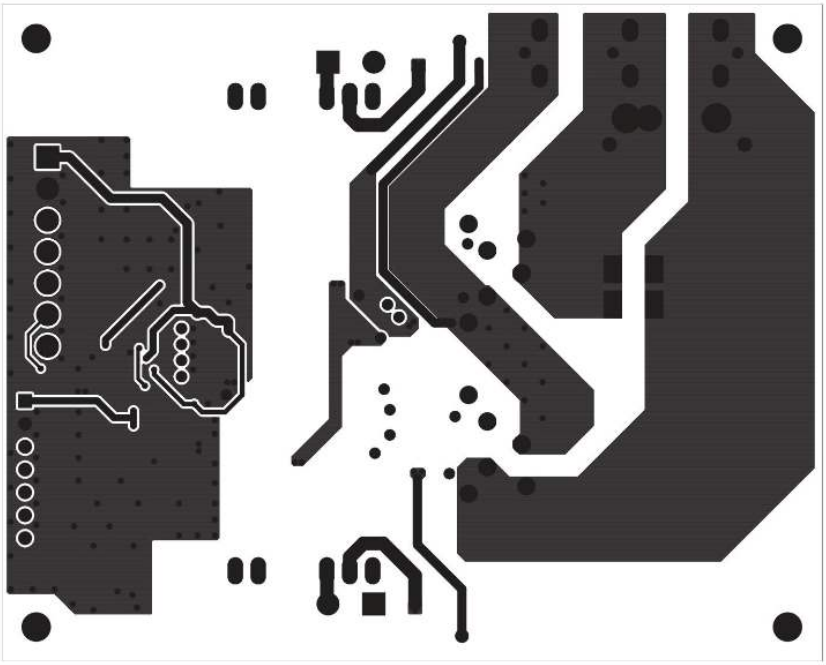


Figure 6. **EVALSTGAP2SICD – Layout (bottom layer)**



Revision history

Table 2. **Document revision history**

Date	Version	Changes
29-Oct-2021	1	Initial release.

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