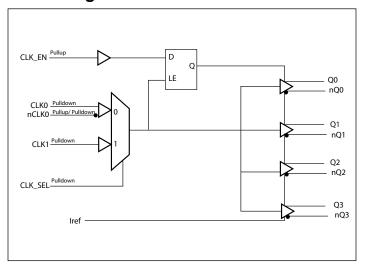




High Performance HCSL Fanout Buffer

Features

- → 4 HCSL outputs
- → Up to 250MHz output frequency
- → Ultra low additive phase jitter: < 0.1 ps (typ)
- → Two selectable inputs
- → Low delay from input to output (Tpd typ. 1.5ns)
- \rightarrow 2.5V / 3.3V power supply
- → Industrial temperature support
- → Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- → Halogen and Antimony Free. "Green" Device (Note 3)
- → TSSOP-20 package



Block Diagram

Description

The PI6C4931504-04 is a high performance fanout buffer device which supports up to 250MHz frequency. This device is ideal for systems that need to distribute low jitter clock signals to multiple destinations.

Applications

- → Networking systems including switches and Routers
- → High frequency backplane based computing and telecom platforms

Pin Configuration (20-Pin TSSOP)

GND [10	20 🛛 Q0
CLK_EN	2	19 🗍 nQ0
CLK_SEL	3	18 🛛 V _{DD}
CLK0	4	17 🛛 Q1
nCLK0	5	16 🗍 nQ1
CLK1	6	15 🛛 Q2
NC E	7	14 🛛 nQ2
NC E	8	13 🛛 V _{DD}
IREF [9	12 🛛 Q3
V _{DD} C	10	11 🗍 nQ3
l		

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- PI6C4931504-04 Document Number DS41269 Rev 1-2





Pin Description

Pin #	Pin Name	Туре	Description		
1	GND	Power	Ground		
2	CLK_EN	Input	Clock output enable/ disable		
3	CLK_SEL	Input	Clock input source selection pin		
4, 5	CLK0	Input	Clock input		
4, 5	nCLK0	Input	Clock input		
6	CLK1	Input	Clock input		
7, 8	NC	-	No connect		
9	IREF	Power	External resistor connection to set differential output current		
10, 13, 18	V _{DD}	Power	Power supply		
11 12	nQ3	Quitmut	UCSI output do de		
11, 12	Q3	Output	HCSL output clock		
14 15	nQ2	Qutput	HCSL output clock		
14, 15 Q2		Output	HCSL output clock		
16 17	nQl	Qutput	HCSL output clock		
16, 17	Q1	Output	HCSL output clock		
10.20	nQ0	Output	HCSL output clock		
19, 20	Q0	Output	HCSL output clock		

Function Table

Table 1: Input select function

CLK_SEL	Function	
0	CLK0, nCLK0	
1	CLK1	

Table 2: Output Enable function

CLK_EN	Outputs		
	Q0:Q4	nQ0:nQ4	
0	Disabled; LOW	Disabled; HIGH	
1	Enabled	Enabled	





Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply Characteristics and Operating Conditions

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Units
V _{DD} Core S	Cone Sumply Voltage		2.97		3.63	V
	Core Supply Voltage		2.375		2.625	V
I _{DD} Power S		V_{DD} = 3.3V, Unloaded			90	
	Power Supply Current	V_{DD} = 2.5V, Unloaded			80	mA
T _A	Ambient Operating Temperature		-40		85	°C

DC Electrical Specifications - Differential Inputs

Symbol	Parameter		Min.	Тур.	Max.	Units
I _{IH}	Input High current: CLK0, nCLK0	Input = V_{DD}			200	uA
т	Input Low current: nCLK0		-200			uA
I _{IL}	Input Low current: CLK0		-10			uA
C _{IN}	Input capacitance			4		PF
V _{IH}	Input high voltage				V _{DD} +0.3	V
V _{IL}	Input low voltage		-0.3			V
V _{ID}	Input Differential Amplitude PK-PK		150		1300	mV
V _{CM}	Common model input voltage		GND + 0.5		V _{DD} -0.85	V





Symbol	Parameter		Conditions	Min.	Тур.	Max.	Units
т	Input High current	CLK1, CLK_SEL	Lement V			200	uA
I _{IH}	Input Ingli current	CLK_EN	Input = V_{DD}			20	uA
I _{IL} Input Low current	CLK1, CLK_SEL	Lucrat CND	-10			uA	
	Input Low current	CLK_EN	Input = GND	-200			uA
V _{IH}	Input high voltage		$V_{DD}=3.3V$	2.0		3.765	V
VIL	Input low voltage		V _{DD} =3.3V	-0.3		0.8	V
VIH	Input high voltage		V _{DD} =2.5V	1.7		2.8	V
V _{IL}	Input low voltage		V _{DD} =2.5V	-0.3		0.7	V

DC Electrical Specifications - LVCMOS Inputs

DC Electrical Specifications – HCSL Outputs

Parameter	Description	Conditions	Min.	Тур.	Max.	Units
Voh	Output High voltage	V _{DD} =3.3V	520	800		mV
Vol	Output Low voltage	V _{DD} =3.3V		0	150	mV

AC Electrical Specifications – Differential Outputs

Parameter	Description	Conditions	Min.	Тур.	Max.	Units
f _{out}	Output frequency				250	MHz
Tr	Output rise time	From 20% to 80%	175		700	ps
T _f	Output fall time	From 80% to 20%	175		700	ps
T _{ODC}	Output duty cycle		48		52	%
Tj	Buffer additive jitter RMS			0.1		ps
V _{MAX}	Absolute Maximum Output Voltage				1150	mV
V _{MIN}	Absolute Minimum Output Voltage		-300			mV
V _{CROSS}	Absolute crossing voltage	HCSL	250		550	mV
DV _{CROSS}	Total variation of crossing voltage	HCSL			140	mV
T _{SK}	Output Skew			40	100	ps
T _{PD}	Propagation Delay			1500		ps
T _{P2P} Skew	Part to Part Skew ¹				600	ps

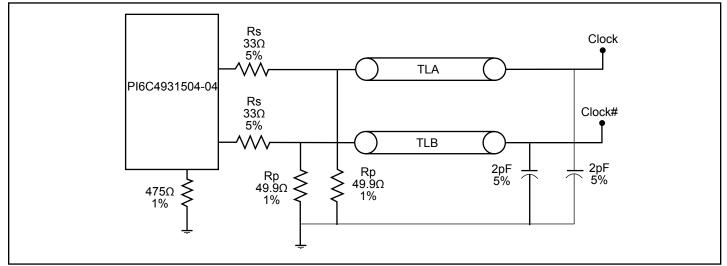
Notes:

1. This parameter is guaranteed by design





Configuration test load board termination for HCSL Outputs



Part Marking

L Package

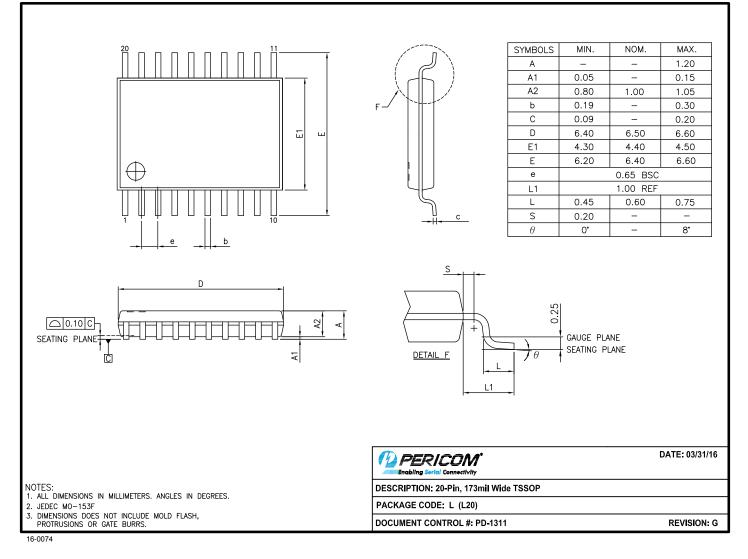


YY: Year WW: Workweek 1st X: Assembly Code 2nd X: Fab Code





Packaging Mechanical: 20-TSSOP (L)



For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information⁽¹⁻³⁾

Ordering Code	Package Code	Package Description
PI6C4931504-04LIEX	L	20-pin, 173mil Wide (TSSOP)

Notes:

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2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm

antimony compounds.

4. E = Pb-free and Green

5. X suffix = Tape/Reel





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