Data Sheet, Version 1.1, 2007-02-26

TDA5252 G2
ASK/FSK 915MHz Wireless Transceiver

Wireless Control Components

Never stop thinking.

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Data Sheet

Revision History:	**2007-02-26**	TDA5252 G2
Previous Version: 1.0 as of 2006-12-12		
Page	Subjects (major changes since last revision)	
72	indication of the ESD-integrity values	

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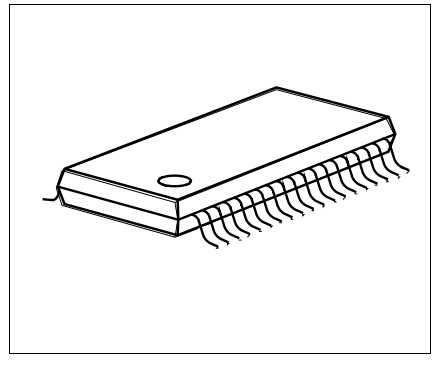
Product Info

General Description



The IC is a low power consumption single chip FSK/ASK Transceiver for half duplex low datarate communication in the 915MHz band. The IC offers a very high level of integration and needs only a few external components. It contains a highly efficient power amplifier, a low noise amplifier (LNA) with AGC, a double balanced mixer, a complex direct conversion stage, I/Q limiters with RSSI generation, an FSK demodulator, a fully integrated VCO and PLL synthesizer, a tuneable crystal oscillator, an onboard data filter, a data comparator (slicer), positive and negative peak detectors, a data rate detection circuit and a 2/3-wire bus interface. Additionally there is a power down feature to save battery power.

Features

- Low supply current (I_s = 9mA typ. receive, I_s = 13mA typ. transmit mode)
- Supply voltage range 2.1 - 5.5V
- Power down mode with very low supply current consumption
- FSK and ASK modulation and demodulation capability
- Fully integrated VCO and PLL synthesizer and loop filter on-chip with on chip crystal oscillator tuning
- I^2C/3-wire µController Interface
- On-chip low pass channel select filter and data filter with tuneable bandwidth
- Data slicer with self-adjusting threshold and 2 peak detectors
- FSK sensitivity < -109dBm, ASK sensitivity < -109dBm
- Transmit power up to +13dBm
- Self-polling logic with ultra fast data rate detection

Application

- Low Bitrate Communication Systems
- Keyless Entry Systems
- Remote Control Systems
- Alarm Systems
- Telemetry Systems
- Electronic Metering
- Home Automation Systems

Type	Ordering Code	Package
TDA5252 G2	SP000057332	PG-TSSOP-38

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1 Product Description

1.1 Overview

The IC is a low power consumption single chip FSK/ASK Transceiver for the ISM frequency band 915MHz. The IC combines a very high level of integration and minimum external part count. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesizer, a crystal oscillator with FSK modulator, a limiter with RSSI generator, an FSK demodulator, a data filter, a data comparator (slicer), a positive and a negative data peak detector, a highly efficient power amplifier and a complex digital timing and control unit with I^2C/3-wire microcontroller interface. Additionally there is a power down feature to save battery power.

The transmit section uses direct ASK modulation by switching the power amplifier, and crystal oscillator detuning for FSK modulation. The necessary detuning load capacitors are external. The capacitors for fine tuning are integrated. The receive section is using a novel single-conversion/ direct-conversion scheme that is combining the advantages of both receive topologies. The IF is contained on the chip, no RF channel filters are necessary as the channel filter is also on the chip.

The self-polling logic can be used to let the device operate autonomously as a master for a decoding microcontroller.

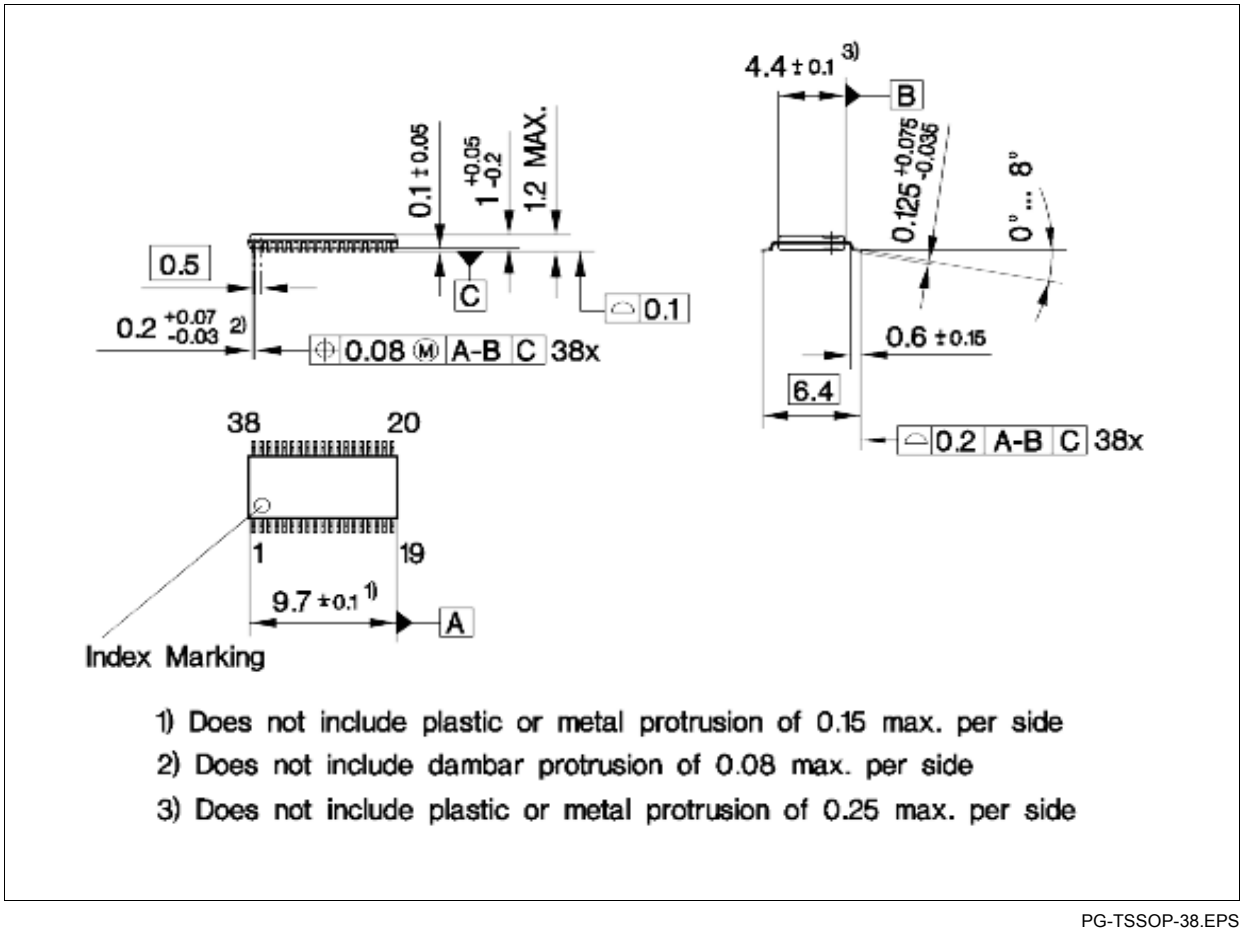
1.2 Features

- Low supply current (I_s = 9 mA typ. receive, I_s = 13mA typ. transmit mode, both at 3 V supply voltage, 25°C)
- Supply voltage range 2.1 V to 5.5 V
- Operating temperature range -40°C to +85°C
- Power down mode with very low supply current consumption
- FSK and ASK modulation and demodulation capability without external circuitry changes, FM demodulation capability
- Fully integrated VCO and PLL synthesizer and loop filter on-chip with on-chip crystal oscillator tuning, therefore no additional external components necessary
- Differential receive signal path completely on-chip, therefore no external filters are necessary
- On-chip low pass channel select and data filter with tuneable bandwith
- Data slicer with self-adjusting threshold and 2 peak detectors
- Self-polling logic with adjustable duty cycle and ultrafast data rate detection and timer mode providing periodical interrupt
- FSK and ASK sensitivity < -109 dBm
- Adjustable LNA gain
- Digital RSSI and Battery Voltage Readout
- Provides Clock Out Pin for external microcontroller
- Transmit power up to +13 dBm in 50Ω load at 5V supply voltage
- I^2C/3-wire microcontroller interface, working at max. 400kbit/s

1.3 Application

- Low Bitrate Communication Systems
- Keyless Entry Systems
- Remote Control Systems
- Alarm Systems
- Telemetry Systems
- Electronic Metering
- Home Automation Systems

1.4 Package Outlines

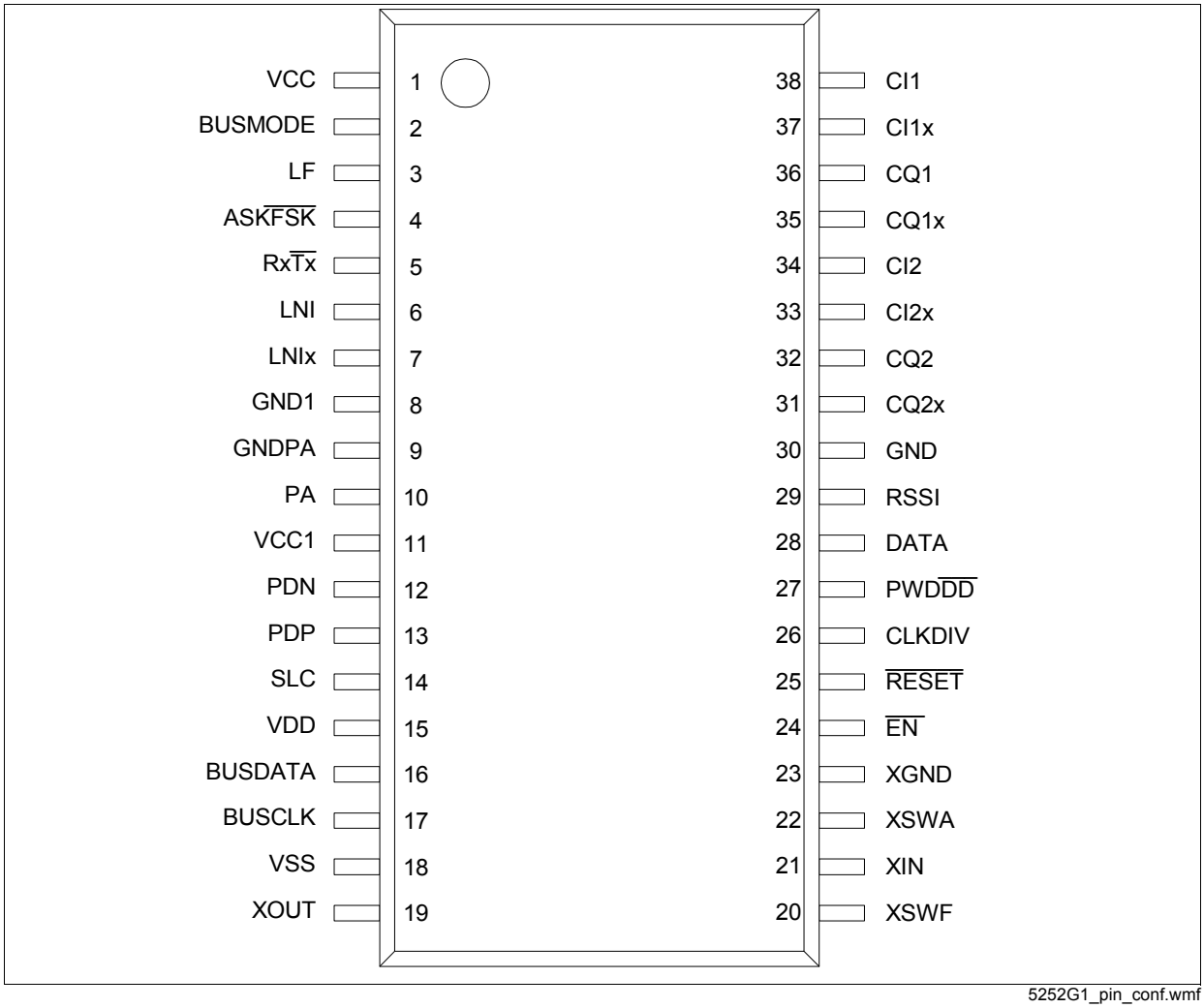


PG-TSSOP-38.EPS

Figure 1-1 PG-TSSOP-38 package outlines

2 Functional Description

2.1 Pin Configuration

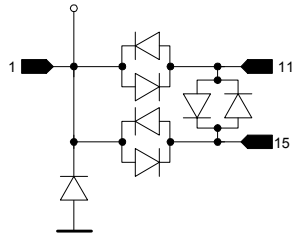
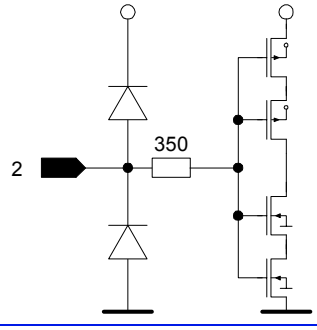
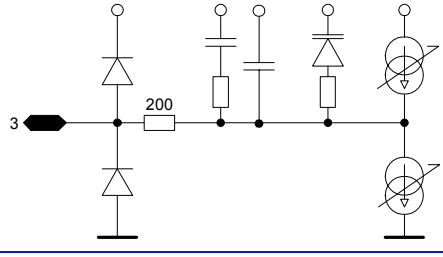
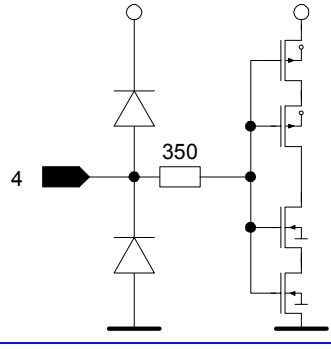


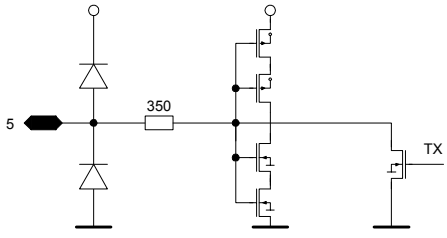
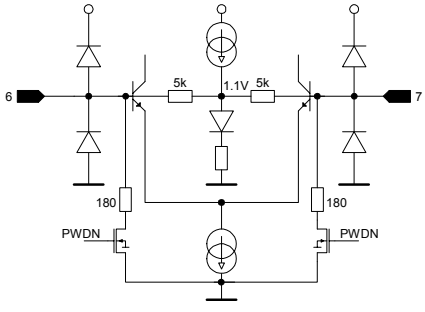
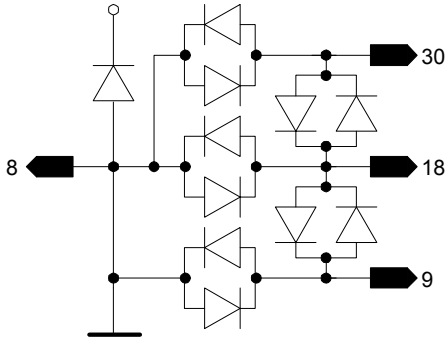
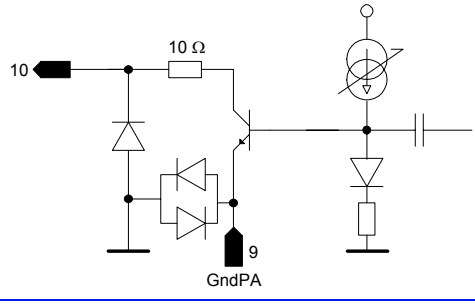
5252G1_pin_conf.wmf

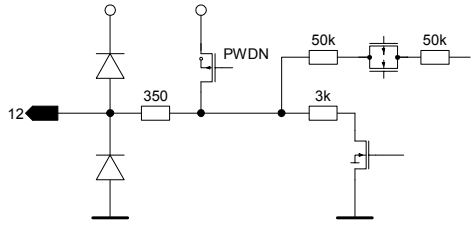
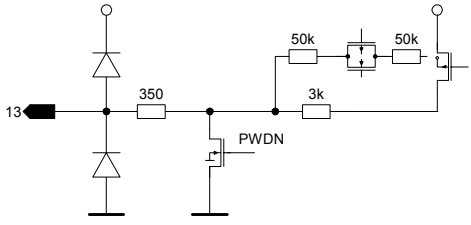
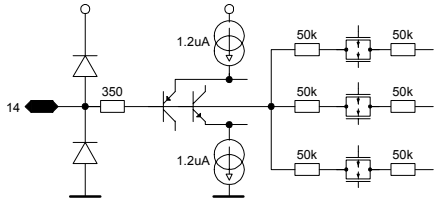
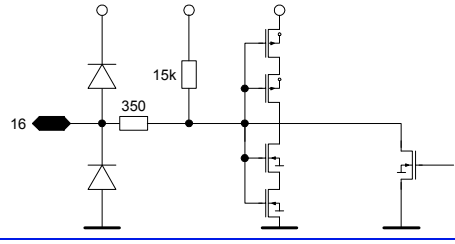
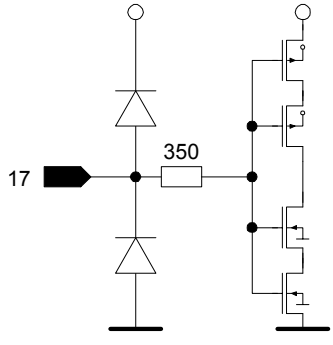
Figure 2-1 Pin Configuration

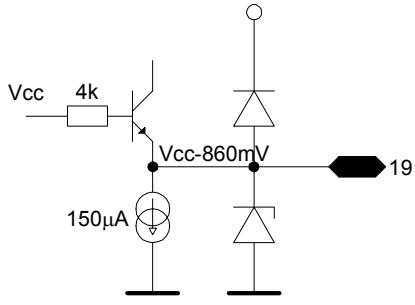
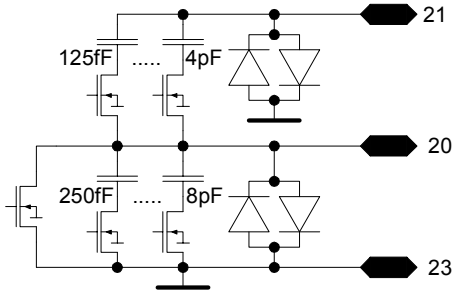
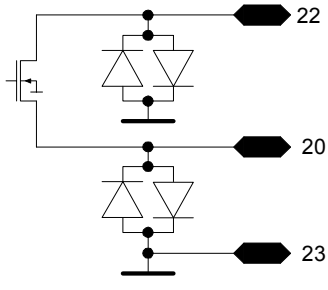
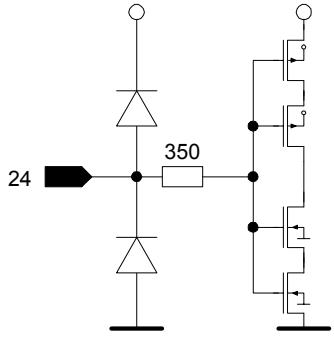
2.2 Pin Definitions and Functions

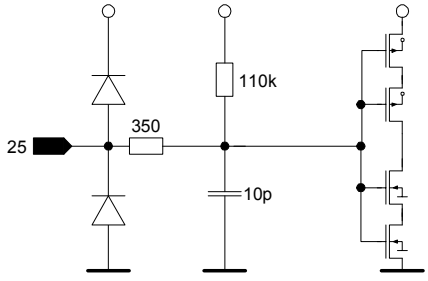
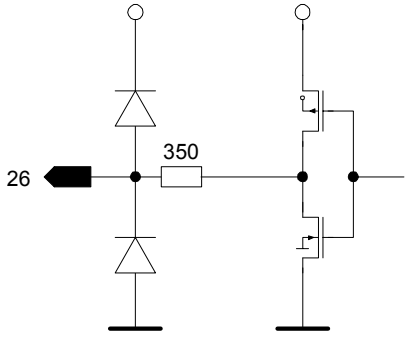
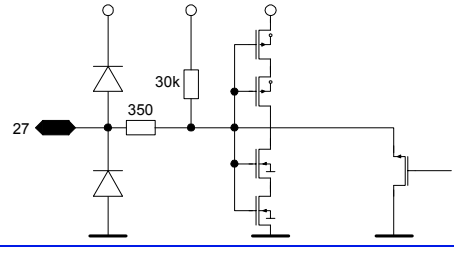
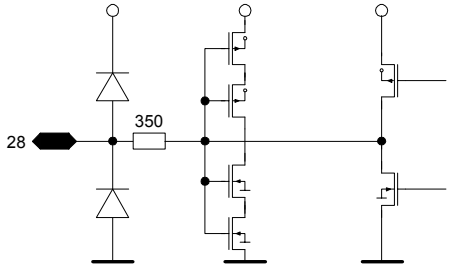
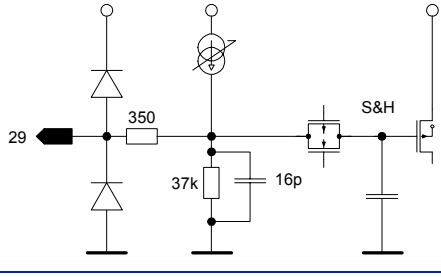
Table 2-1 Pin Definition and Function

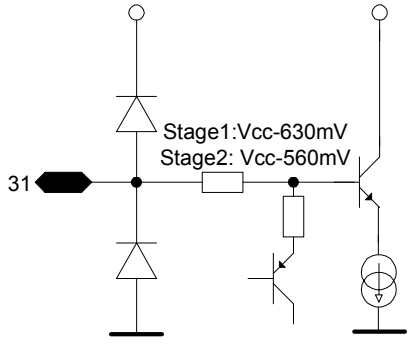
Pin No.	Symbol	Equivalent I/O-Schematic	Function
1	VCC		Analog supply (antiparallel diodes between VCC, VCC1, VDD)
2	BUSMODE		Bus mode selection (I²C/3 wire bus mode selection)
3	LF		Loop filter and VCO control voltage
4	ASK$\overline{\text{FSK}}$		ASK/FSK- mode switch input

5	RXTX		RX/TX-mode switch input/output
6	LNI		RF input to differential Low Noise Amplifier (LNA))
7	LNIX	see Pin 6	Complementary RF input to differential LNA
8	GND1		Ground return for LNA and Power Amplifier (PA) dirver stage
9	GNDPA	see Pin 8	Ground return for PA output stage
10	PA		PA output stage
11	VCC1	see Pin 1	Supply for LNA and PA

12	PDN		Output of the negative peak detector
13	PDP		Output of the positive peakdetector
14	SLC		Slicer level for the data slicer
15	VDD	see Pin 1	Digital supply
16	BUSDATA		Bus data in/output
17	BUSCLK		Bus clock input
18	VSS	see Pin 8	Ground for digital section

19	XOUT		Crystal oscillator output, can also be used as external reference frequency input.
20	XSWF		FSK modulation switch
21	XIN	see Pin 20	
22	XSWA		ASK modulation/FSK center frequency switch
23	XGND	see Pin 22	Crystal oscillator ground return
24	$\overline{EN}$		3-wire bus enable input

25	$\overline{\text{RESET}}$		Reset of the entire system (to default values), active low
26	CLKDIV		Clock output
27	PWD$\overline{\text{DD}}$		Power Down input (active high), data detect output (active low)
28	DATA		TX Data input, RX data output (RX powerdown: pin 28 @ GND)
29	RSSI		RSSI output

30	GND	see Pin 8	Analog ground
31	CQ2x		Pin for external Capacitor Q-channel, stage 2
32	CQ2	II	Q-channel, stage 2
33	CI2x	II	I-channel, stage 2
34	CI2	II	I-channel, stage 2
35	CQ1x	II	Q-channel, stage 1
36	CQ1	II	Q-channel, stage 1
37	CI1x	II	I-channel, stage 1
38	CI1	II	I-channel, stage 1

2.3 Functional Block Diagram

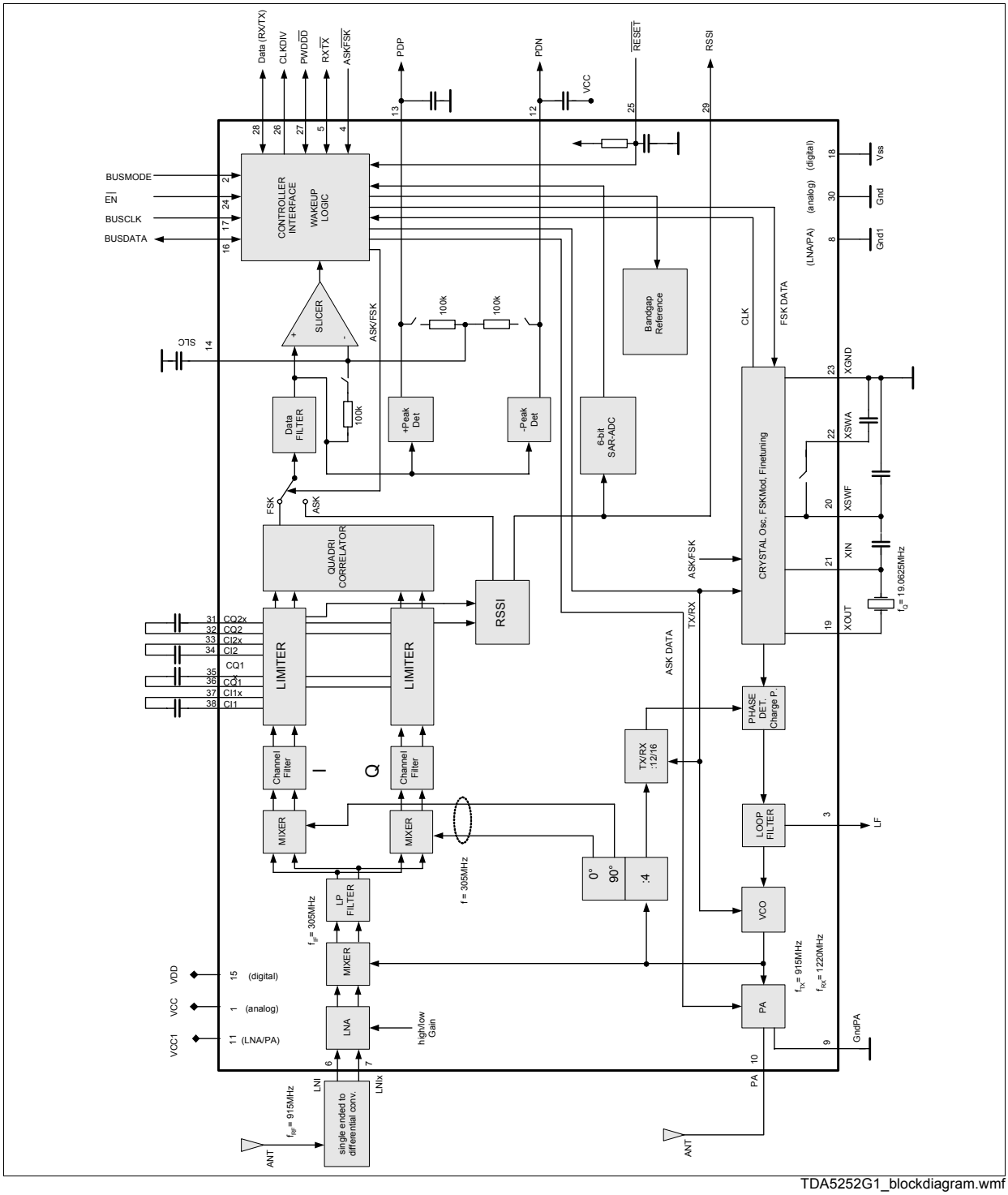


Figure 2-2 Main Block Diagram

2.4 Functional Block Description

2.4.1 Power Amplifier (PA)

The power amplifier is operating in C-mode. It can be used in either high or low power mode. In high-power mode the transmit power is approximately +13dBm into 50 Ohm at 5V and +6dBm at 2.1V supply voltage. In low power mode the transmit power is approximately -3dBm at 5V and -30dBm at 2.1V supply voltage using the same matching network. The transmit power is controlled by the **D0**-bit of the **CONFIG** register (subaddress 00H) as shown in the following **Table 2-2**. The default output power mode is high power mode.

Table 2-2 Sub Address 00H: CONFIG

Bit	Function	Description	Default
D0	PA_PWR	0= low TX Power, 1= high TX Power	1

In case of ASK modulation the power amplifier is turned fully on and off by the transmit baseband data, i.e. 100% On-Off-Keying.

2.4.2 Low Noise Amplifier (LNA)

The LNA is an on-chip cascode amplifier with a voltage gain of 15 to 20dB and symmetrical inputs. It is possible to reduce the gain to 0 dB via logic.

Table 2-3 Sub Address 00H: CONFIG

Bit	Function	Description	Default
D4	LNA_GAIN	0= low Gain, 1= high Gain	1

2.4.3 Downconverter 1st Mixer

The Double Balanced 1st Mixer converts the input frequency (RF) in the range of 915MHz down to the intermediate frequency (IF) at approximately 305MHz. The local oscillator frequency is generated by the PLL synthesizer that is fully implemented on-chip as described in **Section 2.4.5**. This local oscillator operates at approximately 1220MHz in receive mode providing the above mentioned IF frequency of 305MHz. The mixer is followed by a low pass filter with a corner frequency of approximately 350MHz in order to prevent RF and LO signals from appearing in the 305MHz IF signal.

2.4.4 Downconverter 2nd I/Q Mixers

The Low pass filter is followed by 2 mixers (inphase I and quadrature Q) that convert the 305MHz IF signal down to zero-IF. These two mixers are driven by a signal that is generated by dividing the local oscillator signal by 4, thus equalling the IF frequency.

2.4.5 PLL Synthesizer

The Phase Locked Loop synthesizer consists of two VCOs (i.e. transmit and receive VCO), a divider by 4, an asynchronous divider chain with selectable overall division ratio, a phase detector with charge pump and a loop filter and is fully implemented on-chip. The VCOs are including spiral inductors and varactor diodes. The center frequency of the transmit VCO is 915MHz, the center frequency of the receive VCO is 1220MHz.

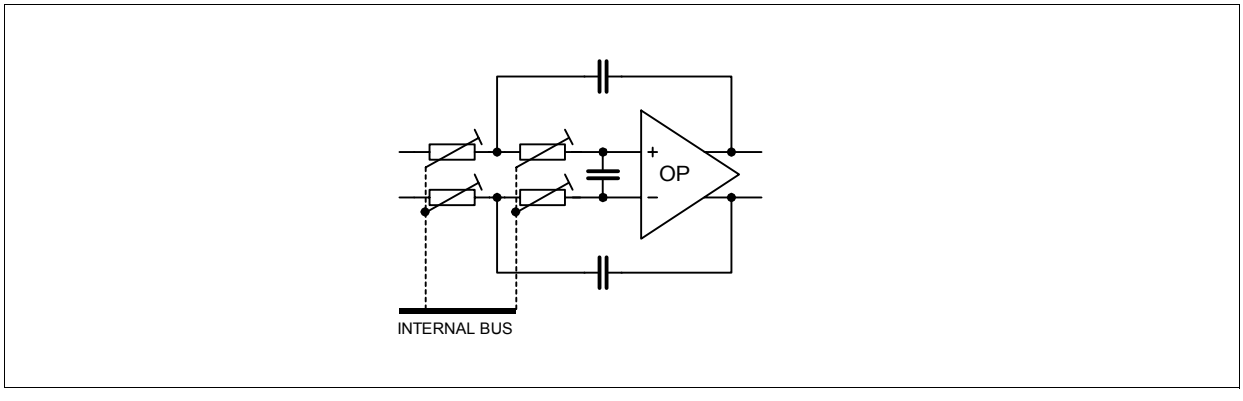
Generally in receive mode the relationship between local oscillator frequency f_{osc}, the receive RF frequency f_{RF} and the IF frequency f_{IF} and thus the frequency that is applied to the I/Q Mixers is given in the following formula:

$$f_{osc} = 4/3\ f_{RF} = 4\ f_{IF} \qquad [2-1]$$

The VCO signal is applied to a divider by 4 which is producing approximately 305MHz signals in quadrature. The overall division ratio of the divider chain following the divider by 4 is 12 in transmit mode and 16 in receive mode as the nominal crystal oscillator frequency is 19.0625MHz. The division ratio is controlled by the **RxTx** pin (pin 5) and the **D10** bit in the **CONFIG** register.

2.4.6 I/Q Filters

The I/Q IF to zero-IF mixers are followed by baseband 6th order low pass filters that are used for RF-channel filtering.



iq_filter.wmf

Figure 2-3 One I/Q Filter stage

The bandwidth of the filters is controlled by the values set in the filter-register. It can be adjusted between 50 and 350kHz in 50kHz steps via the bits D1 to D3 of the **LPF** register (subaddress 03H).

2.4.7 I/Q Limiters

The I/Q Limiters are DC coupled multistage amplifiers with offset-compensating feedback circuit and an overall gain of approximately 80dB each in the frequency range of 100Hz up to 350kHz.

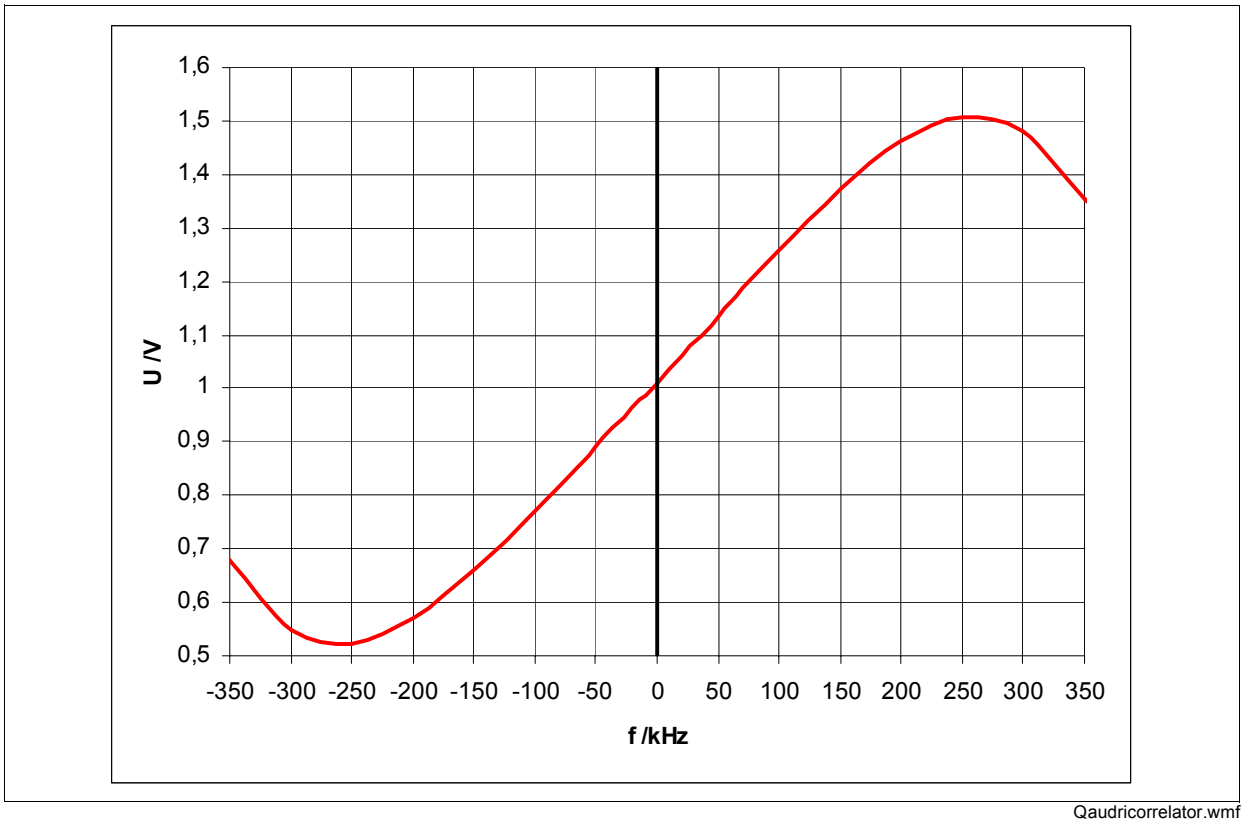
Receive Signal Strength Indicator (RSSI) generators are included in both limiters which produce DC voltages that are directly proportional to the input signal level in the respective channels. The resulting I- and Q-channel RSSI-signals are summed to the nominal RSSI signal.

2.4.8 FSK Demodulator

The output differential signals of the I/Q limiters are fed to a quadrature correlator circuit that is used to demodulate frequency shift keyed (FSK) signals. The demodulator gain is 2.4mV/kHz, the maximum frequency deviation is ±300kHz as shown in **Figure 2-4** below.

The demodulated signal is applied to the ASK/FSK mode switch which is connected to the input of the data filter. The switch can be controlled by the **ASKFSK** pin (pin 4) and via the D11 bit in the CONFIG register.

The modulation index *m* must be significantly larger than 2 and the deviation at least larger than 25kHz for correct demodulation of the signal.

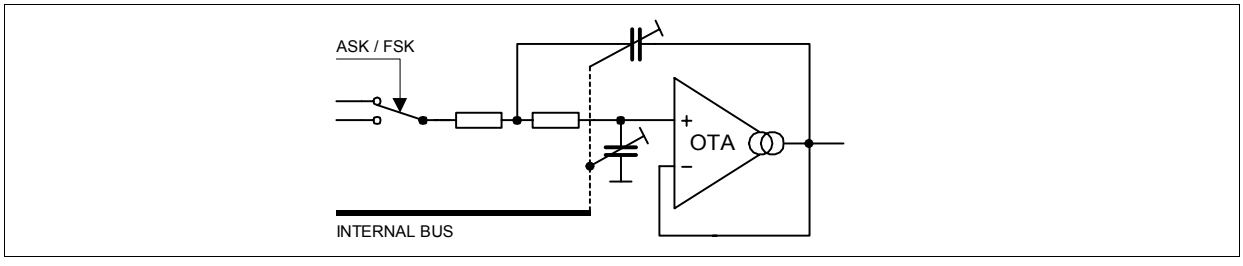


Qaudricorrelator.wmf

Figure 2-4 Typical Quadricorrelator Demodulation Characteristic

2.4.9 Data Filter

The 2-pole data filter has a Sallen-Key architecture and is implemented fully on-chip. The bandwidth can be adjusted between approximately 5kHz and 102kHz via the bits **D4** to **D7** of the **LPF** register (see also Table 2-18).



data_filter.wmf

Figure 2-5 Data Filter architecture

2.4.10 Data Slicer

The data slicer is a fast comparator with a bandwidth of 100kHz. The self-adjusting threshold is generated by a RC-network (LPF) or by use of one or both peak detectors depending on the baseband coding scheme. This can be controlled by the **D15** bit of the **CONFIG** register as shown in the following table.

Table 2-4 Sub Address 00H: CONFIG

Bit	Function	Description	Default
D15	SLICER	0= Lowpass Filter, 1= Peak Detector	0

2.4.11 Peak Detectors

Two separate Peak Detectors are available. They are generating DC voltages in a fast-attack and slow-release manner that are proportional to the positive and negative peak voltages appearing in the data signal. These voltages may be used to generate a threshold voltage for non-Manchester encoded signals, for example. The time-constant of the fast-attack/slow-release action is determined by the RC network with external capacitor.

2.4.12 Crystal Oscillator

The reference oscillator is an NIC oscillator type (Negative Impedance Converter) with a crystal operating in serial resonance. The nominal operating frequency of 19.0625MHz and the frequencies for FSK modulation can be adjusted via 3 external capacitors. Via microcontroller and bus interface the chip-internal capacitors can be used for finetuning of the nominal and the FSK modulation frequencies. This finetuning of the crystal oscillator allows to eliminate frequency errors due to crystal or component tolerances.

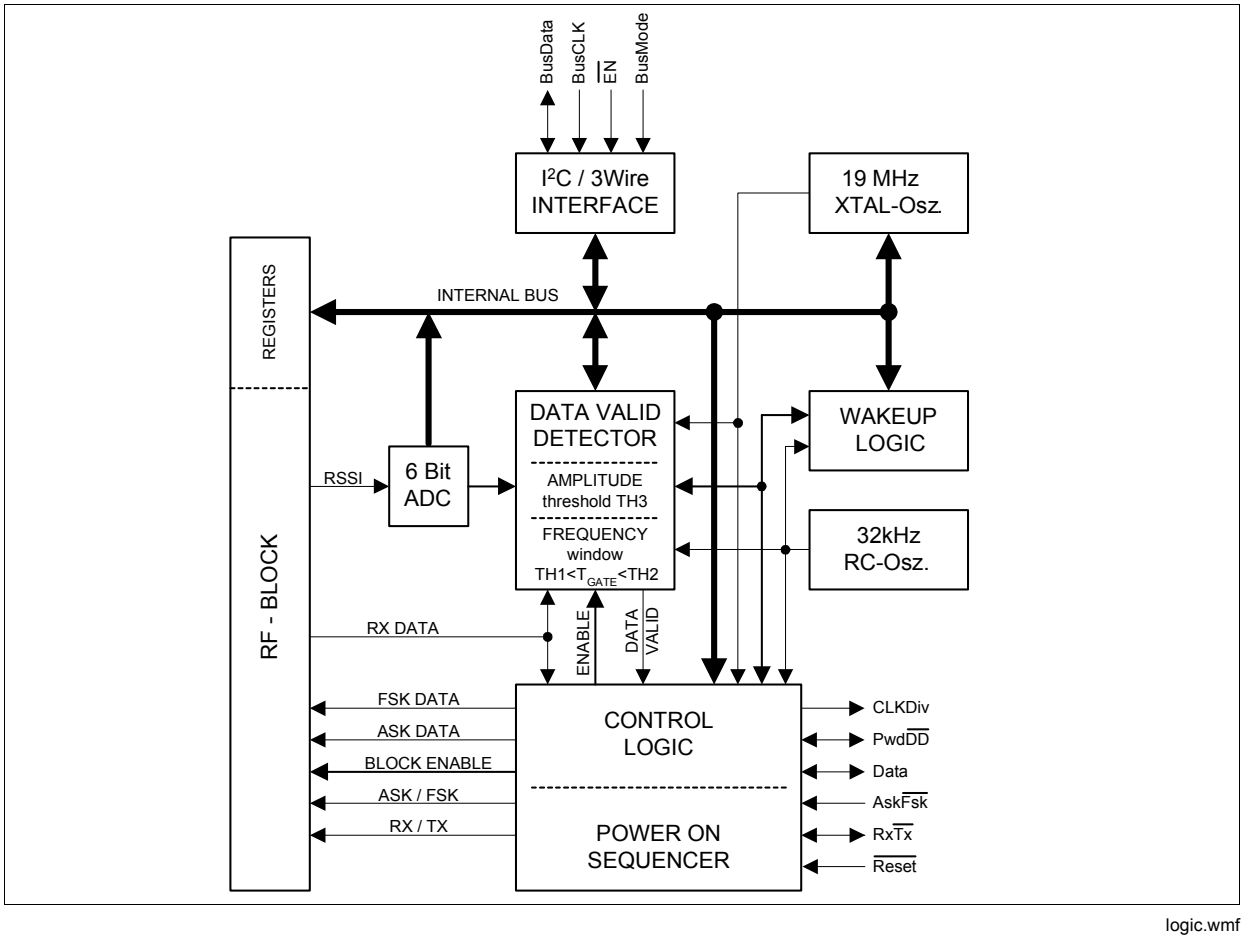
2.4.13 Bandgap Reference Circuitry and Powerdown

A Bandgap Reference Circuit provides a temperature stable 1.2V reference voltage for the device. A power down mode is available to switch off all subcircuits that are controlled by the bidirectional Powerdown&DataDetect **PwdDD** pin (pin 27) as shown in the following table. Power down mode can either be activated by pin 27 or bit D14 in Register 00h. In power down mode also pin 28 (DATA) is affected (see **Section 2.4.17**).

Table 2-5 PwdDD Pin Operating States	
PwdDD	**Operating State**
VDD	Powerdown Mode
Ground/VSS	Device On

2.4.14 Timing and Data Control Unit

The timing and data control unit contains a wake-up logic unit, an I²C/3-wire microcontroller interface, a “data valid” detection unit and a set of configuration registers as shown in the subsequent figure.



logic.wmf

Figure 2-6 Timing and Data Control Unit

The I²C / 3-wire Bus Interface gives an external microcontroller full control over important system parameters at any time.

It is possible to set the device in three different modes: Slave Mode, Self Polling Mode and Timer Mode. This is done by a state machine which is implemented in the WAKEUP LOGIC unit. A detailed description is given in **Section 2.4.16**.

The DATA VALID DETECTOR contains a frequency window counter and an RSSI threshold comparator. The window counter uses the incoming data signal from the data slicer as the gating signal and the crystal oscillator frequency as the timebase to determine the actual datarate. The result is compared with the expected datarate.
The threshold comparator compares the actual RSSI level with the expected RSSI level.

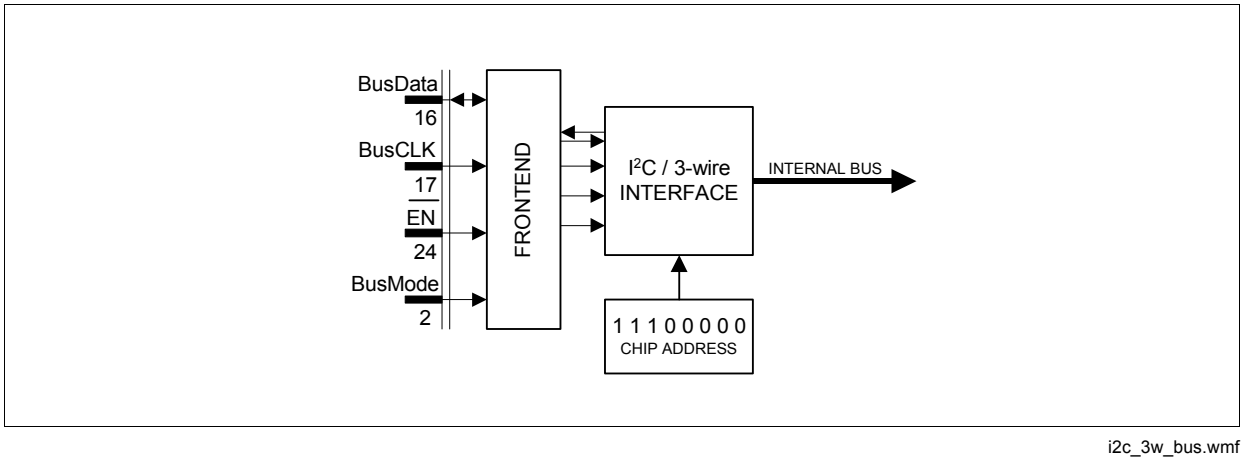
If both conditions are true the **PwdDD** pin is set to LOW in self polling mode as you can see in **Section 2.4.16**. This signal can be used as an interrupt for an external µP. Because the **PwdDD** pin is bidirectional and open drain driven by an internal pull-up resistor it is possible to apply an external LOW thus enabling the device.

2.4.15 Bus Interface and Register Definition

The TDA5252 supports the I^2C bus protocol (2 wire) and a 3-wire bus protocol. Operation is selectable by the **BusMode** pin (pin 2) as shown in the following table. All bus pins (BusData, BusCLK, **EN**, BusMode) have a Schmitt-triggered input stage. The BusData pin is bidirectional where the output is open drain driven by an internal 15kΩ pull up resistor.

Table 2-6 Bus Interface Format

Function	BusMode	EN	BusCLK	BusData
I^2C Mode	Low	High= inactive, Low= active	Clock input	Data in/out
3-wire Mode	High			



i2c_3w_bus.wmf

Figure 2-7 Bus Interface

Note: The Interface is able to access the internal registers at any time, even in POWER DOWN mode. There is no internal clock necessary for Interface operation.

I²C Bus Mode

In this mode the **BusMode** pin (pin 2) = LOW and the **$\overline{\text{EN}}$** pin (pin 24) = LOW.

Data Transition:

Data transition on the pin BusData can only occur when BusCLK is LOW. BusData transitions while BusCLK is HIGH will be interpreted as start or stop condition.

Start Condition (STA):

A start condition is defined by a HIGH to LOW transition of the BusData line while BusCLK is HIGH. This start condition must precede any command and initiate a data transfer onto the bus.

Stop Condition (STO):

A stop condition is defined by a LOW to HIGH transition of the BusData line while BusCLK is HIGH. This condition terminates the communication between the devices and forces the bus interface into the initial state.

Acknowledge (ACK):

Indicates a successful data transfer. The transmitter will release the bus after sending 8 bit of data. During the 9th clock cycle the receiver will set the SDA line to LOW level to indicate it has received the 8 bits of data correctly.

Data Transfer Write Mode:

To start the communication, the bus master must initiate a start condition (STA), followed by the 8bit chip address. The chip address for the TDA5252 is fixed as „1110000“ (MSB at first). The last bit (LSB=A0) of the chip address byte defines the type of operation to be performed:

A0=0, a write operation is selected and A0=1 a read operation is selected.

After this comparison the TDA5252 will generate an ACK and awaits the desired sub address byte (00H...0FH) and data bytes. At the end of the data transition the master has to generate the stop condition (STO).

Data Transfer Read Mode:

To start the communication in the read mode, the bus master must initiate a start condition (STA), followed by the 8 bit chip address (write: A0=0), followed by the sub address to read (80H, 81H), followed by the chip address (read: A0=1). After that procedure the data of the selected register (80H, 81H) is read out. During this time the data line has to be kept in HIGH state and the chip sends out the data. At the end of data transition the master has to generate the stop condition (STO).

Bus Data Format in I²C Mode

Table 2-7 Chip address Organization

MSB							LSB	Function
1	1	1	0	0	0	0	0	Chip Address Write
1	1	1	0	0	0	0	1	Chip Address Read

Table 2-8 I²C Bus Write Mode 8 Bit

	MSB	CHIP ADDRESS (WRITE)						LSB		MSB	SUB ADDRESS (WRITE) 00H...08H, 0DH, 0EH, 0FH						LSB		MSB	DATA IN							LSB		
STA	1	1	1	0	0	0	0	0	ACK	S7	S6	S5	S4	S3	S2	S1	S0	ACK	D7	D6	D5	D4	D3	D2	D1	D0	ACK	STO

Table 2-9 I²C Bus Write Mode 16 Bit

	MSB	CHIP ADDRESS (WRITE)						LSB		MSB	SUB ADDRESS (WRITE) 00H...08H, 0DH, 0EH, 0FH						LSB		MSB	DATA IN							LSB		
STA	1	1	1	0	0	0	0	**0**	ACK	S7	S6	S5	S4	S3	S2	S1	S0	ACK	D15	...	D8	ACK	D7	D6	...	D0	ACK	STO

Table 2-10 I²C Bus Read Mode

	MSB	CHIP ADDRESS (WRITE)						LSB		MSB	SUB ADDRESS (READ) 80H, 81H						LSB			MSB	CHIP ADDRESS (READ)						LSB	
STA	1	1	1	0	0	0	0	**0**	ACK	S7	S6	S5	S4	S3	S2	S1	S0	ACK	STA	1	1	1	0	0	0	0	**1**	ACK

Table 2-10 I²C Bus Read Mode (continued)

MSB	DATA OUT FROM SUB ADDRESS							LSB		
R7	R6	R5	R4	R3	R2	R1	R0	ACK*	STO	

* mandatory HIGH

3-wire Bus Mode

In this mode pin 2 (BusMode)= HIGH and Pin 16 (BusData) is in the data input/output pin. Pin 24 ($\overline{EN}$) is used to activate the bus interface to allow the transfer of data to / from the device. When pin 24 ($\overline{EN}$) is inactive (HIGH), data transfer is inhibited.

Data Transition:

Data transition on pin 16 (BusData) can only occur if the clock BusCLK is LOW. To perform a data transfer the interface has to be enabled. This is done by setting the $\overline{EN}$ line to LOW. A serial transfer is done via BusData, BusCLK and $\overline{EN}$. The bit stream needs no chip address.

Data Transfer Write Mode:

To start the communication the $\overline{EN}$ line has to be set to LOW. The desired sub address byte and data bytes have to follow. The subaddress (00H...0FH) determines which of the data bytes are transmitted. At the end of data transition the $\overline{EN}$ must be HIGH.

Data transfer Read Mode:

To start the communication in the read mode, the $\overline{EN}$ line has to be set to LOW followed by the sub address to read (80H, 81H). Afterwards the device is ready to read out data. At the end of data transition $\overline{EN}$ must be HIGH.

Bus Data Format 3-wire Bus Mode

Table 2-11 3-wire Bus Write Mode

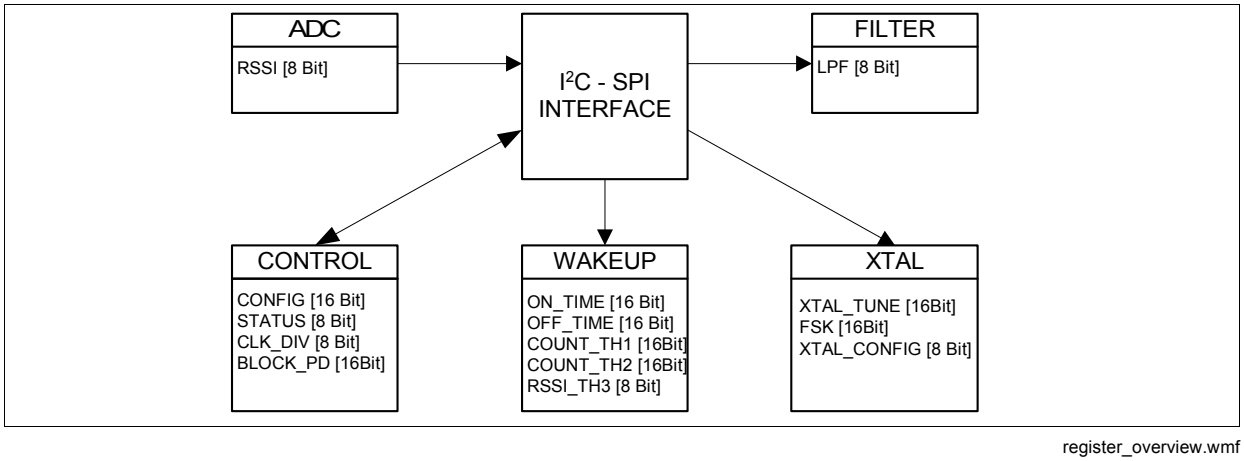
MSB	SUB ADDRESS (WRITE) 00H...08H, 0DH, 0EH,0FH						LSB	MSB	DATA IN X...0 (X=7 or 15)						LSB
S7	S6	S5	S4	S3	S2	S1	S0	DX	...	D5	D4	D3	D2	D1	D0

Table 2-12 3-wire Bus Read Mode

MSB	SUB ADDRESS (READ) 80H, 81H						LSB	MSB	DATA OUT FROM SUB ADDRESS						LSB
S7	S6	S5	S4	S3	S2	S1	S0	R7	R6	R5	R4	R3	R2	R1	R0

Register Definition

Sub Addresses Overview



register_overview.wmf

Figure 2-8 Sub Addresses Overview

Subaddress Organization

Table 2-13 Sub Addresses of Data Registers Write

MSB							LSB	HEX	Function	Description	Bit Length
0	0	0	0	0	0	0	0	00h	CONFIG	General definition of status bits	16
0	0	0	0	0	0	0	1	01h	FSK	Values for FSK-shift	16
0	0	0	0	0	0	1	0	02h	XTAL_TUNING	Nominal frequency	16
0	0	0	0	0	0	1	1	03h	LPF	I/Q and data filter cutoff frequencies	8
0	0	0	0	0	1	0	0	04h	ON_TIME	ON time of wakeup counter	16
0	0	0	0	0	1	0	1	05h	OFF_TIME	OFF time of wakeup counter	16
0	0	0	0	0	1	1	0	06h	COUNT_TH1	Lower threshold of window counter	16
0	0	0	0	0	1	1	1	07h	COUNT_TH2	Higher threshold of window counter	16
0	0	0	0	1	0	0	0	08h	RSSI_TH3	Threshold for RSSI signal	8
0	0	0	0	1	1	0	1	0Dh	CLK_DIV	Configuration and Ratio of clock divider	8
0	0	0	0	1	1	1	0	0Eh	XTAL_CONFIG	XTAL configuration	8
0	0	0	0	1	1	1	1	0Fh	BLOCK_PD	Building Blocks Power Down	16

Table 2-14 Sub Addresses of Data Registers Read

MSB							LSB	HEX	Function	Description	Bit Length
1	0	0	0	0	0	0	0	80h	STATUS	Results of comparison: ADC & WINDOW	8
1	0	0	0	0	0	0	1	81h	ADC	ADC data out	8

Data Byte Specification

Table 2-15 Sub Address 00H: CONFIG

Bit	Function	Description	Default
D15	SLICER	0= Lowpass, 1= Peak Detector	0
D14	ALL_PD	0= normal operation, 1= all Power down	0
D13	TESTMODE	0= normal operation, 1=Testmode	0
D12	CONTROL	0= RX/TX and ASK/FSK external controlled, 1= Register controlled	0
D11	ASK_NFSK	0= FSK, 1=ASK	0
D10	RX_NTX	0= TX, 1=RX	1
D9	CLK_EN	0= CLK off during power down, 1= always CLK on, ever in PD	0
D8	RX_DATA_INV	0= no Data inversion, 1= Data inversion	0
D7	D_OUT	0= Data out if valid, 1= always Data out	1
D6	ADC_MODE	0= one shot, 1= continuous	1
D5	F_COUNT_MODE	0= one shot, 1= continuous	1
D4	LNA_GAIN	0= low gain, 1= high gain	1
D3	EN_RX	0= disable receiver, 1= enable receiver (in self polling and timer mode) *	1
D2	MODE_2	0= slave mode, 1= timer mode	0
D1	MODE_1	0= slave or timer mode, 1= self polling mode	0
D0	PA_PWR	0= low TX Power, 1= high TX Power	1

Note D3: Function is only active in selfpolling and timer mode. When D3 is set to LOW the RX path is not enabled if PwdDD pin is set to LOW. A delayed setting of D3 results in a delayed power ON of the RX building blocks.

Table 2-16	Sub Address 01H: FSK			
Bit	Function	Value	Description	Default
D15			not used	0
D14			not used	0
D13	FSK+5	8pF	Setting for positive frequency shift: +FSK or ASK-RX	0
D12	FSK+4	4pF		0
D11	FSK+3	2pF		1
D10	FSK+2	1pF		0
D9	FSK+1	500fF		1
D8	FSK+0	250fF		0
D7			not used	0
D6			not used	0
D5	FSK-5	4pF	Setting for negative frequency shift: -FSK	0
D4	FSK-4	2pF		0
D3	FSK-3	1pF		1
D2	FSK-2	500fF		1
D1	FSK-1	250fF		0
D0	FSK-0	125fF		0

Table 2-17	Sub Address 02H: XTAL_TUNING			
Bit	Function	Value	Description	Default
D15			not used	0
D14			not used	0
D13			not used	0
D12			not used	0
D11			not used	0
D10			not used	0
D9			not used	0
D8			not used	0
D7			not used	0
D6			not used	0
D5	Nominal_Frequ_5	8pF	Setting for nominal frequency ASK-TX FSK-RX	0
D4	Nominal_Frequ_4	4pF		1
D3	Nominal_Frequ_3	2pF		0
D2	Nominal_Frequ_2	1pF		0
D1	Nominal_Frequ_1	500fF		1
D0	Nominal_Frequ_0	250fF		0

Table 2-18	Sub Address 03H: LPF		
Bit	Function	Description	Default
D7	Datafilter_3	3dB cutoff frequency of data filter	0
D6	Datafilter_2		0
D5	Datafilter_1		0
D4	Datafilter_0		1
D3	IQ_Filter_2	3dB cutoff frequency of IQ-filter	1
D2	IQ_Filter_1		0
D1	IQ_Filter_0		0
D0	not used		0

Table 2-19	Sub Addresses 04H / 05H: ON/OFF_TIME		
Bit	Function	Default ON_TIME	Default OFF_TIME
D15	ON_15 / OFF_15	1	1
D14	ON_14 / OFF_14	1	1
D13	ON_13 / OFF_13	1	1
D12	ON_12 / OFF_12	1	1
D11	ON_11 / OFF_11	1	0
D10	ON_10 / OFF_10	1	0
D9	ON_9 / OFF_9	1	1
D8	ON_8 / OFF_8	0	1
D7	ON_7 / OFF_7	1	1
D6	ON_6 / OFF_6	1	0
D5	ON_5 / OFF_5	0	0
D4	ON_4 / OFF_4	0	0
D3	ON_3 / OFF_3	0	0
D2	ON_2 / OFF_2	0	0
D1	ON_1 / OFF_1	0	0
D0	ON_0 / OFF_0	0	0

Table 2-20	Sub Address 06H: COUNT_TH1	
Bit	Function	Default
D15	not used	0
D14	not used	0
D13	not used	0
D12	not used	0
D11	TH1_11	0
D10	TH1_10	0
D9	TH1_9	0
D8	TH1_8	0
D7	TH1_7	0
D6	TH1_6	0
D5	TH1_5	0
D4	TH1_4	0
D3	TH1_3	0
D2	TH1_2	0
D1	TH1_1	0
D0	TH1_0	0

Table 2-21	Sub Address 07H: COUNT_TH2	
Bit	Function	Default
D15	not used	0
D14	not used	0
D13	not used	0
D12	not used	0
D11	TH2_11	0
D10	TH2_10	0
D9	TH2_9	0
D8	TH2_8	0
D7	TH2_7	0
D6	TH2_6	0
D5	TH2_5	0
D4	TH2_4	0
D3	TH2_3	0
D2	TH2_2	0
D1	TH2_1	0

Table 2-22	Sub Address 08H: RSSI_TH3		
Bit	**Function**	**Description**	**Default**
D7	not used		1
D6	SELECT	0= VCC, 1= RSSI	1
D5	TH3_5		1
D4	TH3_4		1
D3	TH3_3		1
D2	TH3_2		1
D1	TH3_1		1
D0	TH3_0		1

Table 2-23	Sub Address 0DH: CLK_DIV	
Bit	**Function**	**Default**
D7	not used	0
D6	not used	0
D5	DIVMODE_1	0
D4	DIVMODE_0	0
D3	CLKDIV_3	1
D2	CLKDIV_2	0
D1	CLKDIV_1	0
D0	CLKDIV_0	0

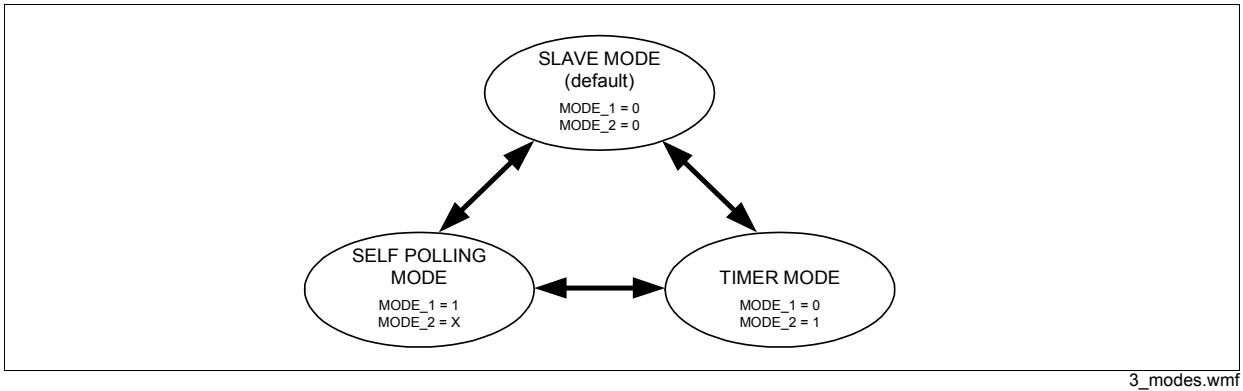
Table 2-24	Sub Address 0EH: XTAL_CONFIG		
Bit	**Function**	**Description**	**Default**
D7		not used	0
D6		not used	0
D5		not used	0
D4		not used	0
D3		not used	0
D2	FSK-Ramp 0	only in bipolar mode	0
D1	FSK-Ramp 1		0
D0	Bipolar_FET	0= FET, 1=Bipolar	1

Table 2-25	Sub Address 0FH: BLOCK_PD		
Bit	**Function**	**Description**	**Default**
D15	REF_PD	1= power down Band Gap Reference	1
D14	RC_PD	1= power down RC Oscillator	1
D13	WINDOW_PD	1= power down Window Counter	1
D12	ADC_PD	1= power down ADC	1
D11	PEAK_DET_PD	1= power down Peak Detectors	1
D10	DATA_SLIC_PD	1= power down Data Slicer	1
D9	DATA_FIL_PD	1= power down Data Filter	1
D8	QUAD_PD	1= power down Quadri Correlator	1
D7	LIM_PD	1= power down Limiter	1
D6	I/Q_FIL_PD	1= power down I/Q Filters	1
D5	MIX2_PD	1= power down I/Q Mixer	1
D4	MIX1_PD	1= power down 1st Mixer	1
D3	LNA_PD	1= power down LNA	1
D2	PA_PD	1= power down Power Amplifier	1
D1	PLL_PD	1= power down PLL	1
D0	XTAL_PD	1= power down XTAL Oscillator	1

Table 2-26	Sub Address 80H: STATUS	
Bit	**Function**	**Description**
D7	COMP_LOW	1 if data rate < TH1
D6	COMP_IN	1 if TH1 < data rate < TH2
D5	COMP_HIGH	1 if TH2 < data rate
D4	COMP_0,5*LOW	1 if data rate < 0,5*TH1
D3	COMP_0,5*IN	1 if 0,5*TH1 < data rate < 0,5*TH2
D2	COMP_0,5*HIGH	1 if 0,5*TH2 < data rate
D1	RSSI=TH3	1 if RSSI value is equal TH3
D0	RSSI>TH3	1 if RSSI value is greater than TH3

Table 2-27	Sub Address 81H: ADC	
Bit	**Function**	**Description**
D7	PD_ADC	ADC power down feedback Bit
D6	SELECT	SELECT feedback Bit
D5	RSSI_5	RSSI value Bit5
D4	RSSI_4	RSSI value Bit4
D3	RSSI_3	RSSI value Bit3
D2	RSSI_2	RSSI value Bit2
D1	RSSI_1	RSSI value Bit1
D0	RSSI_0	RSSI value Bit0

2.4.16 Wakeup Logic



3_modes.wmf

Figure 2-9 Wakeup Logic States

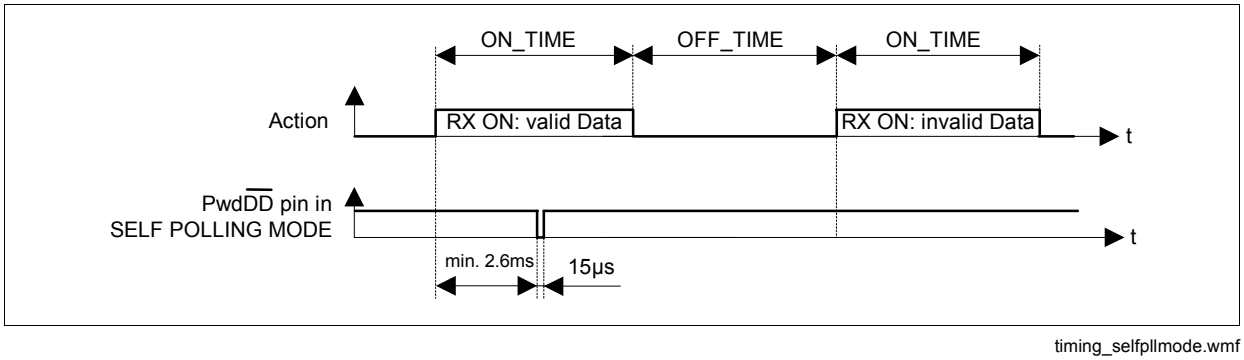
Table 2-28 MODE settings: CONFIG register

MODE_1	MODE_2	Mode
0	0	SLAVE MODE
0	1	TIMER MODE
1	X	SELF POLLING MODE

SLAVE MODE: The receive and transmit operation is fully controlled by an external control device via the respective **RxTx**, **AskFsk**, **PwdDD**, and **Data** pins. The wakeup logic is inactive in this case.

After RESET or 1st Power-up the chip is in SLAVE MODE. By setting MODE_1 and MODE_2 in the CONFIG register the mode may be changed.

SELF POLLING MODE: The chip turns itself on periodically to receive using a built-in 32kHz RC oscillator. The timing of this is determined by the **ON_TIME** and **OFF_TIME** registers, the duty cycle can be set between 0 and 100% in 31.25µs increments. The data detect logic is enabled and a 15µs LOW impulse is provided at **PwdDD** pin (Pin 27), if the received data is valid.



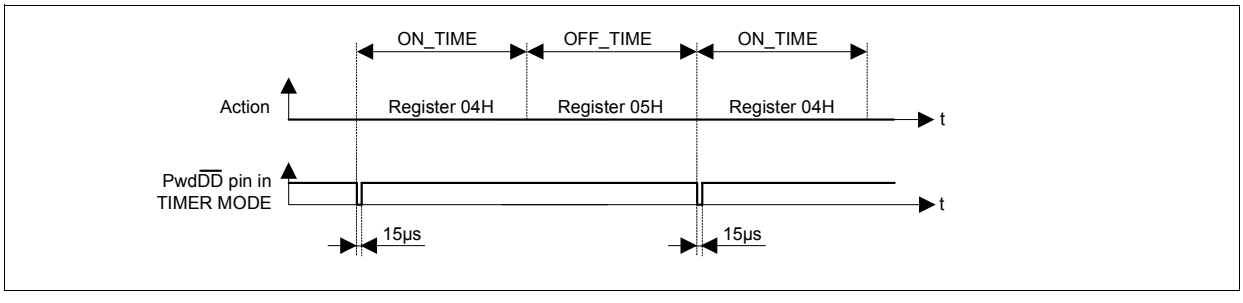
timing_selfpllmode.wmf

Figure 2-10 Timing for Self Polling Mode (ADC & Data Detect in one shot mode)

Note: The time delay between start of ON time and the 15µs LOW impulse is 2.6ms + 3 period of data rate.

If ADC & Data Detect Logic are in continuous mode the 15µs LOW impulse is applied at **PwdDD** after each data valid decision.
In self polling mode if D9=0 (Register 00h) and when **PwdDD** pin level is HIGH the CLK output is on during ON time and off during OFF time. If D9=1, the CLK output is always on.

TIMER MODE: Only the internal Timer (determined by the **ON_TIME** and **OFF_TIME** registers) is active to support an external logic with periodical Interrupts. After ON_TIME + OFF_TIME a 15µs LOW impulse is applied at the **PwdDD** pin (Pin 27).

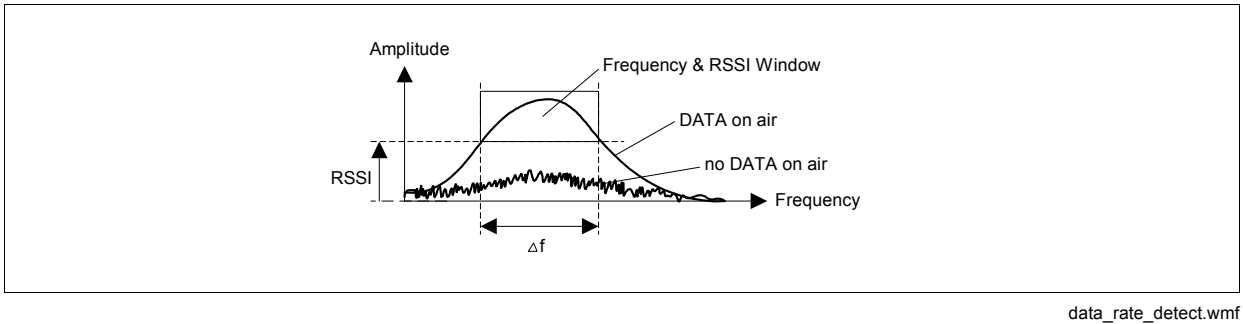


timing_timermode.wmf

Figure 2-11 Timing for Timer Mode

2.4.17 Data Valid Detection, Data Pin

Data signals generate a typical spectrum and this can be used to determine if valid data is on air.

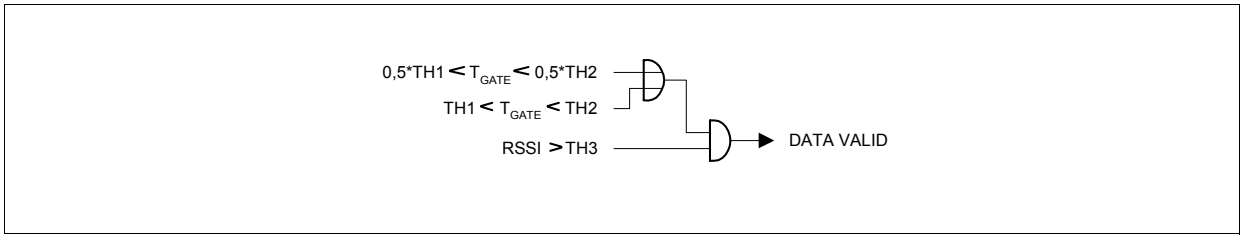


data_rate_detect.wmf

Figure 2-12 Frequency and RSSI Window

The “data valid” criterion is generated from the result of RSSI-TH3 comparison and t_{GATE} between TH1 and TH2 result as shown below. In case of Manchester coding the 0,5*TH1 and 0,5*TH2 gives improved performance.

The use of permanent data valid recognition makes it absolutely necessary to set the RSSI-ADC and the Window counter into continuous mode (Register 00H, Bit D5 = D6 = 1).

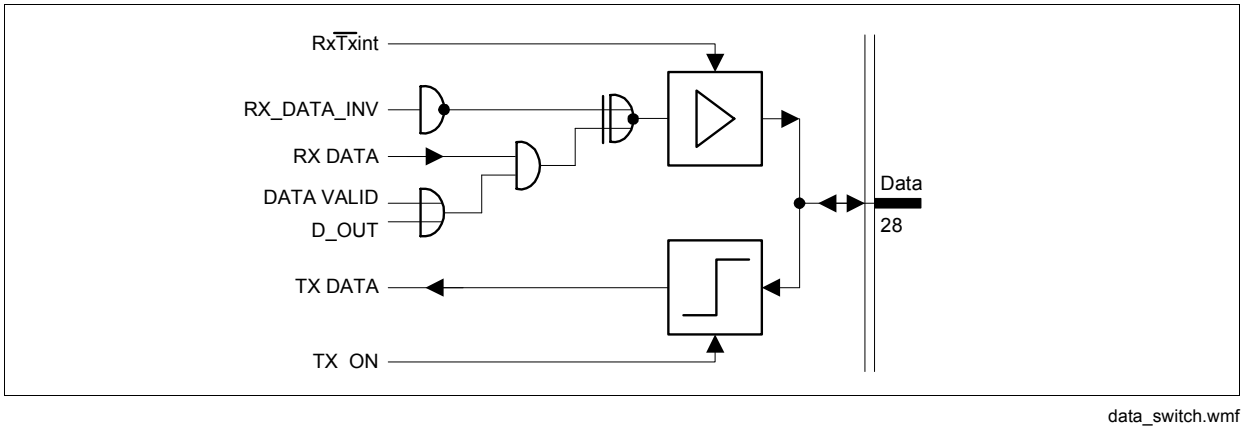


data_valid.wmf

Figure 2-13 Data Valid Circuit

D_OUT and RX_DATA_INV from the CONFIG register determine the output of data at Pin 28. **RxTxint** and TX_ON are internally generated signals.

In RX and power down mode Data pin (Pin 28) is tied to GND.



data_switch.wmf

Figure 2-14 Data Input/Output Circuit

2.4.18 Sequence Timer

The sequence timer has to control all the enable signals of the analog components inside the chip. The time base is the 32 kHz RC oscillator.

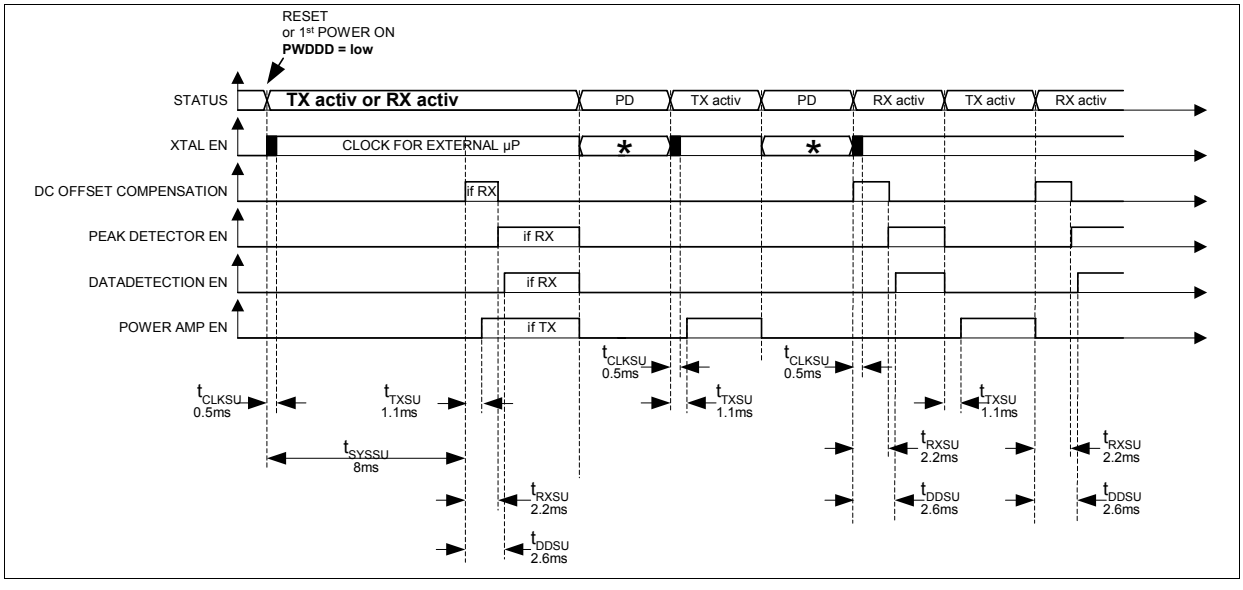
After the first POWER ON or RESET a 1.06MHz clock is available at the clock output pin. This clock output can be used by an external µP to set the system into the desired state and outputs valid data after 500 µs (see **Figure 2-15** and **Figure 2-16**, t_{CLKSU})

There are two possibilities to start the device after a reset or first power on:

- PWDDD pin is LOW: Normal operation timing is performed after t_{SYSSU} (see **Figure 2-15**).
- PWDDD pin is HIGH (device in power down mode): A clock is offered at the clock output pin until the device is activated (PWDDD pin is pulled to LOW). After the first activation the time t_{SYSSU} is required until normal operation timing is performed (see **Figure 2-16**).
  This could be used to extend the clock generation without device programming or activation.

Note: It is **required** to activate the device for the duration of t_{SYSSU} after first power on or a reset. Only if this is done the normal operation timing is performed.

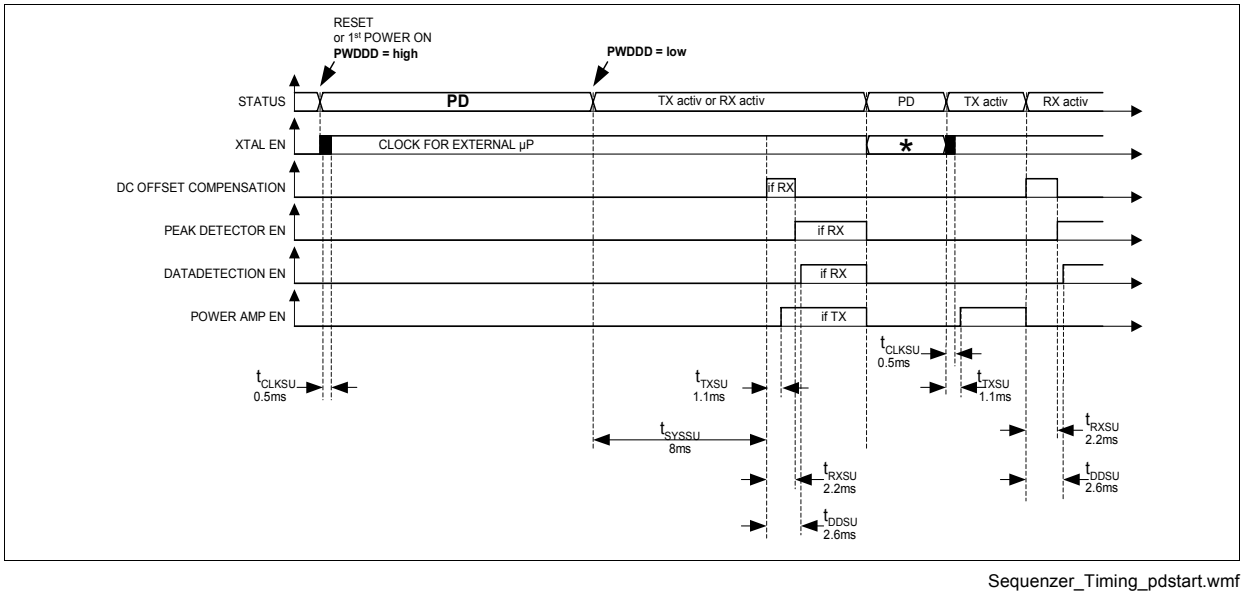
With default settings the clock generating units are disabled during PD, therefore no clock is available at the clock output pin. It is possible to offer a clock signal at the clock output pin every time (also during PD) if the CLK_EN Bit in the CONFIG register is set to HIGH.



Sequenzer_Timing_pupstart.wmf

Figure 2-15 1st start or reset in active mode

Note: The time values are typical values



Sequenzer_Timing_pdstart.wmf

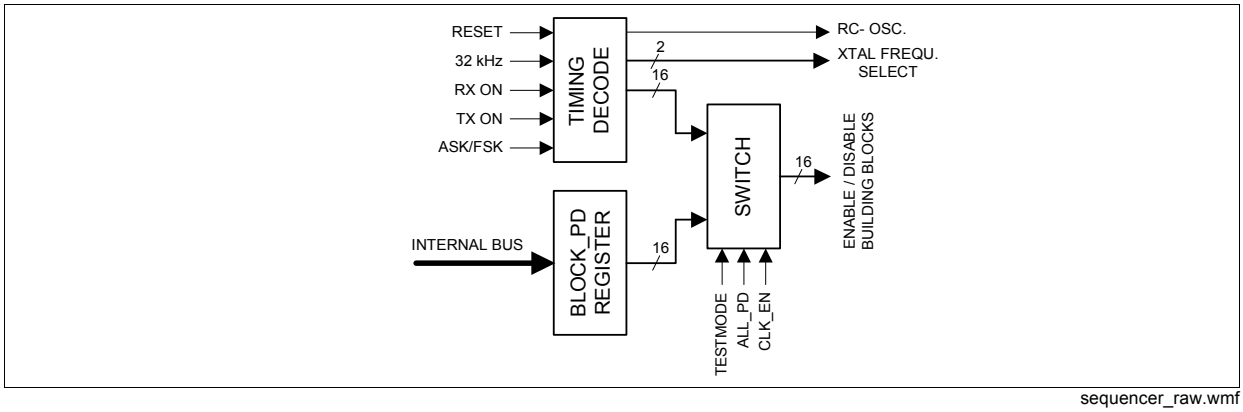
Figure 2-16 1st start or reset in PD mode

* State is either „I“ or „O“ depending on time of setting into powerdown.

Note: The time values are typical values

This means that the device needs t_{DDSU} setup time to start the data detection after RX is activated. When activating TX it requires t_{TXSU} setup time to enable the power amplifier.
For timing information refer to **Table 4-3**.

For test purposes a TESTMODE is provided by the Sequencer as well. In this mode the BLOCK_PD register be set to various values. This will override the Sequencer timing. Depending on the settings in Config Register 00H the corresponding building blocks are enabled, as shown in the subsequent figure.

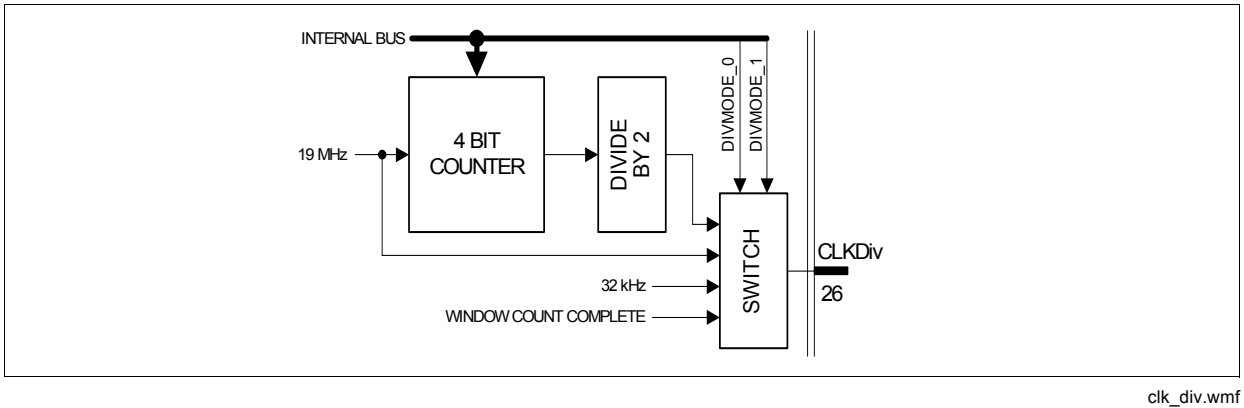


sequencer_raw.wmf

Figure 2-17 Sequencer‘s capability

2.4.19 Clock Divider

It supports an external logic with a programmable Clock at **pin 26 (CLKDIV)**.



clk_div.wmf

Figure 2-18 Clock Divider

The Output Selection and Divider Ratio can be set in the CLK_DIV register.

Table 2-29 CLK_DIV Output Selection		
D5	**D4**	**Output**
0	0	Output from Divider (default)
0	1	19.0625MHz
1	0	32kHz
1	1	Window Count Complete

Note: Data are valid 500 µs after the crystal oscillator is enabled (see **Figure 2-15** and **Figure 2-16**, t_{CLKSU}).

Table 2-30 CLK_DIV Setting					
D3	**D2**	**D1**	**D0**	**Total Divider Ratio**	**Output Frequency [MHz]**
0	0	0	0	2	9.53
0	0	0	1	4	4.77
0	0	1	0	6	3.18
0	0	1	1	8	2.38
0	1	0	0	10	1.91
0	1	0	1	12	1.59
0	1	1	0	14	1.36
0	1	1	1	16	1.19
1	0	0	0	18	1.06 (default)
1	0	0	1	20	0.95
1	0	1	0	22	0.87
1	0	1	1	24	0.79
1	1	0	0	26	0.73
1	1	0	1	28	0.68
1	1	1	0	30	0.64
1	1	1	1	32	0.6

Note: As long as default settings are used, there is no clock available at the clock output during Power Down. It is possible to enable the clock during Power Down by setting CLK_EN (Bit D9) in the Config Register (00H) to HIGH.

2.4.20 RSSI and Supply Voltage Measurement

The input of the 6Bit-ADC can be switched between two different sources: the RSSI voltage (default setting) or a resistor network dividing the Vcc voltage by 5.

Table 2-31 Source for 6Bit-ADC Selection (Register 08H)	
SELECT	**Input for 6Bit-ADC**
0	Vcc / 5
1	RSSI (default)

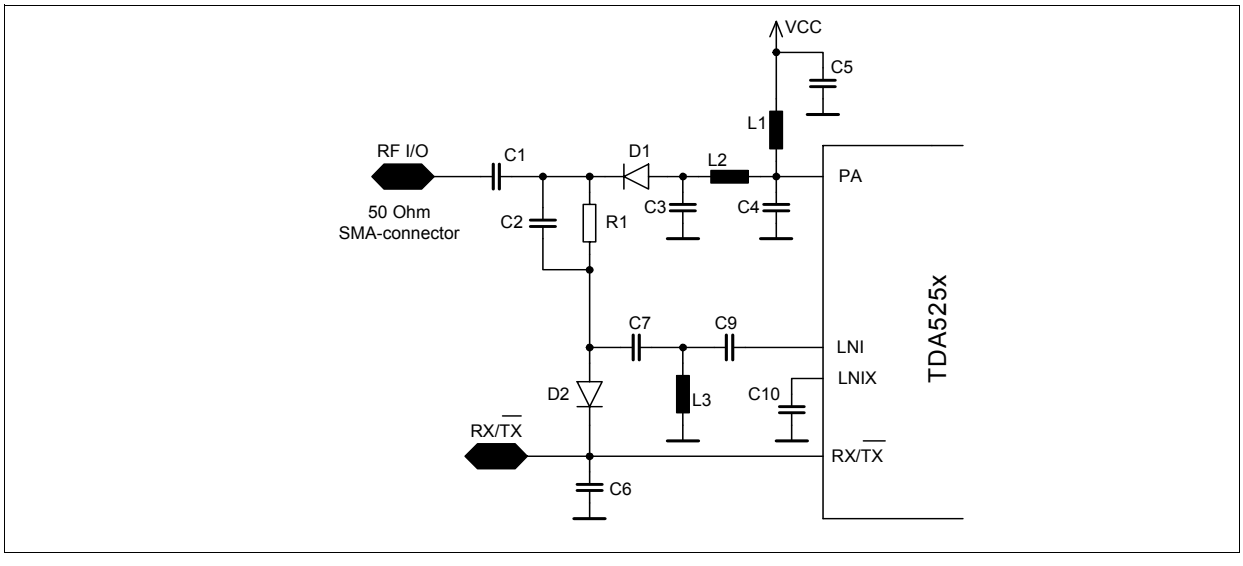
To prevent wrong interpretation of the ADC information (read from Register 81H: ADC) you can use the ADC- Power Down feedback Bit (D7) and the SELECT feedback Bit (D6) which correspond to the actual measurement.

Note: As shown in **Section 2.4.18** there is a setup time of 2.6ms after RX activating. Thus the measurement of RSSI voltage does only make sense after this setup time.

3 Application

3.1 LNA and PA Matching

3.1.1 RX/TX Switch



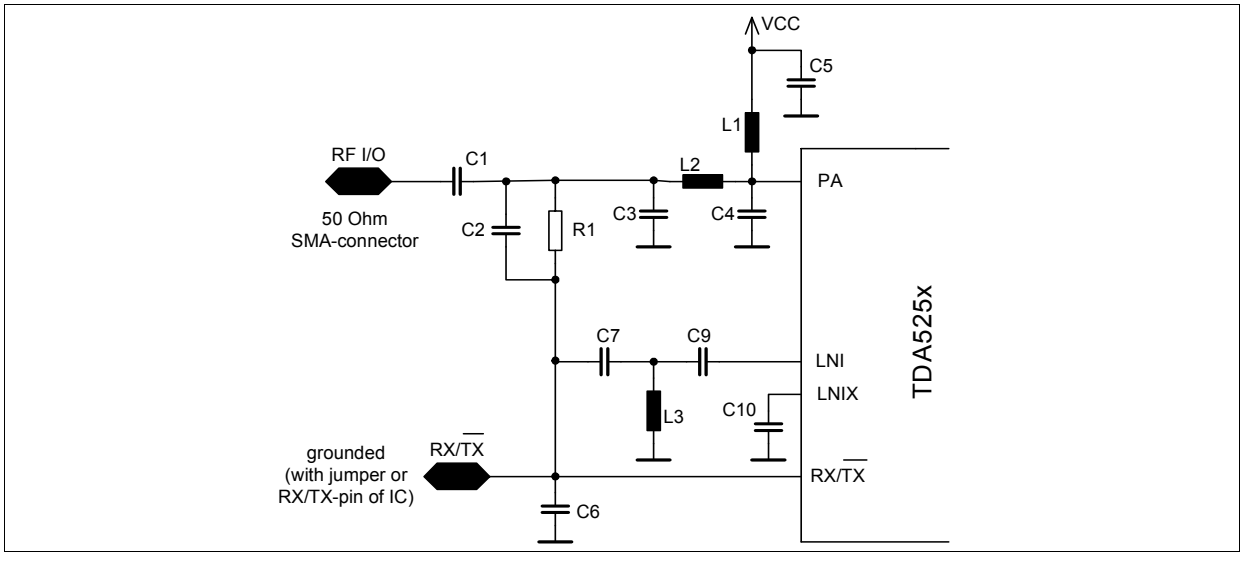
RX/TX_Switch.wmf

Figure 3-1 RX/TX Switch

The RX/TX-switch combines the PA-output and the LNA-input into a single 50 Ohm SMA-connector. Two pin-diodes are used as switching elements. If no current flows through a pin diode, it works as a high impedance for RF with very low capacitance. If the pin-diode is forward biased, it provides a low impedance path for RF. (some Ω)

3.1.2 Switch in RX-Mode

The RX/TX-switch is set to the receive mode by either applying a high level or an open to the RX/TX-jumper on the evalboard or by leaving it open. Then both pin-diodes are not biased and therefore have a high impedance.

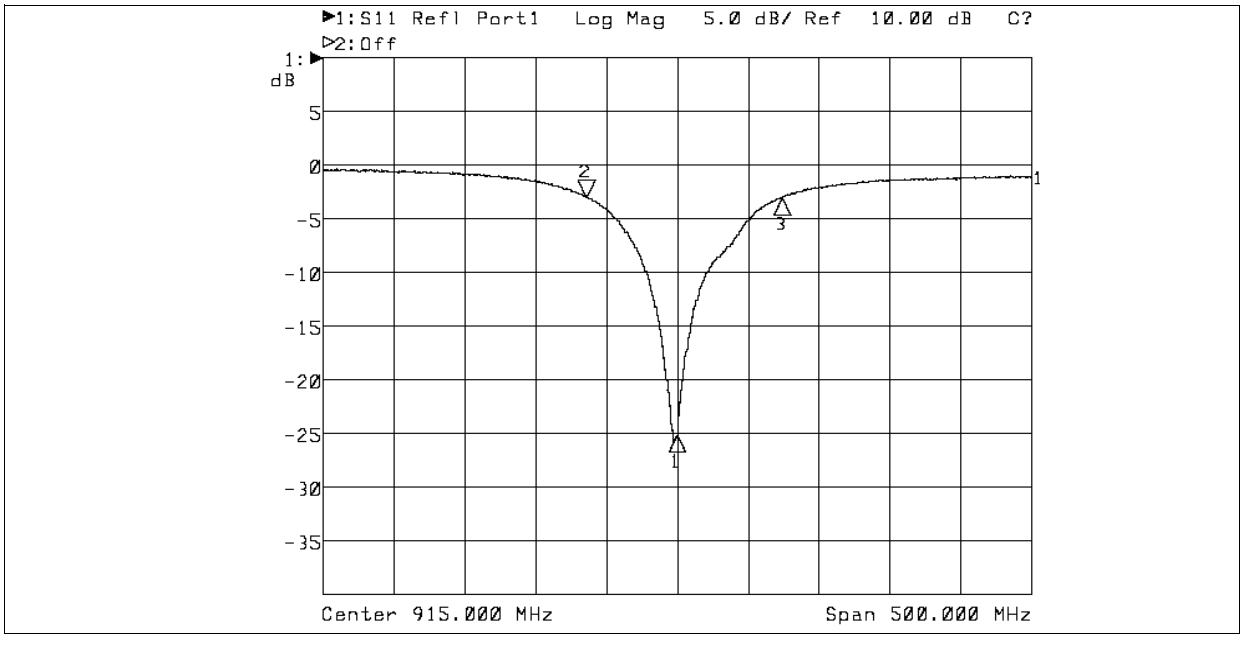


RX_Mode.wmf

Figure 3-2 RX-Mode

The RF-signal is able to run from the RF-input-SMA-connector to the LNA-input-pin LNI via C1, C2, C7, L3 and C9. R1 does not affect the matching circuit due to its high resistance. The other input of the differential LNA LNIX can always be AC-grounded using a large capacitor without any loss of performance. In this case the differential LNA can be used as a single ended LNA, which is easier to match. The S11 of the LNA at pin LNI on the evalboard is 0.931 / -44° (equals a resistor of 1.2kOhm in parallel to a capacitor of 1.4pF) for both high and low-gain-mode of the LNA. (pin LNIX AC-grounded) This impedance has to be matched to 50 Ohm with the parts C9, L3, C7 and C2. C1 is a DC-decoupling-capacitor. On the evalboard the most important matching components are (shunt) L3 and (series)C7, C2. The capacitors is mainly a DC-decoupling-capacitor and may be used for some fine tuning of the matching circuit. A good CAE tool (featuring smith-chart) may be used for the calculation of the values of the components. However, the final values of the matching components always have to be found on the board because of the parasitics of the board, which highly influence the matching circuit at RF.

Measured Magnitude of S11 of evalboard:



S11_measured_915.pcx.

Figure 3-3 S11 measured

Above you can see the measured S11 of the evalboard. The –3dB-points are at 851MHz and 989MHz. So the 3dB-bandwidth is:

$$B = f_U - f_L = 989MHz - 851MHz = 138MHz \quad [3-1]$$

$$Q_L = \frac{f_{center}}{B} = \frac{915\,MHz}{138\,MHz} = 6.63 \quad [3-2]$$

The unloaded Q of the resonant circuit is equal to the Q of the inductor due to its losses.

$$Q_U = Q_{INDUCTOR} \approx 36@915MHz \quad [3-3]$$

An approximation of the losses of the input matching network can be made with the formula:

$$Loss = -20 * \log\left[1 - \frac{Q_L}{Q_U}\right] = -20 * \log\left[1 - \frac{6.63}{36}\right] = 1{,}8dB \quad [3-4]$$

The noise figure of the LNA-input-matching network is equal to its losses. The input matching network is always a compromise of sensitivity and selectivity. The loaded Q should not get too high because of 2 reasons:

more losses in the matching network and hence less sensitivity

tolerances of components affect matching too much. This will cause problems in a tuning-free mass production of the application. A good CAE-tool will help to see the effects of component tolerances on the input matching more accurate by tweaking each value.

A very high selectivity can be reached by using SAW-filters at the expense of higher cost and lower sensitivity which will be reduced by the losses of the SAW-Filter of approx. 4dB.

Image-suppression:

Due to the quite high 1st-IF of the frontend, the image frequency is quite far away. The image frequency of the receiver is at:

$$f_{IMAGE} = f_{SIGNAL} + 2 * f_{IF} = 915MHz + 2 * 305 = 1525MHz \quad [3-5]$$

The image suppression on the evalboard is about 17dB.

LO-leakage:

The LO of the 1st Mixer is at:

$$f_{LO} = f_{RECEIVE} * \frac{4}{3} = 915MHz * \frac{4}{3} = 1220MHz \quad [3-6]$$

The LO-leakage of the evalboard on the RF-input is about –90dBm.

3.1.3 Switch in TX-Mode

The evalboard can be set into the TX-Mode by grounding the RX/TX-jumper on the evalboard or programming the TDA5255 to operate in the TX-Mode. If the IC is programmed to operate in the TX-Mode, the RX/TX-pin will act as an open drain output at a logical LOW. Then a DC-current can flow from VCC to GND via L1, L2, D1, R1 and D2.

$$I_{PIN-DIODE} = \frac{Vcc - 2 * V_{FORWARD,PIN-DIODE}}{R_1} \quad [3-7]$$

Now both pin-diodes are biased with a current of approx. 0.3mA@3V and have a very low impedance for RF.

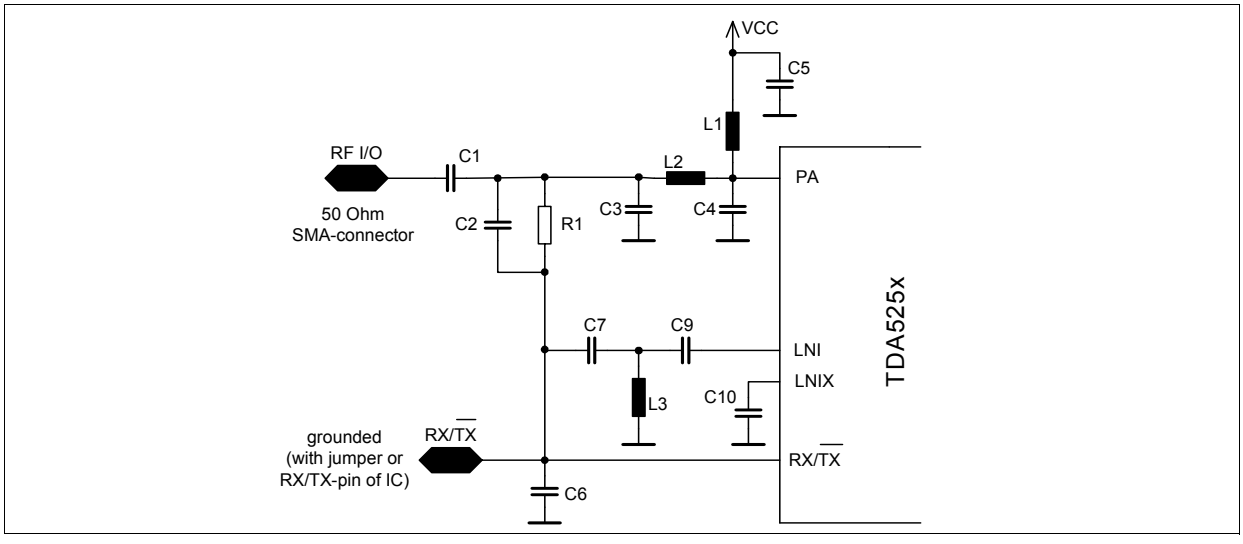


Figure 3-4 TX_Mode

R1 does not influence the matching because of its very high resistance. Due to the large capacitance of C1, C6 and C5 the circuit can be further simplified for RF:

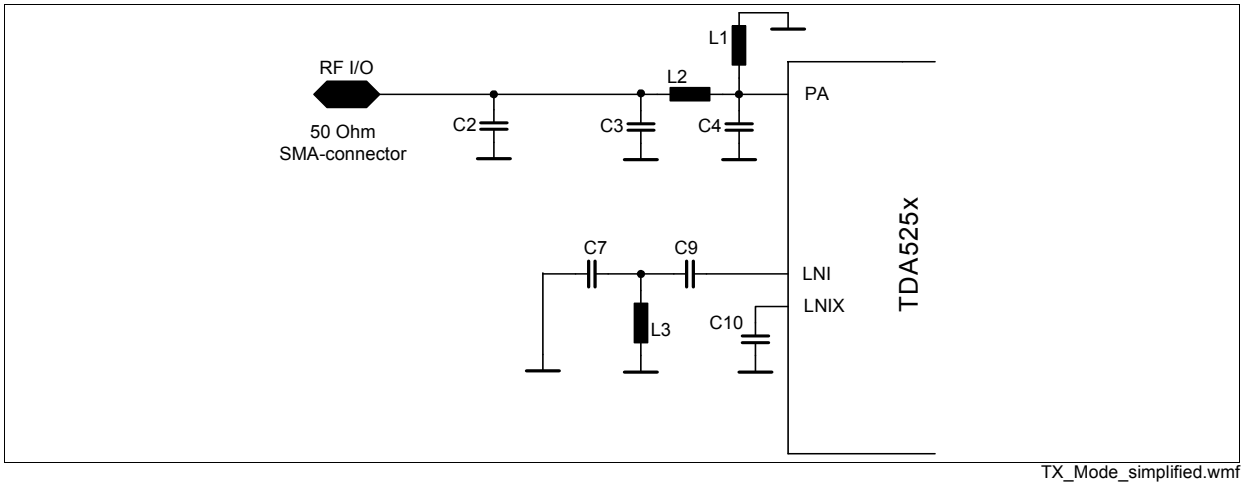


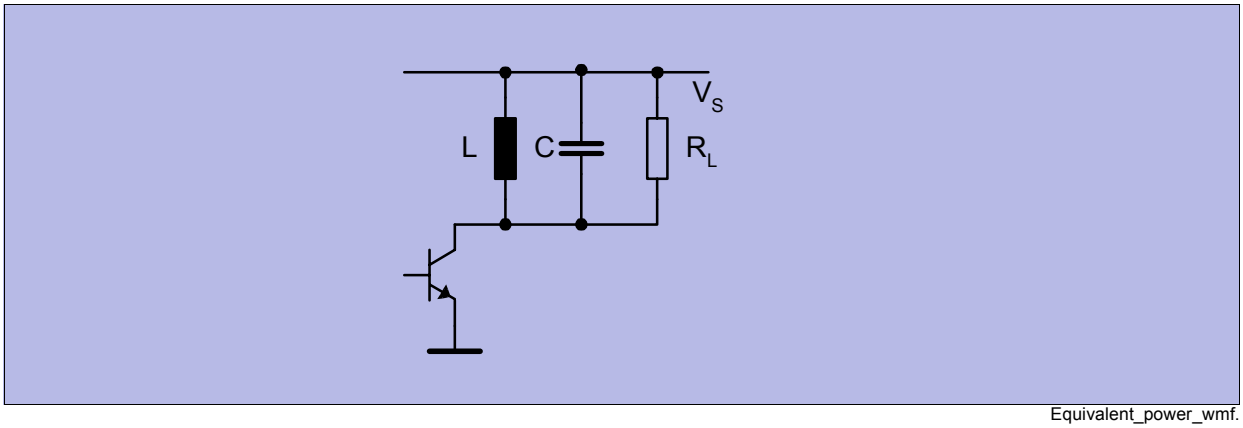
Figure 3-5 TX_Mode_simplified

The LNA-matching is RF-grounded now, so no power is lost in the LNA-input. The PA-matching consists of C2, C3 L2, C4 and L1.

When designing the matching of the PA, C2 must not be changed anymore because its value is already fixed by the LNA-input-matching.

3.1.4 Power-Amplifier

The power amplifier operates in a high efficient class C mode. This mode is characterized by a pulsed operation of the power amplifier transistor at a current flow angle of $\theta << \pi$. A frequency selective network at the amplifier output passes the fundamental frequency component of the pulse spectrum of the collector current to the load. The load and its resonance transformation to the collector of the power amplifier can be generalized by the equivalent circuit of **Figure 3-6**. The tank circuit L//C//RL in parallel to the output impedance of the transistor should be in resonance at the operating frequency of the transmitter.



Equivalent_power_wmf.

Figure 3-6 Equivalent power amplifier tank circuit

The optimum load at the collector of the power amplifier for “critical” operation under idealized conditions at resonance is:

$$R_{LC} = \frac{V_S^{\,2}}{2P_O} \qquad [3-8]$$

A typical value of R_{LC} for an RF output power of P_o= 13mW is:

$$R_{LC} = \frac{3^2}{2 * 0.013} = 350\Omega \qquad [3-9]$$

Critical” operation is characterized by the RF peak voltage swing at the collector of the PA transistor to just reach the supply voltage V_S. The high efficiency under “critical” operating conditions can be explained by the low power loss at the transistor.
During the conducting phase of the transistor there is no or only a very small collector voltage present, thus minimizing the power loss of the transistor ($i_C * u_{CE}$). This is particularly true for low current flow angles of $\theta << \pi$. In practice the RF-saturation voltage of the PA transistor and other parasitics will reduce the “critical” R_{LC}.

The output power P_o will be reduced when operating in an “overcritical” mode at a $R_L > R_{LC}$. As shown in Figure 3-7, however, power efficiency E (and bandwidth) will increase by some degree when operating at higher R_L. The collector efficiency E is defined as

$$E = \frac{P_O}{V_S I_C} \qquad [3-10]$$

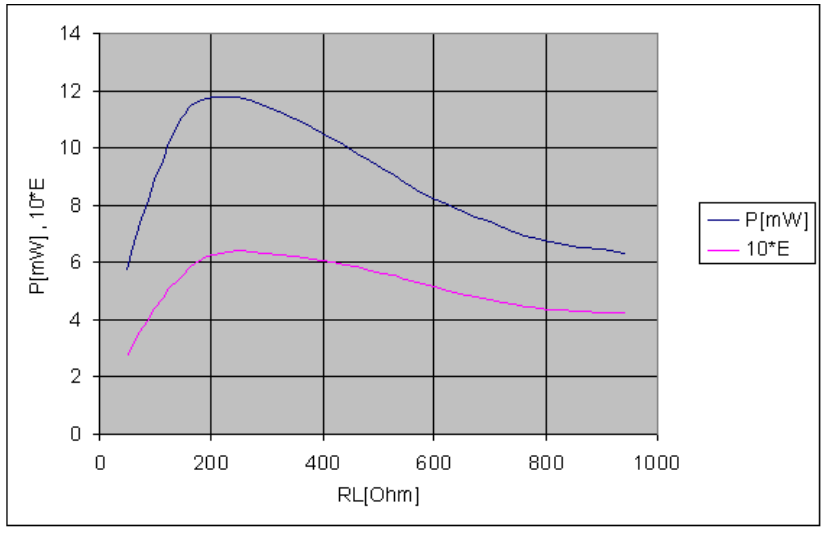
The diagram of Figure 3-7 has been measured directly at the PA-output at V_S=3V. A power loss in the matching circuit of about 3dB will decrease the output power. As shown in the diagram, 250 Ohm is the optimum impedance for operation at 3V. For an approximation of R_{OPT} and P_{OUT} at other supply voltages those 2 formulas can be used:

$$R_{OPT} \sim V_S \qquad [3-11]$$

and

$$P_{OUT} \sim R_{OPT} \qquad [3-12]$$

The behaviour of the power amplifier over the impedance and frequency is in principle the same as of the TDA5250, but of course strongly depends on the matching network. (see also specification of TDA5250)

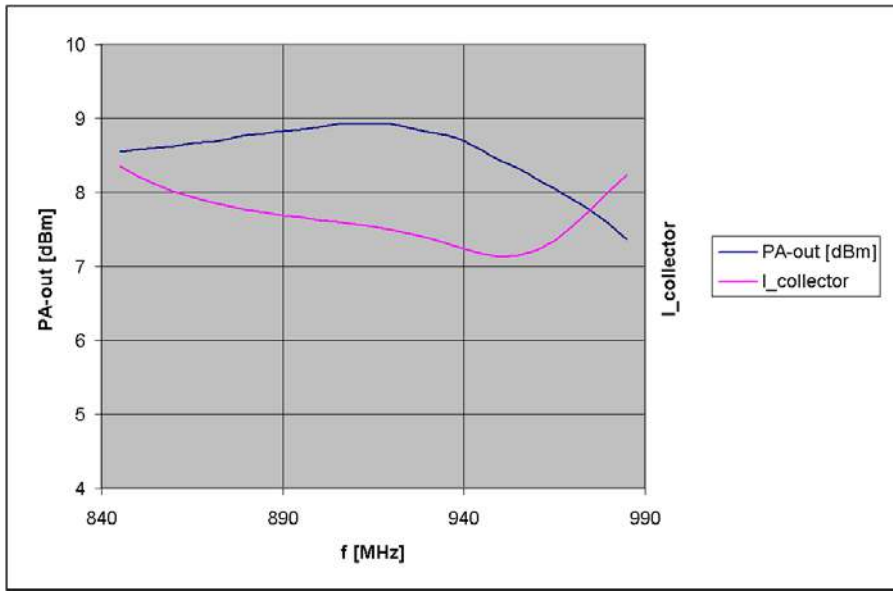


Power_E_vs_RL.wmf

Figure 3-7 Output power P_O (mW) and collector efficiency E vs. load resistor R_L.

The DC collector current I_C of the power amplifier and the RF output power P_O vary with the load resistor R_L. This is typical for overcritical operation of class C amplifiers. The collector current will show a characteristic dip at the resonance frequency for this type of “overcritical” operation. The depth of this dip will increase with higher values of R_L.

As **Figure 3-8** shows, detuning beyond the bandwidth of the matching circuit results in a significant increase of collector current of the power amplifier and in some loss of power. This diagram shows the data of the circuit of the test board around the center frequency of 915MHz.



PA-out_&_I-collector_vs_frequency.wmf

Figure 3-8 PA-out & I-collector vs. frequency

C4, L2 and C3||C2 are the main matching components which are used to transform the 50 Ohm load at the SMA-RF-connector to a higher impedance at the PA-output (250Ohm@3V). L1 can be used for finetuning of the resonance frequency but should not be too low in order to keep its loss low.

The transformed impedance of 250Ohm+j0 at the PA-output-pin can be verified with a network analyzer using this measurement procedure:

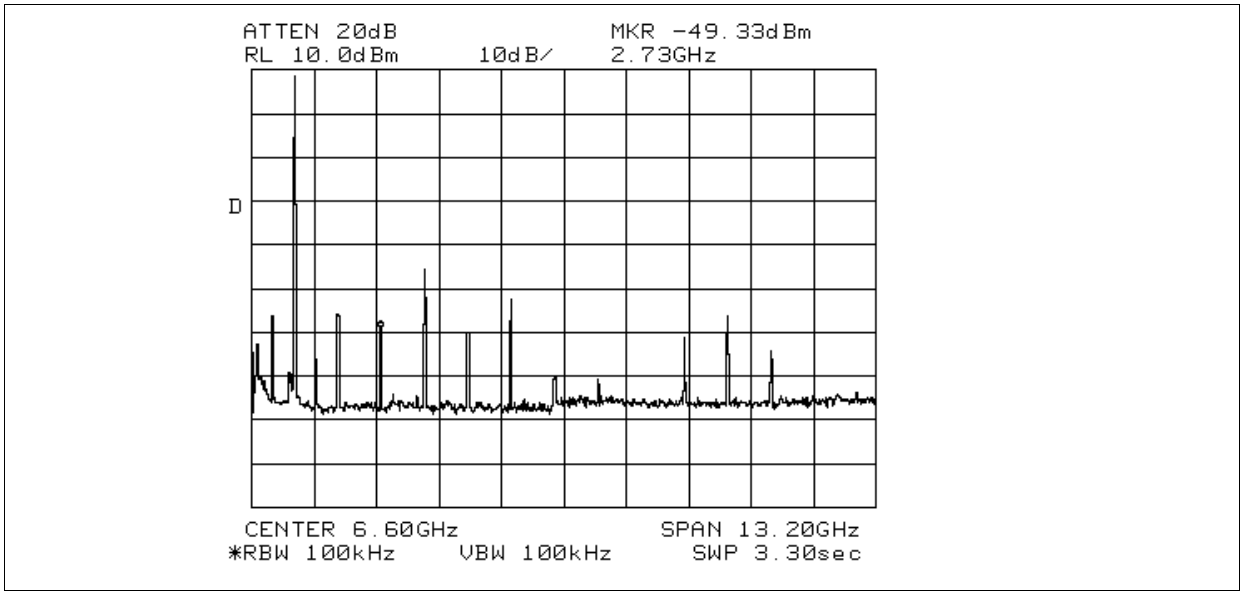
1. Calibrate your network analyzer.
2. Connect a short, low-loss 50 Ohm cable to your network analyzer with an open end on one side. Semirigid cable works best.
3. Use the „Port Extension“ feature of your network analyzer to shift the reference plane of your network analyzer to the open end of the cable.
4. Connect the center-conductor of the cable to the solder pad of the pin „PA“ of the IC. The shield has to be grounded. Very short connections must be used. Do not remove the IC or any part of the matching-components!
5. Screw a 50Ohm-dummy-load on the RF-I/O-SMA-connector
6. The TDA5255 has to be in ASK-TX-Mode, Data-Input=LOW.
7. Be sure that your network analyzer is AC-coupled and turn on the power supply of the IC.
8. Measure the S-parameter

The evalboard has been optimized for 3V. The load is about 250+j0 at 915MHz.

A tuning-free realization requires a careful design of the components within the matching network. A simple linear CAE-tool will help to see the influence of tolerances of matching components.

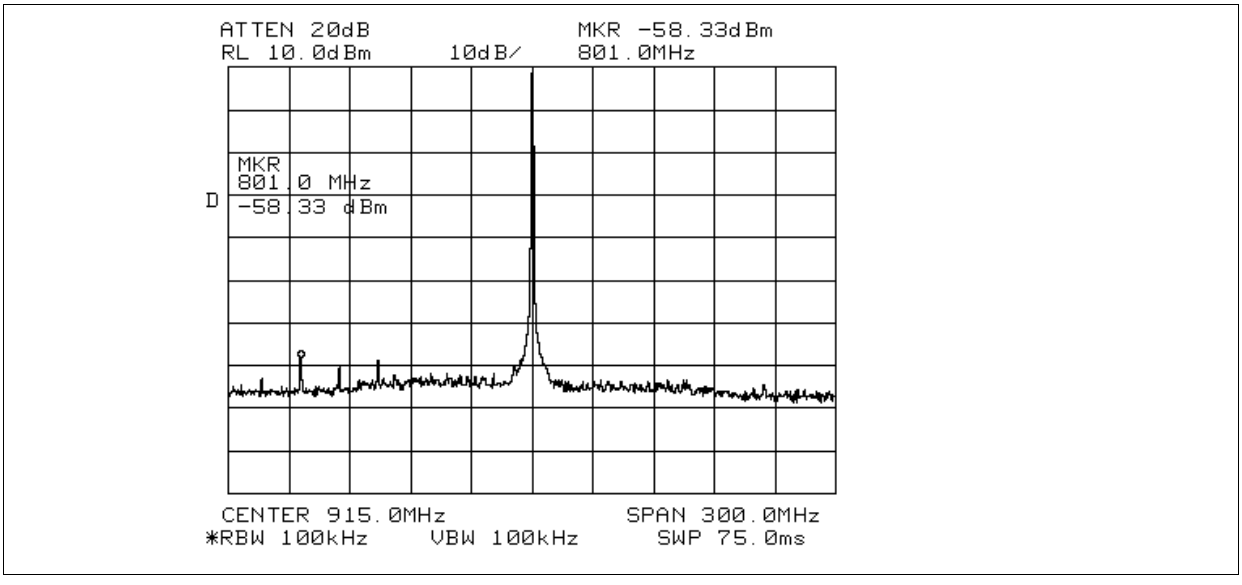
Suppression of spurious harmonics may require some additional filtering within the antenna matching circuit. Both can be seen in **Figure 3-9** and **Figure 3-10** The total spectrum of the evalboard can be summarized as:

Carrier fc	+9dBm
fc-18.1MHz	-69dBm
fc+18.1MHz	-72dBm
2nd harmonic	-45dBm
3rd harmonic	-49dBm



spectrum_13.2GHz.bmp

Figure 3-9 Transmit Spectrum 13.2GHz



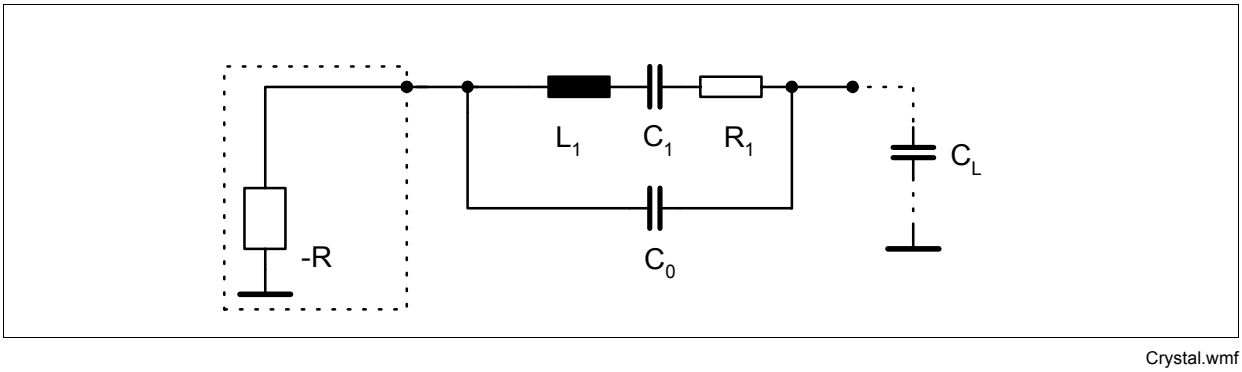
spektrum_300MHz.bmp

Figure 3-10 Transmit Spectrum 300MHz

3.2 Crystal Oscillator

The equivalent schematic of the crystal with its parameters specified by the crystal manufacturer can be taken from the subsequent figure.

Here also the load capacitance of the crystal C_L, which the crystal wants to see in order to oscillate at the desired frequency, can be seen.



Crystal.wmf

Figure 3-11 Crystal

L_1: motional inductance of the crystal

C_1: motional capacitance of the crystal

C_0: shunt capacitance of the crystal

[3 – 14]

Therefore the **Resonant Frequency f_S** of the crystal is defined as:

$$f_S = \frac{1}{2\pi\sqrt{L_1 * C_1}} \qquad [3-13]$$

The **Series Load Resonant Frequency f_S'** of the crystal is defined as:

$$f_S' = \frac{1}{2\pi\sqrt{L_1 * C_1}} * \sqrt{1 + \frac{C_1}{C_0 + C_L}}$$

regarding **Figure 3-11**

f_S' is the nominal frequency of the crystal with a specified load when tested by the crystal manufacturer.

Pulling Sensitivity of the crystal is defined as the magnitude of the relative change in frequency relating to the variation of the load capacitor.

$$\frac{\delta D}{\delta C_L} = \frac{\delta f_S' / f_S}{\delta C_L} = \frac{-C_1}{2(C_0 + C_L)^2} \qquad [3-15]$$

Choosing C_L as large as possible results in a small pulling sensitivity. On the other hand a small C_L keeps the influence of the serial inductance and the tolerances associated to it small (see **formula [3-17]**).

Start-up Time

$$t_{Start} \sim \frac{L_1}{|-R| - R_{ext}} \qquad [3-16]$$

where: -R: is the negative impedance of the oscillator see **Figure 3-11**

R_{ext}: is the sum of all external resistances (e.g. R_1 or any other resistance that may be present in the circuit, see **Figure 3-10**

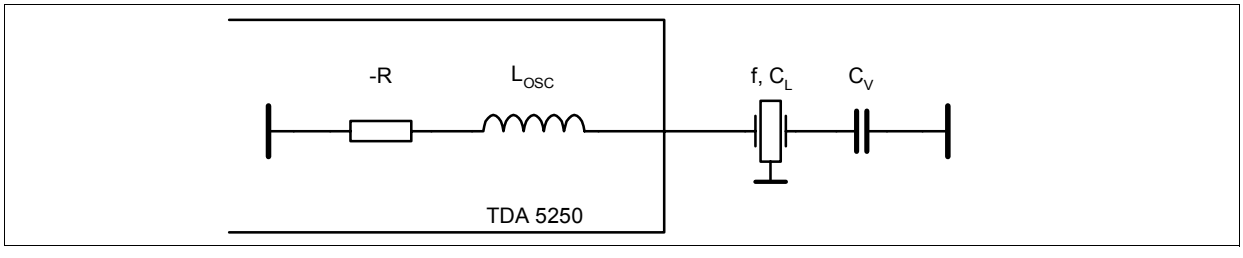
The proportionality of L_1 and C_1 of the crystal is defined by **formula [3-13]**. For a crystal with a small C_1 the start -up time will also be slower. Typically the lower the value of the crystal frequency, the lower the C_1.

A short **conclusion** regarding crystal and crystal oscillator dependencies is shown in the following table:

Table 3-1 Crystal and crystal oscilator dependency

Independent variable	Result		
	Relative Tolerance	Maximum Deviation	$t_{Start-up}$
C_1 >	>>	>>	<
C_0 >	<	<	-
frequency of quartz >	>>>	>	<<
L_{OSC} >	>>	>	-
C_L >	>	<	-

The crystal oscillator in the TDA5252 is a NIC (negative impedance converter) oscillator type. The input impedance of this oscillator is a negative impedance in series to an inductance. Therefore the load capacitance of the crystal C_L (specified by the crystal supplier) is transformed to the capacitance C_v as shown in **formula [3-17].**



QOSZ_NIC.wmf

Figure 3-12 Crystal Oscillator

$$C_L = \frac{1}{\frac{1}{C_V} - \omega^2 L_{OSC}} \leftrightarrow C_V = \frac{1}{\frac{1}{C_L} + \omega^2 L_{OSC}} \qquad [3-17]$$

C_L: crystal load capacitance for nominal frequency
ω: angular frequency
L_{OSC}: inductivity of the crystal oscillator - typ: 2.75µH with pad of board
2.5µH without pad

With the aid of this formula it becomes obvious that the higher the serial capacitance C_V is, the higher is the influence of L_{OSC}.

The tolerance of the internal oscillator inductivity is much higher, so the inductivity is the dominating value for the tolerance.

FSK modulation and tuning are achieved by a variation of C_V.

In case of small frequency deviations (up to +/- 1000 ppm), the desired load capacitances for FSK modulation are frequency depending and can be calculated with the formula below.

$$C_{L\pm} = \frac{C_L \mp C_0 \cdot \frac{\Delta f}{N \cdot f} \cdot \left(1 + \frac{2 \cdot (C_0 + C_L)}{C_1}\right)}{1 \pm \frac{\Delta f}{N \cdot f} \cdot \left(1 + \frac{2 \cdot (C_0 + C_L)}{C_1}\right)} \qquad [3 - 18]$$

C_L: crystal load capacitance for nominal frequency
C_0: shunt capacitance of the crystal
C_1: motional capacitance of the crystal
f: crystal oscillator frequency
N: division ratio of the PLL
Δf: peak frequency deviation

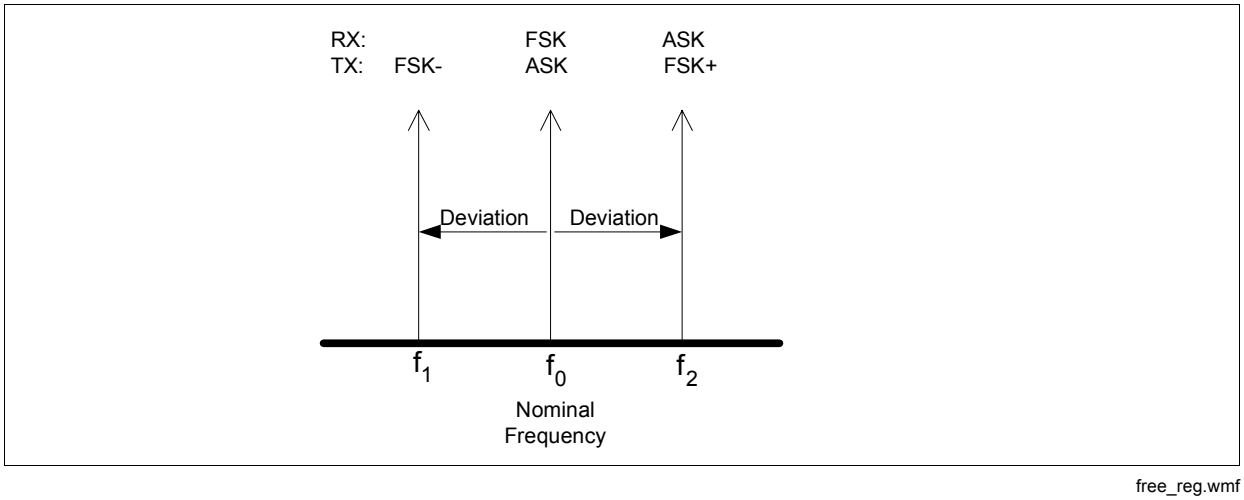
With C_{L+} and C_{L-} the necessary C_{v+} for FSK HIGH and C_{v-} for FSK LOW can be calculated.
Alternatively, an external AC coupled (10nF in series to 1kΩ) signal can be applied at **pin 19 (Xout)**. The drive level should be approximately 100mVpp.

3.2.1 Synthesizer Frequency setting

Generating ASK and FSK modulation 3 setable frequencies are necessary.

3.2.1.1 Possible crystal oscillator frequencies

The resulting possible crystal oscillator frequencies are shown in the following **Figure 3-13**



free_reg.wmf

Figure 3-13 possible crystal oscillator frequencies

In ASK receive mode the crystal oscillator is set to frequency f_2 to realize the necessary frequency offset to receive the ASK signal at f_0*N (N: division ratio of the PLL).

To set the 3 different frequencies 3 different C_v are necessary. Via internal switches 3 external capacitors can be combined to generate the necessary C_v in case of ASK- or FSK-modulation. Internal banks of switchable capacitors allow the finetuning of these frequencies.

3.2.2 Transmit/Receive ASK/FSK Frequency Assignment

Depending on whether the device operates in transmit or receive mode or whether it operates in ASK or FSK the following cases can be distinguished:

3.2.2.1 FSK-mode

In **transmit** mode the two frequencies representing logical HIGH and LOW data states have to be adjusted depending on the intended frequency deviation and separately according to the following formulas:

$f_{COSC\ HI} = (f_{RF} + f_{DEV}) / 48 \qquad f_{COSC\ LOW} = (f_{RF} - f_{DEV}) / 48$ [3 – 19]

e.g.

$f_{COSC\ HI}$ = (915E6 + 50E3) / 48 = 19,0635167MHz

$f_{COSC\ LOW}$ = (915E6 - 50E3) / 48 = 19,0614583MHz

with a frequency deviation of 50kHz.

Figure 3-14 shows the configuration of the switches and the capacitors to achieve the 2 desired frequencies. Gray parts of the schematics indicate inactive parts. For FSK modulation the ASK-switch is always open.

For **FSK LOW** the FSK-switch is closed and C_{v2} and C_{tune2} are bypassed. The effective C_{v-} is given by:

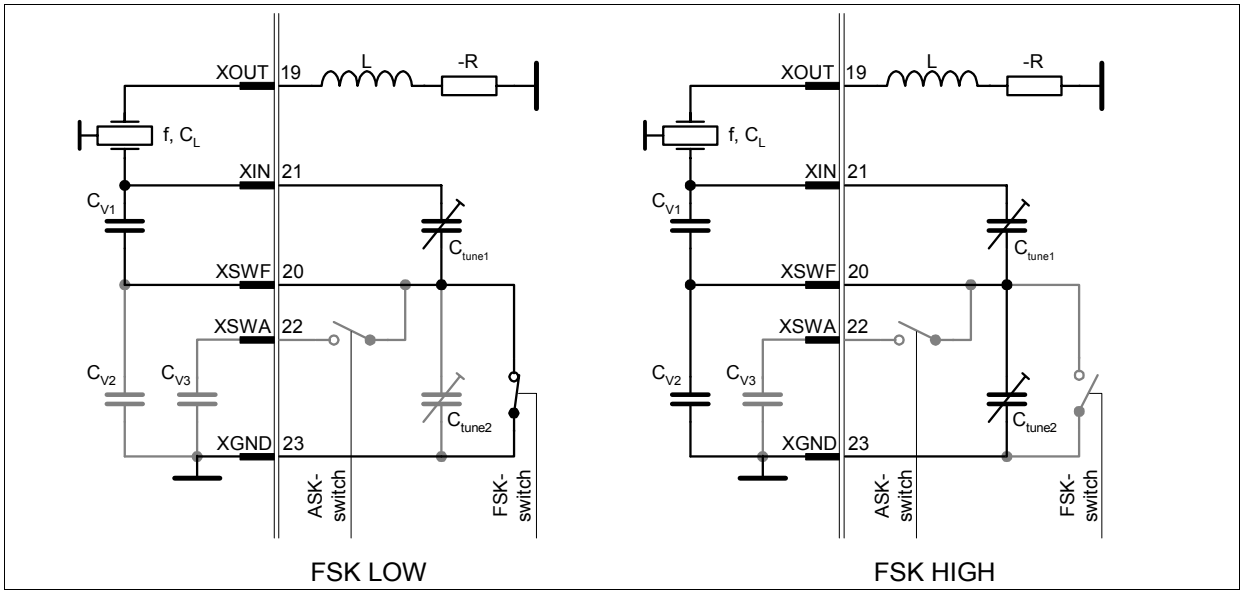
$$C_{V-} = C_{v1} + C_{tune1} \qquad [3 – 20]$$

For finetuning C_{tune1} can be varied over a range of 8 pF in steps of 125fF. The switches of this C-bank are controlled by the bits **D0** to **D5** in the **FSK** register (subaddress 01H, see **Table 3-6**).

For **FSK HIGH** the FSK-switch is open. So the effective C_{v+} is given by:

$$C_{v+} = \frac{(C_{v1} + C_{tune1}) \cdot (C_{v2} + C_{tune2})}{C_{v1} + C_{tune1} + C_{v2} + C_{tune2}} \qquad [3 – 21]$$

The C-bank C_{tune2} can be varied over a range of 16 pF in steps of 250fF for finetuning of the FSK HIGH frequency. The switches of this C-bank are controlled by the bits **D8** to **D13** in the **FSK** register (subaddress 01H, **see Table 3-6**).



QOSC_FSK.wmf

Figure 3-14 FSK modulation

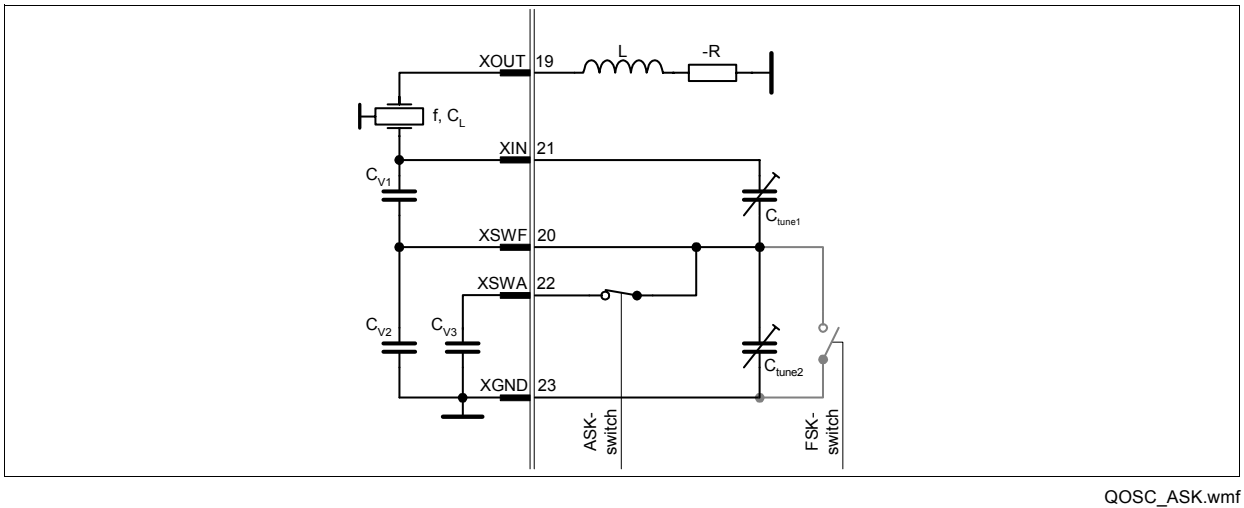
In **receive** mode the crystal oscillator frequency is set to yield a direct-to-zero conversion of the receive data. Thus the frequency may be calculated as

$$f_{COSC} = f_{RF} / 48, \qquad [3 - 22]$$

e.g.

$$f_{COSC} = 915E6 / 48 = 19.0625MHz$$

which is identical to the ASK transmit case.



QOSC_ASK.wmf

Figure 3-15 FSK receive

In this case the ASK-switch is closed. The necessary C_{vm} is given by:

$$C_{vm} = \frac{(C_{v1} + C_{tune1}) \cdot (C_{v2} + C_{v3} + C_{tune2})}{C_{v1} + C_{tune1} + C_{v2} + C_{v3} + C_{tune2}} \qquad [3 - 23]$$

The C-bank C_{tune2} can be varied over a range of 16 pF in steps of 250fF for finetuning of the FSK receive frequency. In this case the switches of the C-bank are controlled by the bits **D0** to **D5** of the **XTAL_TUNING** register (subaddress 02H, **see Table 3-5**).

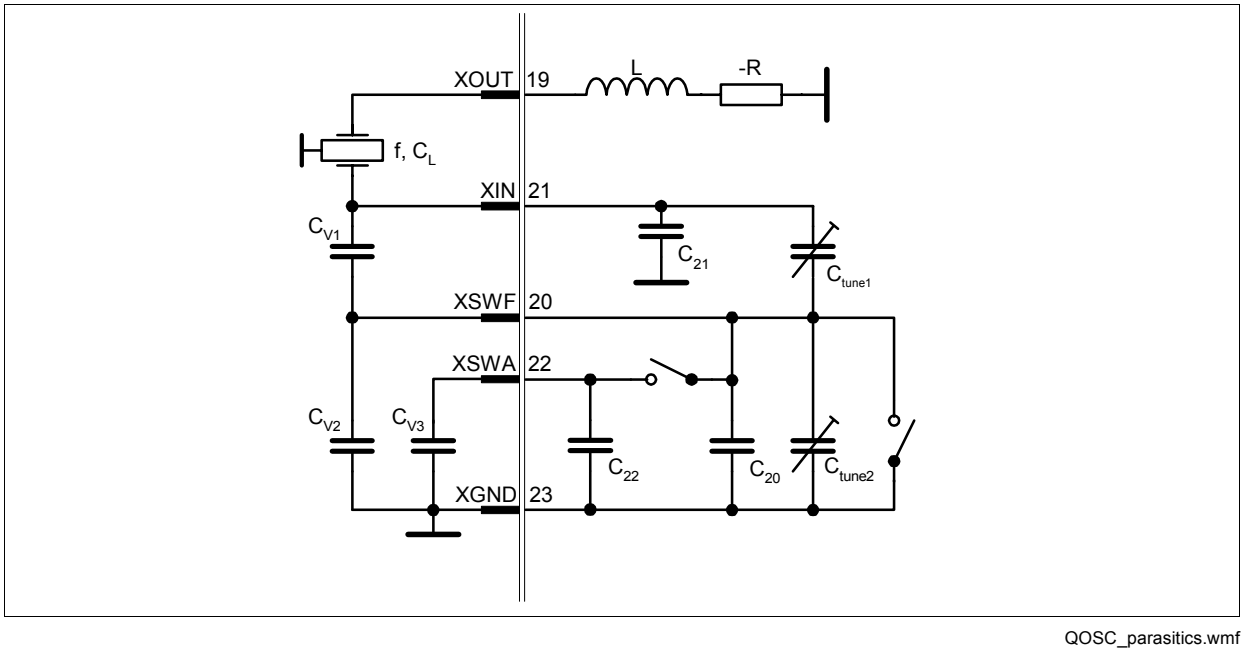
3.2.2.2 ASK-mode:

In **transmit** mode the crystal oscillator frequency is the same as in the FSK receive case, **see Figure 3-15**.

In **receive** mode a receive frequency offset is necessary as the limiters feedback is AC-coupled. This offset is achieved by setting the oscillator frequency to the FSK HIGH transmit frequency, **see Figure 3-14**.

3.2.3 Parasitics

For the correct calculation of the external capacitors the parasitic capacitances of the pins and the switches (C_{20}, C_{21}, C_{22}) have to be taken into account.



QOSC_parasitics.wmf

Figure 3-16 parasitics of the switching network

Table 3-2 Typical values of parasitic capacitances	
Name	**Value**
C_{20}	4,6 pF
C_{21}	FSK-: 2,8 pF / FSK+&ASK: 2.2pF
C_{22}	1 pF

With the given parasitics the actual C_v can be calculated:

$$C_{v-} = C_{v1} + C_{tune1} + C_{21} \quad [3-24]$$

$$C_{v+} = \frac{(C_{v1} + C_{tune1}) \cdot (C_{v2} + C_{20} + C_{tune2})}{C_{v1} + C_{tune1} + C_{v2} + C_{20} + C_{tune2}} + C_{21} \quad [3-25]$$

$$C_{vm} = \frac{(C_{v1} + C_{tune1}) \cdot (C_{v2} + C_{20} + C_{v3} + C_{22} + C_{tune2})}{C_{v1} + C_{tune1} + C_{v2} + C_{20} + C_{v3} + C_{22} + C_{tune2}} + C_{21} \quad [3-26]$$

Note: Please keep in mind also to include the Pad parasitics of the circuit board.

3.2.4 Calculation of the external capacitors

1. Determination of necessary crystal frequency using **formula [3-19].**
   e.g. $f_{FSK-} = f_{COSC\ LOW}$
2. Determine corresponding C_{Load} applying **formula [3-18]**.
   e.g. $C_{L\ FSK-} = C_{L\ \pm}$
3. Necessary C_V using **formula [3-17]**.
   e.g.

$$C_{V-} = \frac{1}{\frac{1}{C_{L,FSK-}} + (2\pi f_{FSK-})^2 * L_{OSC}}$$

1. When the necessary C_v for the 3 frequencies (C_{v-} for FSK LOW, C_{v+} for FSK HIGH and C_{vm} for FSK-receive) are known the external capacitors and the internal tuning caps can be calculated using the following formulas:

[3 – 29]

-FSK: $$C_{v1} + C_{tune1} = C_{v-} - C_{21}$$ [3 – 27]

+FSK: $$C_{v2} + C_{tune2} = \frac{(C_{v1} + C_{tune1}) \cdot (C_{v+} - C_{21})}{(C_{v1} + C_{tune1}) - (C_{v+} - C_{21})} - C_{20}$$ [3 – 28]

FSK_RX: $$C_{v3} + C_{tune2} = \frac{(C_{v1} + C_{tune1}) \cdot (C_{vm} - C_{21})}{(C_{v1} + C_{tune1}) - (C_{vm} - C_{21})} - C_{20} - C_{v2} - C_{22}$$

To compensate frequency errors due to crystal and component tolerance C_{v1}, C_{v2} and C_{v3} have to be varied. To enable this correction, half of the necessary capacitance variation has to be realized with the internal C-banks.

If no finetuning is intended it is recommended to leave XIN (Pin 21) open. So the parasitic capacitance of Pin 21 has no effect.

Note: Please keep in mind also to include the Pad parasitics of the circuit board.

In the suitable range for the serial capacitor, either capacitors with a tolerance of 0.1pF or 1% are available.

A spreadsheet, which can be used to predict the total frequency error by simply entering the crystal specification, may be obtained from Infineon.

3.2.5 FSK-switch modes

The FSK-switch can be used either in a bipolar or in a FET mode. The mode of this switch is controlled by bit **D0** of the **XTAL_CONFIG** register (subaddress 0EH).

In the bipolar mode the FSK-switch can be controlled by a ramp function. This ramp function is set by the bits D1 and D2 of the XTAL_CONFIG register (subadress 0EH). With these modes of the FSK-switch the bandwidth of the FSK spectrum can be influenced.

When working in the FET mode the power consumption can be reduced by about 200 µA.

The default mode is bipolar switch with no ramp function (D0 = 1, D1 = D2 = 0), which is suitable for all bitrates.

Table 3-3 Sub Address 0EH: XTAL_CONFIG

D0	D1	D2	Switch mode	Ramp time	Max. Bitrate
0	n.a.	n.a.	FET	< 0.2 µs	> 32 kBit/s NRZ
1	**0**	**0**	**bipolar (default)**	**< 0.2 µs**	**> 32 kBit/s NRZ**
1	1	0	bipolar	4 µs	32 kBit/s NRZ
1	0	1	bipolar	8 µs	16 kBit/s NRZ
1	1	1	bipolar	12 µs	12 kBit/s NRZ

3.2.6 Finetuning and FSK modulation relevant registers

Case FSK-RX or ASK-TX (C_{tune2}):

Table 3-4 Sub Address 02H: XTAL_TUNING				
Bit	**Function**	**Value**	**Description**	**Default**
D5	Nominal_Frequ_5	8pF	Setting for nominal frequency ASK-TX FSK-RX (C_{tune2})	0
D4	Nominal_Frequ_4	4pF		1
D3	Nominal_Frequ_3	2pF		0
D2	Nominal_Frequ_2	1pF		0
D1	Nominal_Frequ_1	500fF		1
D0	Nominal_Frequ_0	250fF		0

Case FSK-TX or ASK-RX (C_{tune1} and C_{tune2}):

Table 3-5 Sub Address 01H: FSK				
Bit	**Function**	**Value**	**Description**	**Default**
D13	FSK+5	8pF	Setting for positive frequency shift: +FSK or ASK-RX (C_{tune2})	0
D12	FSK+4	4pF		0
D11	FSK+3	2pF		1
D10	FSK+2	1pF		0
D9	FSK+1	500fF		1
D8	FSK+0	250fF		0
D5	FSK-5	4pF	Setting for negative frequency shift: -FSK (C_{tune1})	0
D4	FSK-4	2pF		0
D3	FSK-3	1pF		1
D2	FSK-2	500fF		1
D1	FSK-1	250fF		0
D0	FSK-0	125fF		0

Default values

In case of using the evaluation board, the crystal with its typical parameters (fp=19,0625MHz, C_1=8fF, C_0=2,1pF, C_L=20pF) and external capacitors with Cv1=8.2pF, Cv2=6.8pF, Cv3=22pF each are used the following default states are set in the device.

Table 3-6 Default oscillator settings	
Operating state	**Frequency**
ASK-TX / FSK-RX	915 MHz
+FSK-TX / ASK-RX	+50 kHz
-FSK-TX	-50 kHz

3.2.7 Chip and System Tolerances

Quartz: fp=19.0625MHz; C1=8fF; C0=2.1pF; CL=20pF (typical values)
Cv1=8.2pF, Cv2=6.8pF, Cv3=22pF

Table 3-7 Internal Tuning

Part	Frequency tolerance @ 915MHz	Rel. tolerance
Frequency set accuracy	+/- 1.5kHz	+/- 1.6ppm
Temperature (-40...+85C)	+/- 5kHz	+/- 6ppm
Supply Voltage(2.1...5.5V)	+/- 1.5kHz	+/- 1.5ppm
Total	+/- 8kHz	+/- 9ppm

Table 3-8 Default Setup (without internal tuning & without Pin21 usage)

Part	Frequency tolerance @ 915MHz	Rel. tolerance
Internal capacitors (+/- 10%)	+/- 4kHz	+/- 4.5ppm
Inductivity of the crystal oscillator	+/- 29kHz	+/- 33ppm
Temperature (-40...+85C)	+/- 5kHz	+/- 6ppm
Supply Voltage (2.1...5.5V)	+/- 1kHz	+/- 1.5ppm
Total	+/- 39kHz	+/- 45ppm

Tolerance values in **Table 3-8** are valid, if pin 21 is not connected. Establishing the connection to pin 21 the tolerances increase.

Concerning the frequency tolerances of the whole system also crystal tolerances (tuning tolerances, temperature stability, tolerance of C_L) have to be considered.

In addition to the chip tolerances also the crystal and external component tolerances have to be considered in the tuning and non-tuning case.

In case of internal tuning: The crystal on the evaluation board has a temperature stability of +/- 20ppm (or +/- 18kHz of the RF), which must be added to the total tolerances.

In case of default setup (without internal tuning and without usage of pin 21) the temperature stability and tuning tolerance of the crystal as well as the tolerance of the external capacitors (+/- 0.1pF) have to be added. The crystal on the evaluation board has a temperature stability of +/- 20ppm (means +/- 18kHz of the RF) and a tuning tolerance of +/- 10ppm (means +/- 9kHz of the RF). The external capacitors add a tolerance of +/- 3.5ppm (or +/- 3.2kHz regarding to the RF).

The frequency stabilities of both the receiver and the transmitter and the modulation bandwidth set the limit for the bandwidth of the IQ filter. To achieve a high receiver sensitivity and efficient

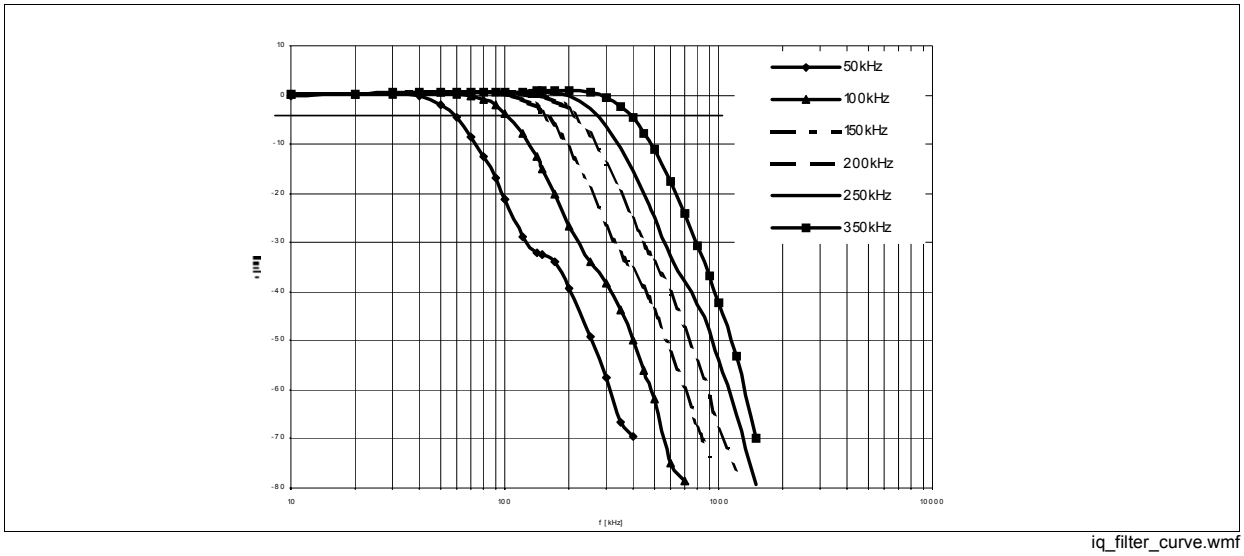
suppression of adjacent interference signals, the narrowest possible IQ bandwidth should be realized (**see Section 3.3**).

3.3 IQ-Filter

The IQ-Filter should be set to values corresponding to the RF-bandwidth of the received RF signal via the **D1** to **D3** bits of the **LPF** register (subaddress 03H).

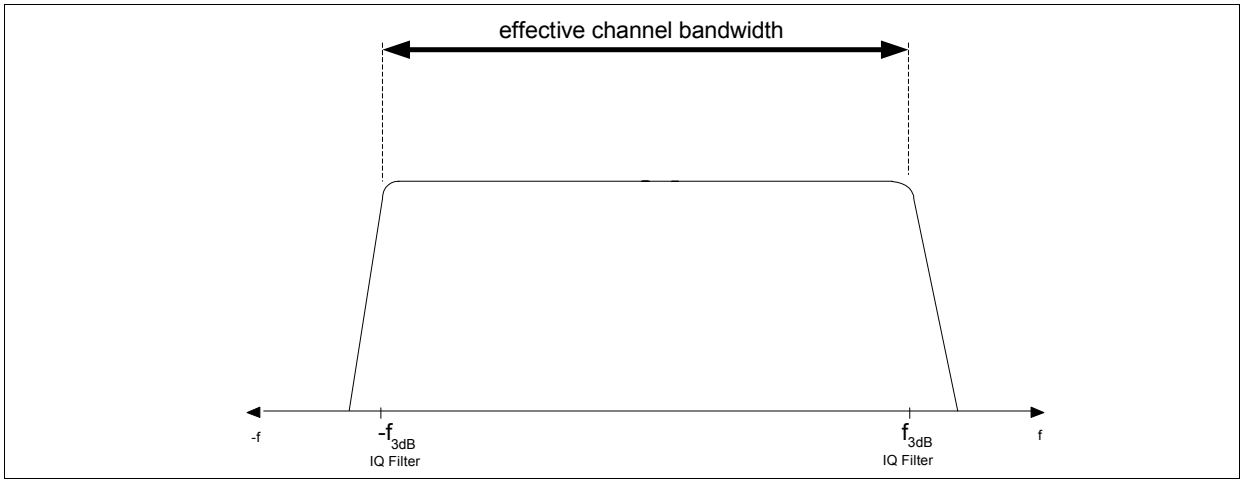
Table 3-9 3dB cutoff frequencies I/Q Filter

D3	D2	D1	nominal f_{-3dB} in kHz (programmable)	resulting effective channel bandwidth in kHz
0	0	0	not used	
0	0	1	350	700
0	1	0	250	500
0	1	1	200	400
1	0	0	150 (default)	300
1	0	1	100	200
1	1	0	50	100
1	1	1	not used	



iq_filter_curve.wmf

Figure 3-17 I/Q Filter Characteristics



iq_char.wmf

Figure 3-18 IQ Filter and frequency characteristics of the receive system

3.4 Data Filter

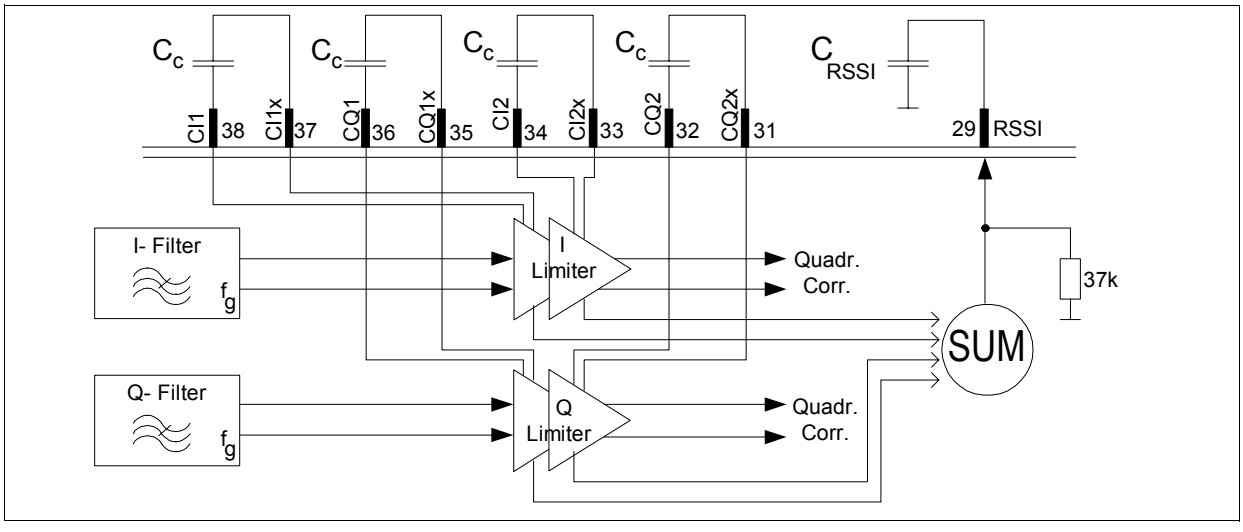
The Data-Filter should be set to values corresponding to the bandwidth of the transmitted Data signal via the D4 to D7 bits of the LPF register (subaddress 03H).

Table 3-10 3dB cutoff frequencies Data Filter

D7	D6	D5	D4	nominal f_{-3dB} in kHz
0	0	0	0	5
0	0	0	1	7 (default)
0	0	1	0	9
0	0	1	1	11
0	1	0	0	14
0	1	0	1	18
0	1	1	0	23
0	1	1	1	28
1	0	0	0	32
1	0	0	1	39
1	0	1	0	49
1	0	1	1	55
1	1	0	0	64
1	1	0	1	73
1	1	1	0	86
1	1	1	1	102

3.5 Limiter and RSSI

The I/Q Limiters are DC coupled multistage amplifiers with offset-compensating feedback circuit and an overall gain of approximately 80dB each in the frequency range of 100Hz up to 350kHz. Receive Signal Strength Indicator (RSSI) generators are included in both limiters which produce DC voltages that are directly proportional to the input signal level in the respective channels. The resulting I- and Q-channel RSSI-signals are summed to the nominal RSSI signal.



limiter input.wmf

Figure 3-19 Limiter and Pinning

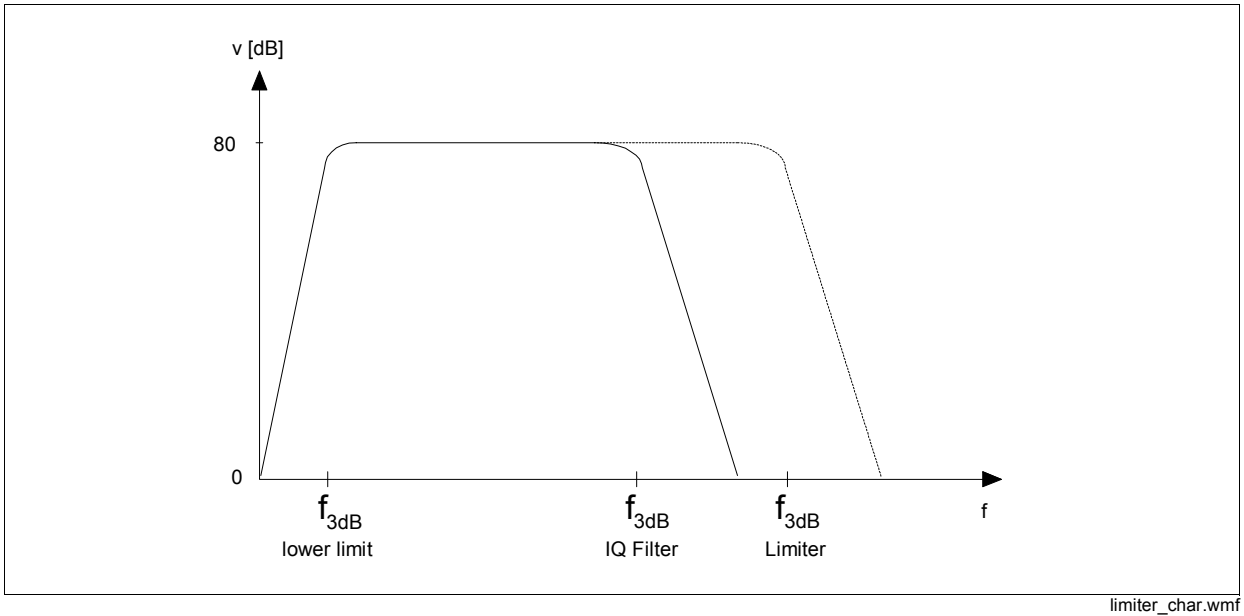
The DC offset compensation needs 2.2ms after Power On or Tx/Rx switch. This time is hard wired and independent from external capacitors C_C on pins 31 to 38. The maximum value for this capacitors is 47nF.

RSSI accuracy settling time = 2.2ms + 5*RC=2.2ms+5*37k*2.2nF=2.6ms

R - internal resistor; C - external capacitor at Pin 29

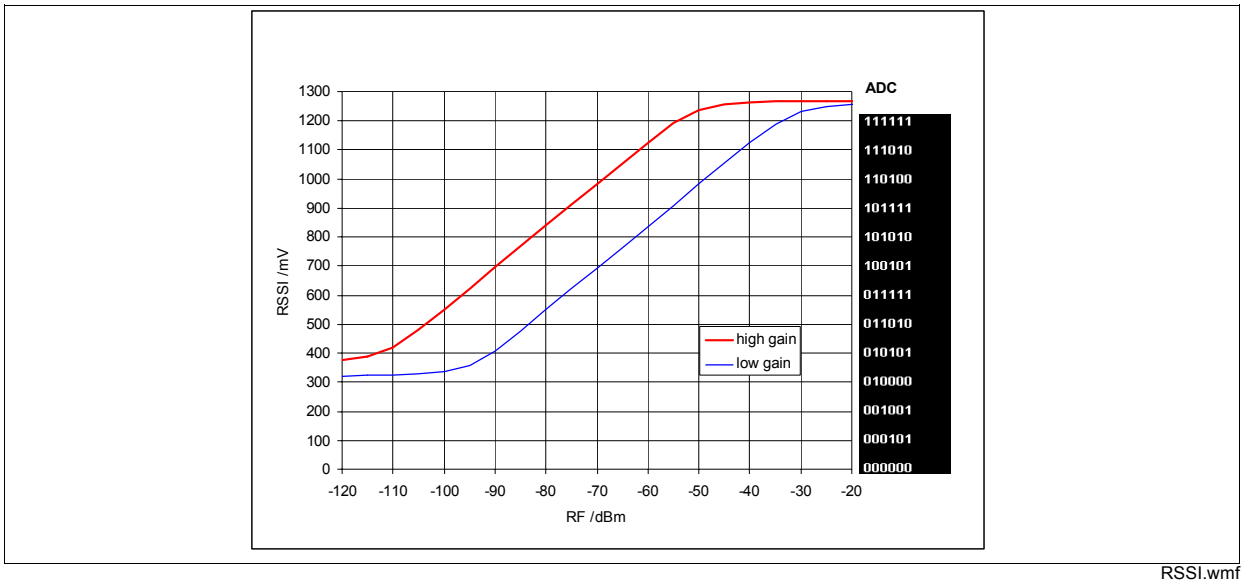
Table 3-11 Limiter Bandwidth

Cc [nF]	f3dB lower limit [Hz]	f3dB upper limit	Comment
220	100	IQ Filter	*setup time not guaranteed*
100	220	- II -	*setup time not guaranteed*
47	**470**	**- II -**	**Eval Board**
22	1000	- II -	
10	2200	- II -	



limiter_char.wmf

Figure 3-20 Limiter frequency characteristics



RSSI.wmf

Figure 3-21 Typ. RSSI Level (Eval Board) @3V

3.6 Data Slicer - Slicing Level

The data slicer is an analog-to-digital converter. It is necessary to generate a threshold value for the negative comparator input (data slicer). The TDA5255 offers an RC integrator and a peak detector which can be selected via logic. Independent of the choice, the peak detector outputs are always active.

3.6.1 RC Integrator

Table 3-12 Sub Address 00H: CONFIG

Bit	Function	Description	Default	SET
D15	SLICER	0= LP, 1= Peak Detector	0	0

Necessary external component (**Pin14**): C_{SLC}

This integrator generates the mean value of the data filter output. For a stable threshold value, the cut-off frequency has to be lower than the lowest signal frequency. The cutoff frequency results from the internal resistance R=100kΩ and the external capacitor C_{SLC} on **Pin14**.

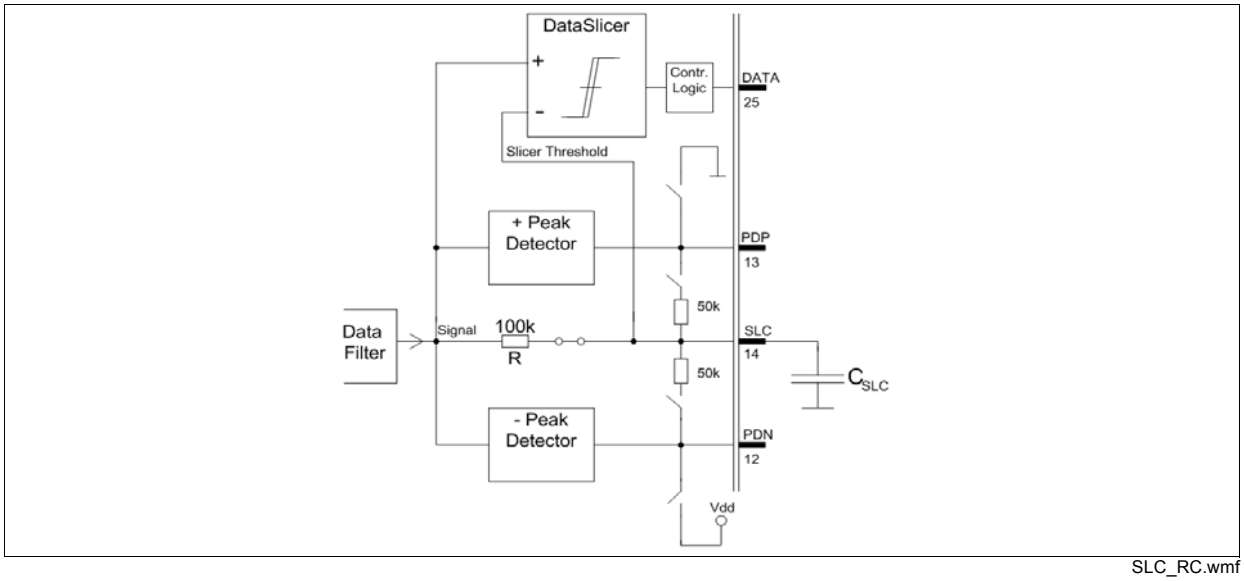
Cut-off frequency:

$$f_{cut-off} = \frac{1}{2\pi \cdot 100\,k\Omega \cdot C_{SLC}} < Min\{f_{Signal}\} \qquad [3-30]$$

Component calculation: (rule of thumb)

T_L – longest period of no signal change

$$C_{SLC} \geq \frac{3 \cdot T_L}{100\ k\Omega} \qquad [3-31]$$



SLC_RC.wmf

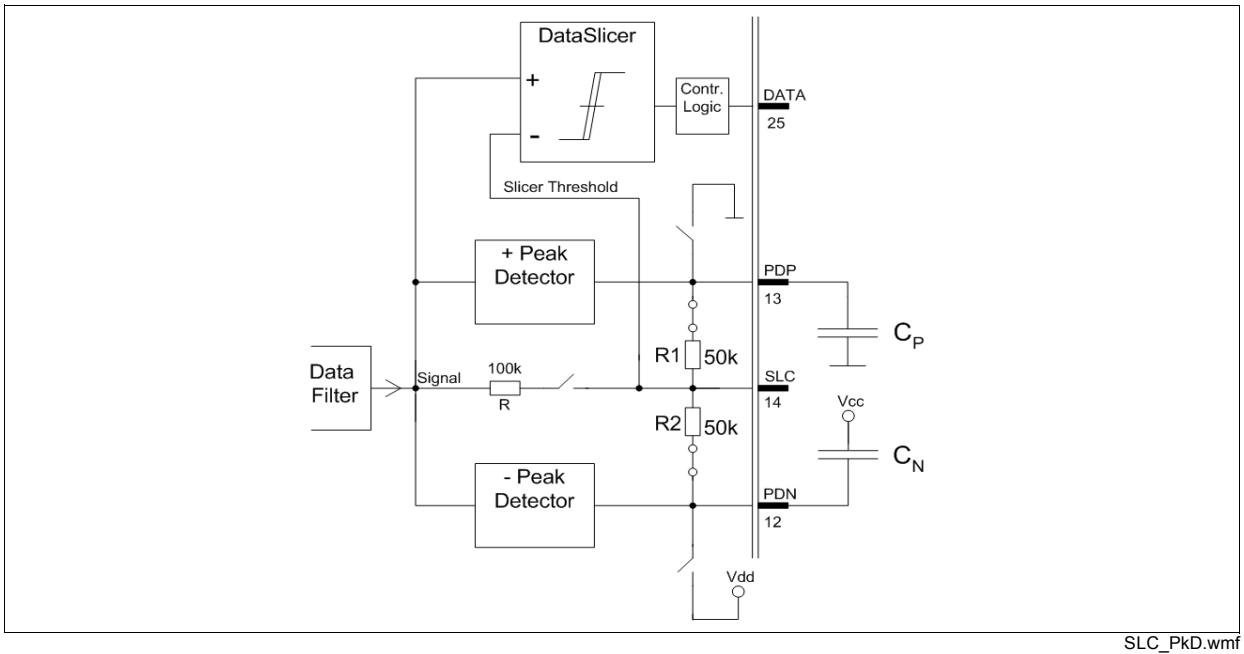
Figure 3-22 Slicer Level using RC Integrator

3.6.2 Peak Detectors

Table 3-13 Sub Address 00H: CONFIG				
Bit	**Function**	**Description**	**Default**	**SET**
D15	SLICER	0= LP, 1= Peak Detector	0	1

The TDA5252 has two peak detectors built in, one for positive peaks in the data stream and the other for the negative ones.

Necessary external components:
- **Pin12:** C_N
- **Pin13:** C_P



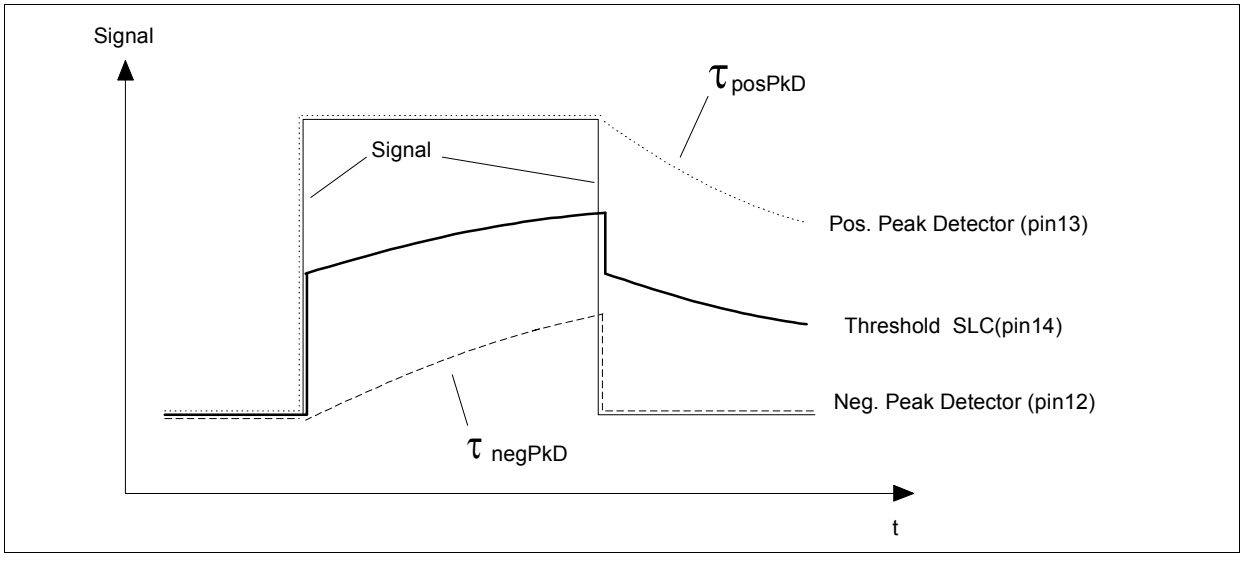
SLC_PkD.wmf

Figure 3-23 Slicer Level using Peak Detector

For applications requiring fast attack and slow release from the threshold value it is reasonable to use the peak detectors. The threshold value is generated by an internal voltage divider. The release time is defined by the internal resistance values and the external capacitors.

$$\tau_{posPkD} = 100\ k\Omega \cdot C_p \qquad [3-32]$$

$$\tau_{negPkD} = 100\ k\Omega \cdot C_n \qquad [3-33]$$



PkD_timing.wmf

Figure 3-24 Peak Detector timing

Component calculation: (rule of thumb)

$$C_p \geq \frac{2 \cdot T_{L1}}{100k\Omega} \qquad [3 - 34]$$

T_{L1} – longest period of no signal change (LOW signal)

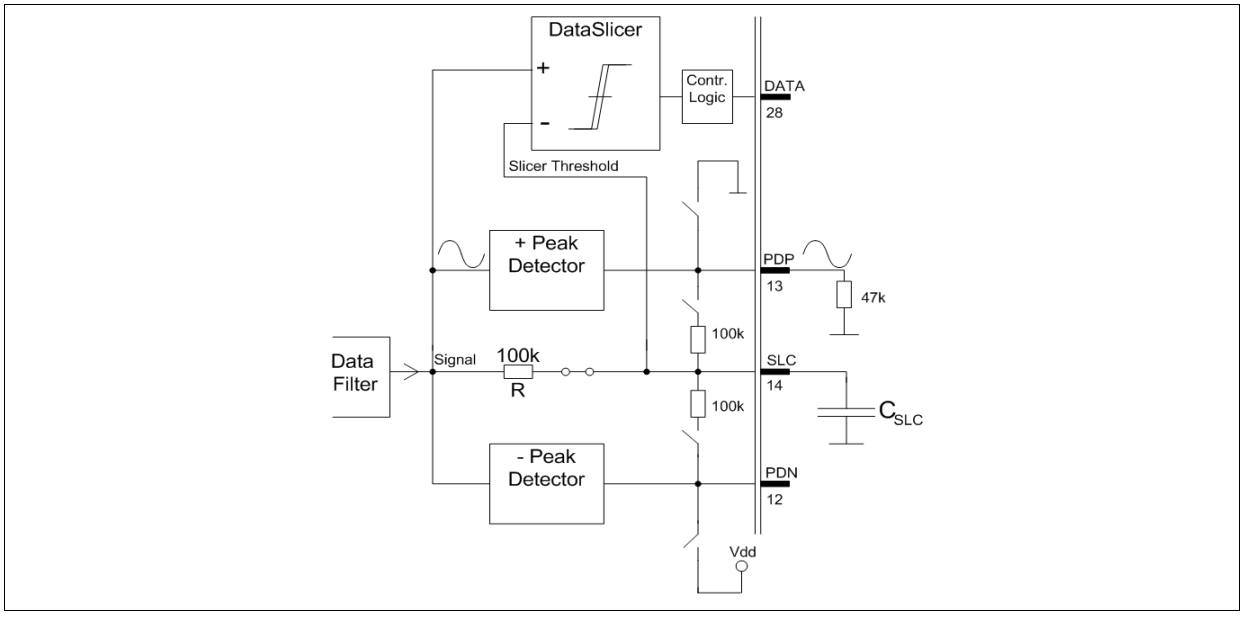
$$C_n \geq \frac{2 \cdot T_{L2}}{100k\Omega}$$

T_{L2} – longest period of no signal change (HIGH signal) [3 – 35]

3.6.3 Peak Detector - Analog output signal

The TDA5255 data output can be digital (pin 28) or in analog form by using the peak detector output and changing some settings.

To get an analog data output the slicer must be set to **lowpass mode (Reg. 0, D15 = LP = 0)** and the peak detector capacitor at pin 12 or 13 has to be changed to a resistor of about 47kOhm.



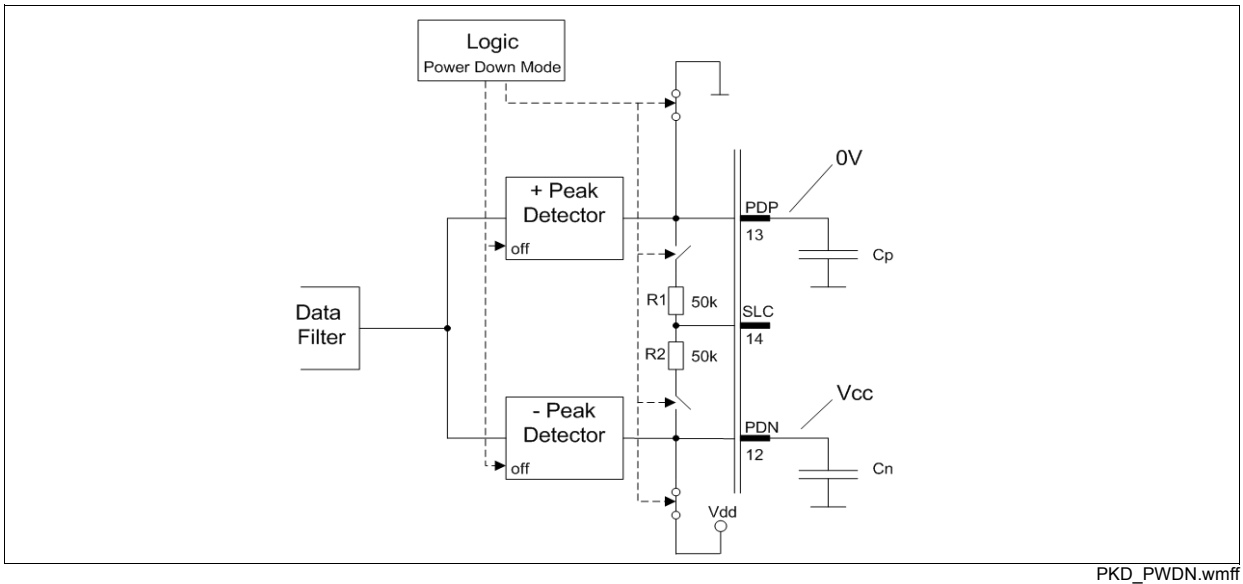
PkD_analog.wmf

Figure 3-25 Peak Detector as analog Buffer (v=1)

3.6.4 Peak Detector – Power Down Mode

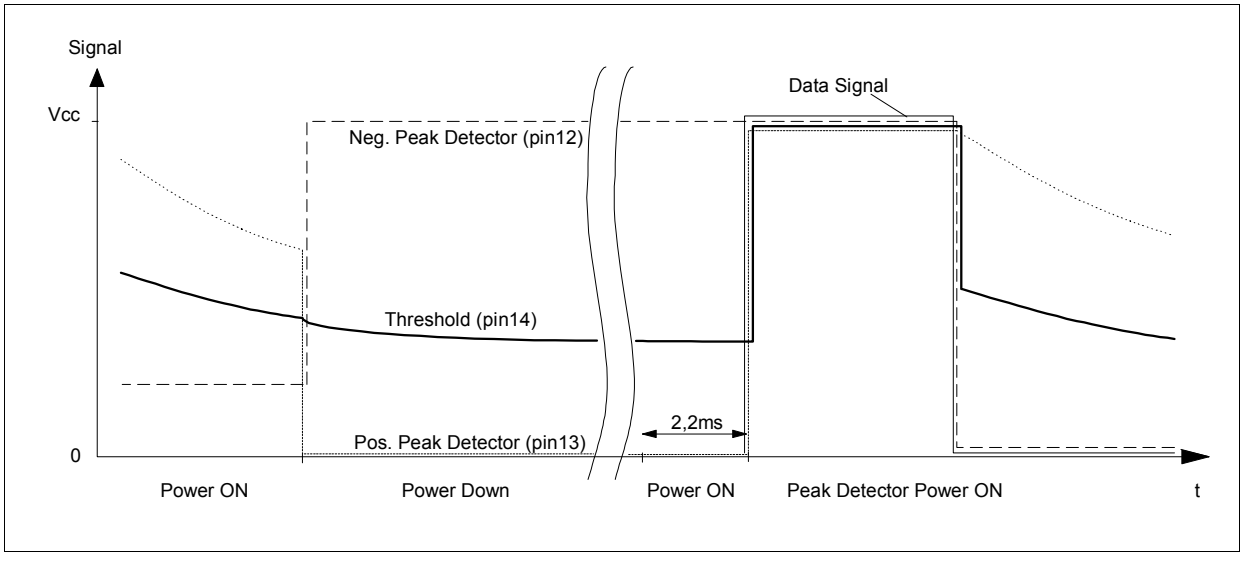
For a safe and fast threshold value generation the peak detector is turned on by the sequencer circuit (see **Section 2.4.18**) only after the entire receiving path is active.

In the off state the output of the positive peak detector is tied down to GND and the output of the negative peak detector is pulled up to VCC.



PKD_PWDN.wmf

Figure 3-26 Peak detector - power down mode



PkD_PWDN3.wmf

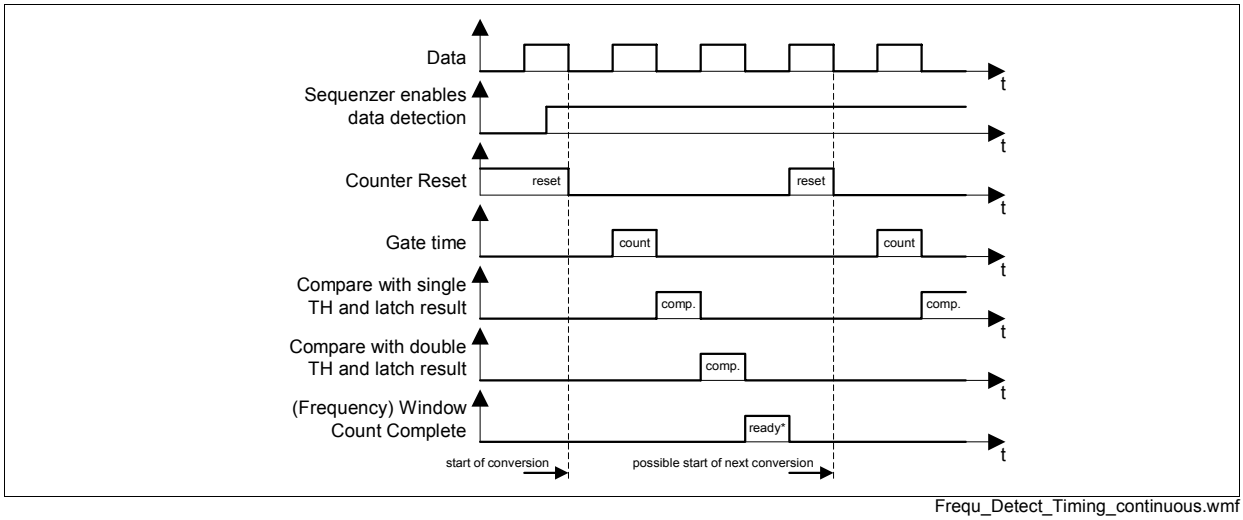
Figure 3-27 Power down mode

3.7 Data Valid Detection

In order to detect valid data two criteria must be fulfilled.

One criteria is the data rate, which can be set in register 06h and 07h. The other one is the received RF power level, which can be set in register 08h in form of the RSSI threshold voltage. Thus for using the data valid detection FSK modulation is recommended.

Timing for data detection looks like the following. Two settings are possible: „Continuous“ and „Single Shot“, which can be set by D5 and D6 in register 00H.



Frequ_Detect_Timing_continuous.wmf

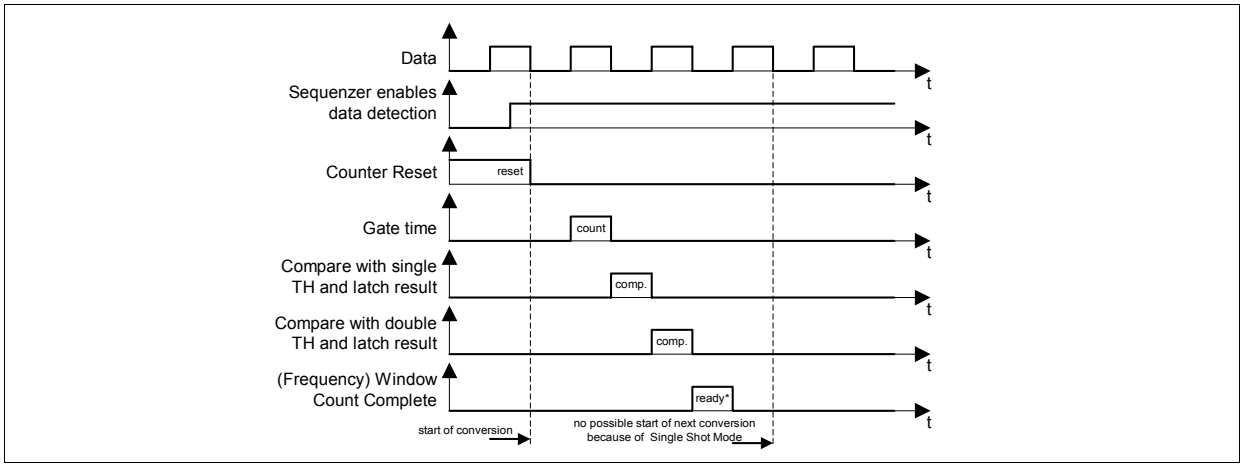
Figure 3-28 Frequency Detection timing in continuous mode

Note 1: Chip internal signal „Sequencer enables data detection“ has a LOW to HIGH transition about 2.6ms after RX is activated (see **Figure 2-15**).

Note 2: The positive edge of the „Window Count Complete“ signal latches the result of comparison of the analog to digital converted RSSI voltage with TH3 (register 08H). A logic combination of this output and the result of the comparison with single/double TH_X defines the internal signal „data_valid“.

Figure 3-27 shows that the logic is ready for the next conversion after 3 periods of the data signal.

Timing in Single Shot mode can be seen in the subsequent figure:



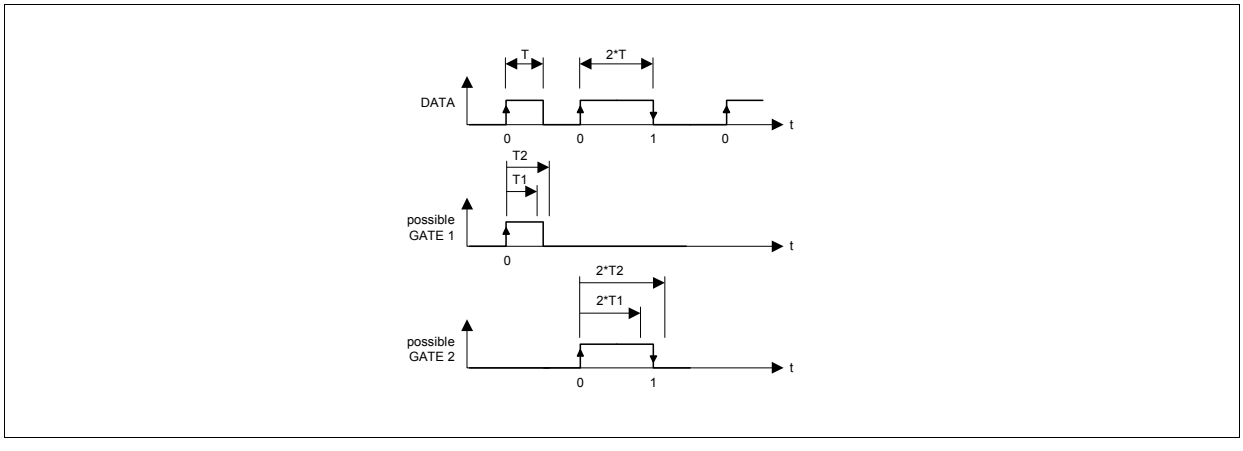
Frequ_Detect_Timing_singleShot_wmf

Figure 3-29 Frequency Detection timing in Single Shot mode

3.7.1 Frequency Window for Data Rate Detection

The high time of data is used to measure the frequency of the data signal. For Manchester coding either the data frequency or half of the data frequency have to be detected corresponding to one high time or twice the high time of data signal.

A time period of 3*2*T is necessary to decide about valid or invalid data.



window_count_timing.wmf

Figure 3-30 Window Counter timing

Example to calculate the thresholds for a given data rate:
- Data signal manchester coded
- Data Rate: 2kbit//s
- f_{clk}= 19.0625 MHz

Then the period equals to

$$2 \cdot T = \frac{1}{2\text{kbit/s}} = 0{,}5\text{ms} \qquad [3-36]$$

respectively the high time is 0,25ms.
We set the thresholds to +-10% and get: T1= 0,225ms and T2= 0,275ms

The thresholds TH1 and TH2 are calculated with following formulas

$$TH1 = T1 \cdot \frac{f_{clk}}{4} \qquad [3-37]$$

$$TH2 = T2 \cdot \frac{f_{clk}}{4} \qquad [3-38]$$

This yields the following results:

$$TH1 \sim 1072 = 010000110000_b$$
$$TH2 \sim 1310 = 010100011110_b$$

which have to be programmed into the **D0** to **D11** bits of the **COUNT_TH1** and **COUNT_TH2** registers (subaddresses 06H and 07H), respectively.

Default values (window counter inactive):
TH1= 000000000000_b
TH2= 000000000001_b

Note: The timing window of +-10% of a given high time T in general does not correspond to a frequency window +-10% of the calculated data frequency.

3.7.2 RSSI threshold voltage - RF input power

The RF input power level is corresponding to a certain RSSI voltage, which can be seen in Section 3.5. The threshold TH3 of this RSSI voltage can be calculated with the following formula:

$$TH3 = \frac{desired\ RSSI\ threshold\ voltage}{1.2V} \cdot (2^6 - 1) \qquad [3 - 39]$$

As an example a desired RSSI threshold voltage of 500mV results in TH3~26=011010$_b$, which has to be written into D0 to D5 of the RSSI_TH3 register (sub address 08H).

Default value (RSSI detection inactive):

TH3=111111$_b$

3.8 Calculation of ON_TIME and OFF_TIME

ON= (2^{16}-1)-(f_{RC}*t_{ON}) [3 – 40]

OFF=(2^{16}-1)-(f_{RC}*t_{OFF}) [3 – 41]

f_{RC}= Frequency of internal RC Oszillator

Example: t_{ON}= 0,005s, t_{OFF}= 0,055s, f_{RC}= 32300Hz

ON= 65535-(32300*0,005) ~ 65373= 1111111101011101$_b$

OFF= 65535-(32300*0,055) ~ 63758= 1111100100001110$_b$

The values have to be written into the **D0** to **D15** bits of the **ON_TIME** and **OFF_TIME** registers (subaddresses 04H and 05H).

Default values:

ON= 65215 = 1111111011000000$_b$

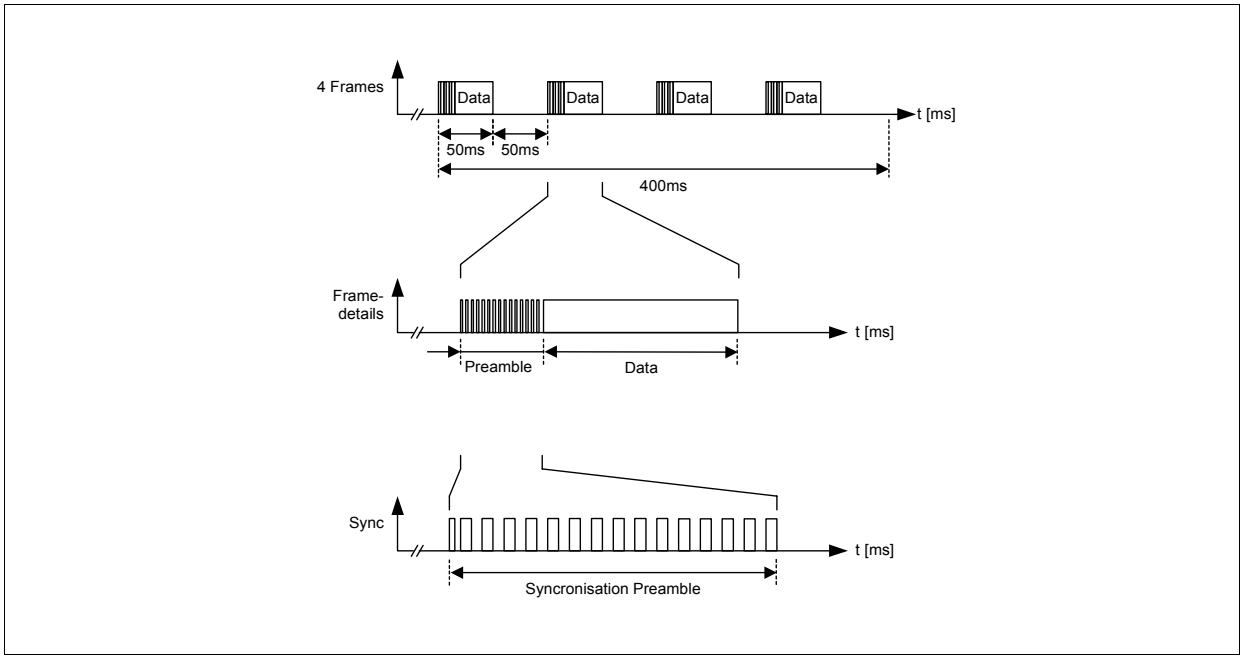
OFF= 62335 = 1111001110000000$_b$

t_{ON} ~10ms @ f_{RC}= 32kHz

t_{OFF} ~100ms @ f_{RC}= 32kHz

3.9 Example for Self Polling Mode

The settings for Self Polling Mode depend very much on the timing of the transmitted Signal. To create an example we consider following data structure transmitted in FSK.



data_timing011.wmf

Figure 3-31 Example for transmitted Data-structure

According to existing synchronization techniques there are some synchronization bursts in front of the data added (code violation!). A minimum of 4 Frames is transmitted. Data are preferably Manchester encoded to get fastest respond out of the Data Rate Detection.

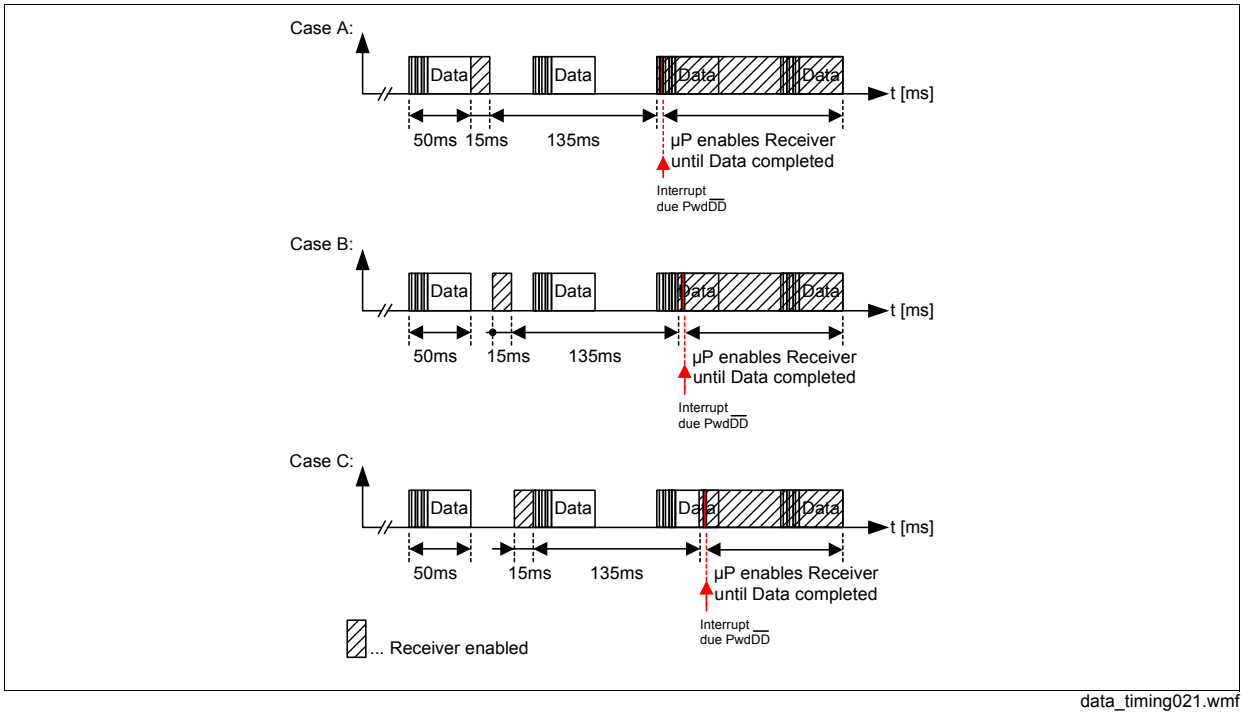
Target Application:

- received Signal has code violation as described before
- total mean current consumption below 1mA
- data reception within max. 400ms after first transmitted frame

One possible Solution:

t_{ON} = 15ms, t_{OFF}= 135ms

This gives 15ms ON time of a total period of 150ms which results in max. 0.9mA mean current consumption in Self Polling Mode. The resulting worst case timing is shown in the following figure:



data_timing021.wmf

Figure 3-32 3 possible timings

Description:

Assumption: the ON time comes right after the first frame (Case A). If OFF time is 135ms the receiver turns on during Sync-pulses and the PwdDD- pulse wakes up the µP.
If the ON time is in the center of the 50ms gap of transmission (Case B), the Data Detect Logic will wake up the µP 135ms later.
If ON time is over just before Sync-pulses (Case C), next ON time is during Data transmission and Data Detect Logic will trigger a PwdDD- pulse to wake up the µP.

Note: In this example it is recommended to use the Peak Detector for slicer threshold generation, because of its fast attack and slow release characteristic. To overcome the data zero gap of 50ms larger external capacitors than noted in **Section 4.4** at pin12 and 13 are recommended. Further information on calculating these components can be taken from **Section 3.6.2**.

3.10 Default Setup

Default setup is hard wired on chip and effective after a reset or return of power supply.

Table 3-14 Default Setup

Parameter	Value	IFX-Board	Comment
IQ-Filter Bandwidth	150kHz		
Data Filter Bandwidth	7kHz		
Limiter lower fg	470Hz	47nF	
Slicing Level Generation	RC	10nF	
Nom. Frequency Capacity intern (ASK TX, FSK RX)	4.5pF	915MHz	
FSK+ Frequency Capacity intern (FSK+, ASK RX)	2.5pF	+50kHz	
FSK- Frequency Capacity intern (FSK-)	1.5pF	-50kHz	
LNA Gain	HIGH		
Power Amplifier	HIGH	+10dBm	
RSSI accuracy settling time	2.6ms	2.2nF	
ADC measurement	RSSI		
ON-Time	10ms		
OFF-Time	100ms		
Clock out RX PowerON	1.06MHz		
Clock out TX PowerON	1.06MHz		
Clock out RX PowerDOWN	-		
Clock out TX PowerDOWN	-		
XTAL modulation switch	bipolar		
XTAL modulation shaping	off		
RX / TX	-	Jumper	
ASK/FSK	-	Jumper	
PwdDD	PWDN	Jumper removed	
Operating Mode	Slave		

4 Reference

4.1 Electrical Data

4.1.1 Absolute Maximum Ratings

WARNING

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC may result.
The AC/DC characteristic limits are not guaranteed.

Table 4-1 Absolute Maximum Ratings

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min	max		
1	Supply Voltage	V_s	-0.3	5.8	V	
2	Junction Temperature	T_j	-40	+125	°C	
3	Storage Temperature	T_s	-40	+150	°C	
4	Thermal Resistance	R_{thJA}		114	K/W	
5	ESD integrity, all pins	$V_{ESD-CDM}$	-1.5	+1.5	kV	CDM according EIA/JESD22-C101
6	ESD integrity, except pin 8, 9, 11, 15, 18, 23, 30	$V_{ESD-HBM}$	-2.0	+2.0	kV	HBM according EIA/JESD22-A114-B (1.5kΩ, 100pF)
7	ESD integrity, of pin 8, 9, 11, 15, 18, 23, 30	$V_{ESD-HBM}$	-500	+500	V	HBM according EIA/JESD22-A114-B (1.5kΩ, 100pF)

4.1.2 Operating Range

Within the operational range the IC operates as explained in the circuit description.

Table 4-2 Operating Range

#	Parameter	Symbol	Limit Values		Unit	Test Conditions	L	Item
			min	max				
1	Supply voltage	V_S	2.1	5.5	V			
2	Ambient temperature	T_A	-40	85	°C			
3	Receive frequency	f_{RX}	910	920	MHz			
4	Transmit frequency	f_{TX}	910	920	MHz			

4.1.3 AC/DC Characteristics

AC/DC characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production. The device performance paramter marked with x are not part of the production test, but were either verified by design or measured in an Infineon Evalboard as described in Section 4-2.

Table 4-3 AC/DC Characteristics with T_A = 25 °C, V_{VCC} = 2.1 ... 5.5 V

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
RECEIVER Characteristics									
1	Supply current RX FSK	I_{RX_FSK}		9.0		mA	3V, FSK, Default		
2	Supply current RX FSK	I_{RX_FSK}		9.5		mA	5V, FSK, Default		
3	Supply current RX ASK	I_{RX_ASK}		8.6		mA	3V, ASK, Default		
4	Supply current RX ASK	I_{RX_ASK}		9.1		mA	5V, ASK, Default		
5	Sensitivity FSK 10^{-3} BER	RFsens		-109		dBm	FSK@30kHz, 4kBit/s Manch. Data, Default 7kHz datafilter, 50kHz IQ filter	X	
6	Sensitivity ASK 10^{-3} BER	RFsens		-109		dBm	ASK, 4kBit/s Manch. data, Default setup 7kHz datafilter, 50kHz IQ filter	X	
7	Power down current	I_{PWDN_RX}		5		nA	5.5V, all power down		
8	System setup time (1st power on or reset)	t_{SYSSU}	4	8	12	ms			
9	Clock Out setup time	t_{CLKSU}		0.5		ms	stable CLKDIV output signal		
10	Receiver setup time	t_{RXSU}	1.54	2.2	2.86	ms	DATA out (valid or invalid)		
11	Data detection setup time	t_{DDSU}	1.82	2.6	3.38	ms	Begin of Data detection		
12	RSSI stable time	t_{RSSI}	1.82	2.6	3.38	ms	RFin -100dBm see chapter 4.5		
13	Data Valid time	t_{Data_Valid}		3.35		ms	4kBit/s Manch. detected (valid)		
14	Input P_{1dB}, high gain	P_{1dB}		-48dBm		dBm	3V, Default, high gain	X	
15	Input P_{1dB}, low gain	P_{1dB_low}		-32dBm		dBm	3V, Default, low gain	X	
16	Selectivity	V_{BL_1MHz}		50		dB	f_{RF}+/-1MHz, Default, RF_{sens}+3dB	X	
17	LO Leakage	P_{LO}		-90		dB	1220MHz		

Table 4-3 AC/DC Characteristics with T_A = 25 °C, V_{VCC} = 2.1 ... 5.5 V

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
TRANSMITTER Characteristics									
1	Supply current TX, FSK	I_{TX}		9.5		mA	2.1V, high power		1
2	Supply current TX, FSK	I_{TX}		12.5		mA	3V, high power		1
3	Supply current TX, FSK	I_{TX}		15		mA	5V, high power		1
4	Output power	P_{out}		+6		dBm	2.1V, high power	X	
5	Output power	P_{out}		+9		dBm	3V, high power	X	
6	Output power	P_{out}		+13		dBm	5V, high power	X	
7	Supply current TX, FSK	I_{TX}		4,1		mA	2.1V, low power		1
8	Supply current TX, FSK	I_{TX}		4.9		mA	3V, low power		1
9	Supply current TX, FSK	I_{TX}		6.8		mA	5V, low power		1
10	Output power	P_{out_low}		-30		dBm	2.1V, low power	X	
11	Output power	P_{out_low}		-22		dBm	3V, low power	X	
12	Output power	P_{out_low}		-3		dBm	5V, low power	X	
13	Power down current	I_{PWDN_TX}		5		nA	5.5V, all power down		
14	Clock Out setup time	t_{CLKSU}		0.5		ms	stable CLKDIV output signal		
15	Transmitter setup time	t_{TXSU}	0.77	1.1	1.43	ms	PWDN-->PON or RX-->TX	X	
16	Spurious f_{RF}+/-f_{XTAL}	P_{1st}		-72/-69		dBm	3V, 50Ohm Board	X	
17	Spurious 2nd harmonic	P_{2nd}		-45		dBm	3V, 50Ohm Board	X	
18	Spurious 3rd harmonic	P_{3rd}		-49		dBm	3V, 50Ohm Board	X	

1: without pin diode current (RX/TX-switch)
130uA@2.1V; 310uA@3V; 720uA@5V

Table 4-4 AC/DC Characteristics with T_A = 25 °C, V_{VCC} = 2.1 ... 5.5 V

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
GENERAL Characteristics									
1	Power down current timer mode (standby)	I_{PWDN_32k}		9		uA	3V, 32kHz clock on		
2	Power down current timer mode (standby)	I_{PWDN_32k}		11		uA	5V, 32kHz clock on		
3	Power down current with XTAL ON	I_{PWDN_Xtl}		750		uA	3V, CONFIG9=1		
4	Power down current with XTAL ON	I_{PWDN_Xtl}		860		uA	5V, CONFIG9=1		
5	32kHz oscillator freq.	f_{32kHz}	24	32	40	kHz			
6	XTAL startup time	t_{XTAL}		0.5		ms	IFX Board with Crystal Q1 as specified in **Section 4.4**	X	
7	Load capacitance	C_{C0max}		5		pF		X	
8	Serial resistance of the crystal	R_{Rmax}			100	Ω		X	
9	Input inductance XOUT	L_{OSC}		2.75		uH	with pad on evaluation board	X	
10	Input inductance XOUT	L_{OSC}		2.5		uH	without pad on evaluation board	X	
11	FSK demodulator gain	G_{FSK}		2.4		mV/ kHz			
12	RSSI@-120dBm	$U_{-120dBm}$		0.35		V	default setup	X	
13	RSSI@-100dBm	$U_{-100dBm}$		0.55		V	default setup	X	
14	RSSI@-70dBm	U_{-70dBm}		1		V	default setup	X	
15	RSSI@-50dBm	U_{-50dBm}		1.2		V	default setup	X	
16	RSSI Gradient	G_{RSSI}		14		mV/ dB	default setup	X	
17	IQ-Filter bandwidth	f_{3dB_IQ}	115	150	185	kHz	Default setup	X	
18	Data Filter bandwidth	f_{3dB_LP}	5.3	7	8.7	kHz	Default setup	X	
19	Vcc-Vtune RX, Pin3	$V_{cc\text{-}tune,RX}$	0.5	1	1.6	V	f_{Ref}=19.0625MHz		
20	Vcc-Vtune TX, Pin3	$V_{cc\text{-}tune,TX}$	0.5	1.1	1.6	V	f_{Ref}=19.0625MHz		

„X“ Not part of the production test - either verified by design or measured in an Infineon Evalboard as described in Section 4-2.

4.1.4 Digital Characteristics

I²C Bus Timing

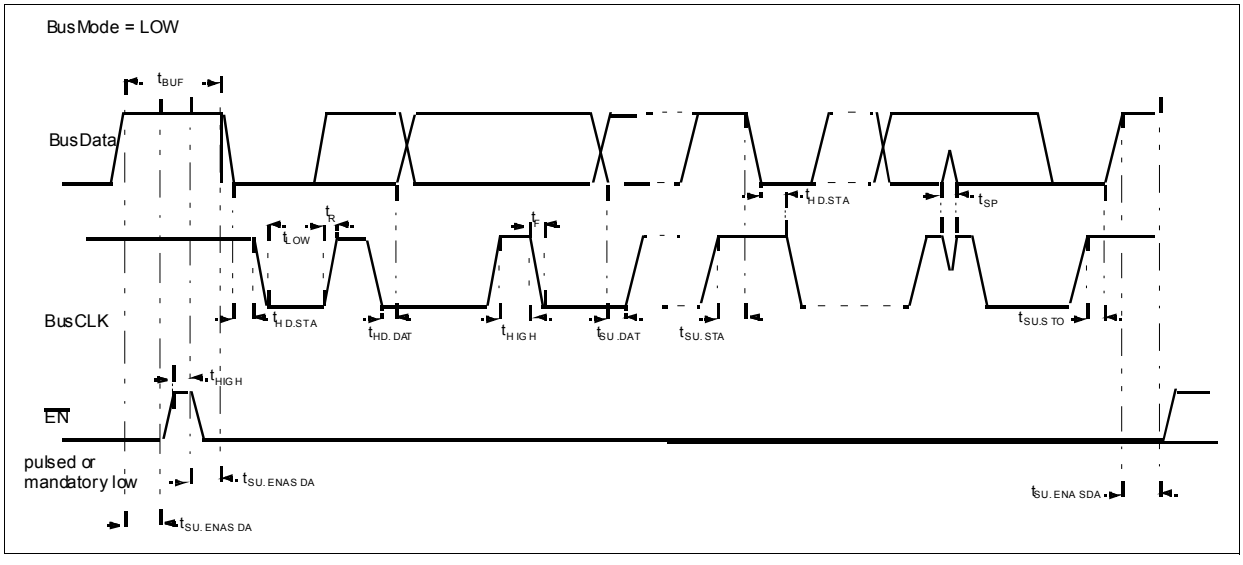


Figure 4-1 I²C Bus Timing

3-wire Bus Timing

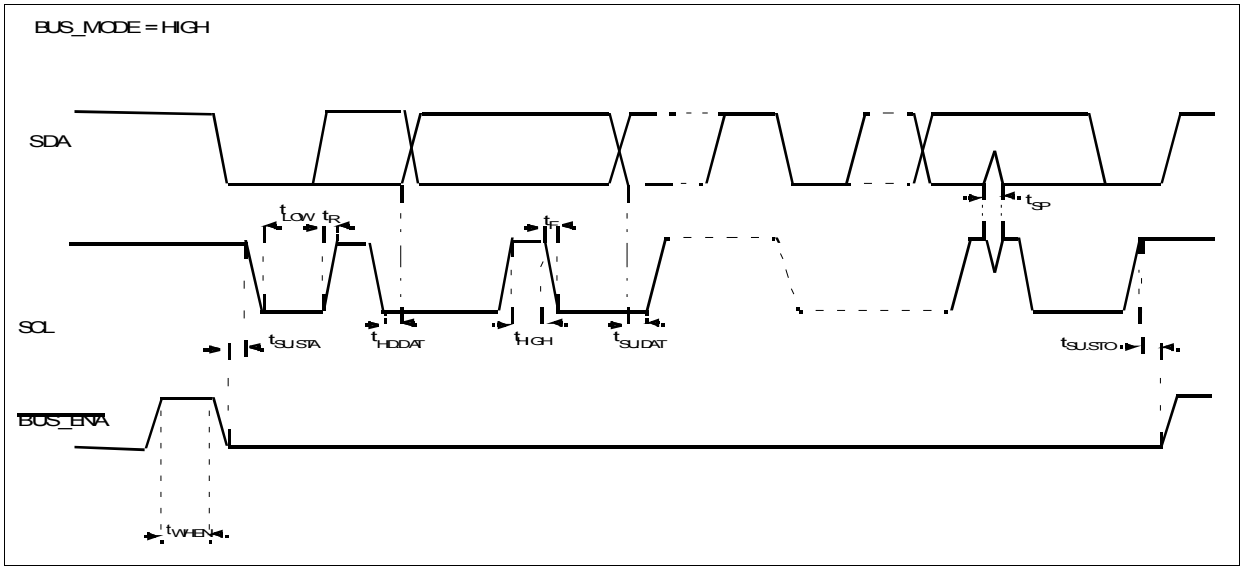


Figure 4-2 3-wire Bus Timing

Table 4-5 Digital Characteristics with T_A = 25 °C, V_{Vdd} = 2.1 ... 5.5 V									
#	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
1	Data rate TX ASK	$f_{TX.ASK}$		10	25	kBaud	PRBS9, Manch.@+9dBm	X	1
2	Data rate TX ASK	$f_{TX.ASK}$		10	64	kBaud	PRBS9, Manch.@-5dBm	X	1
3	Data rate TX FSK	$f_{TX.FSK}$		10	40	kBaud	PRBS9, Manch.@+9dBm @30kHz dev.	X	1
4	Data rate RX ASK	$f_{RX.ASK}$		10	64	kBaud	PRBS9, Manch.	X	
5	Data rate RX FSK	$f_{RX.FSK}$		10	64	kBaud	PRBS9, Manch. @30kHz dev.	X	
6	Digital Inputs High-level Input Voltage Low-level Input Voltage	 V_{IH} V_{IL}	 V_{dd}-0.2 0		 V_{dd} 0.2	 V V		X	
7	RXTX Pin 5 TX operation, int. controlled	V_{OL}		0.4 1.15		V V	@Vdd=3V Isink=800uA Isink=3mA	X	
8	CLKDIV Pin 26 t_{rise} (0.1*Vdd to 0.9*Vdd) t_{fall} (0.9*Vdd to 0.1*Vdd) Output High Voltage Output Low Voltage	 t_r t_f V_{OH} V_{OL}		 35 30 Vdd-0.4 0.4		 ns ns V V	 @Vdd=3V load 10pF load 10pF I_{source}=350uA I_{sink}=400uA	X	

Bus Interface Characteristics

9	Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0		50	ns	V_{dd}=5V	X	
10	LOW level output voltage at BusData	V_{OL}			0.4	V	3mA sink current V_{dd}=5V	X	
11	SLC clock frequency	f_{SLC}	0		400	kHz	V_{dd}=5V	X	
12	Bus free time between STOP and START condition	t_{BUF}	1.3			µs	only I^2C mode V_{dd}=5V	X	
13	Hold time (repeated) START condition.	$t_{HO.STA}$	0.6			µs	After this period, the first clock pulse is generated, only I^2C	X	

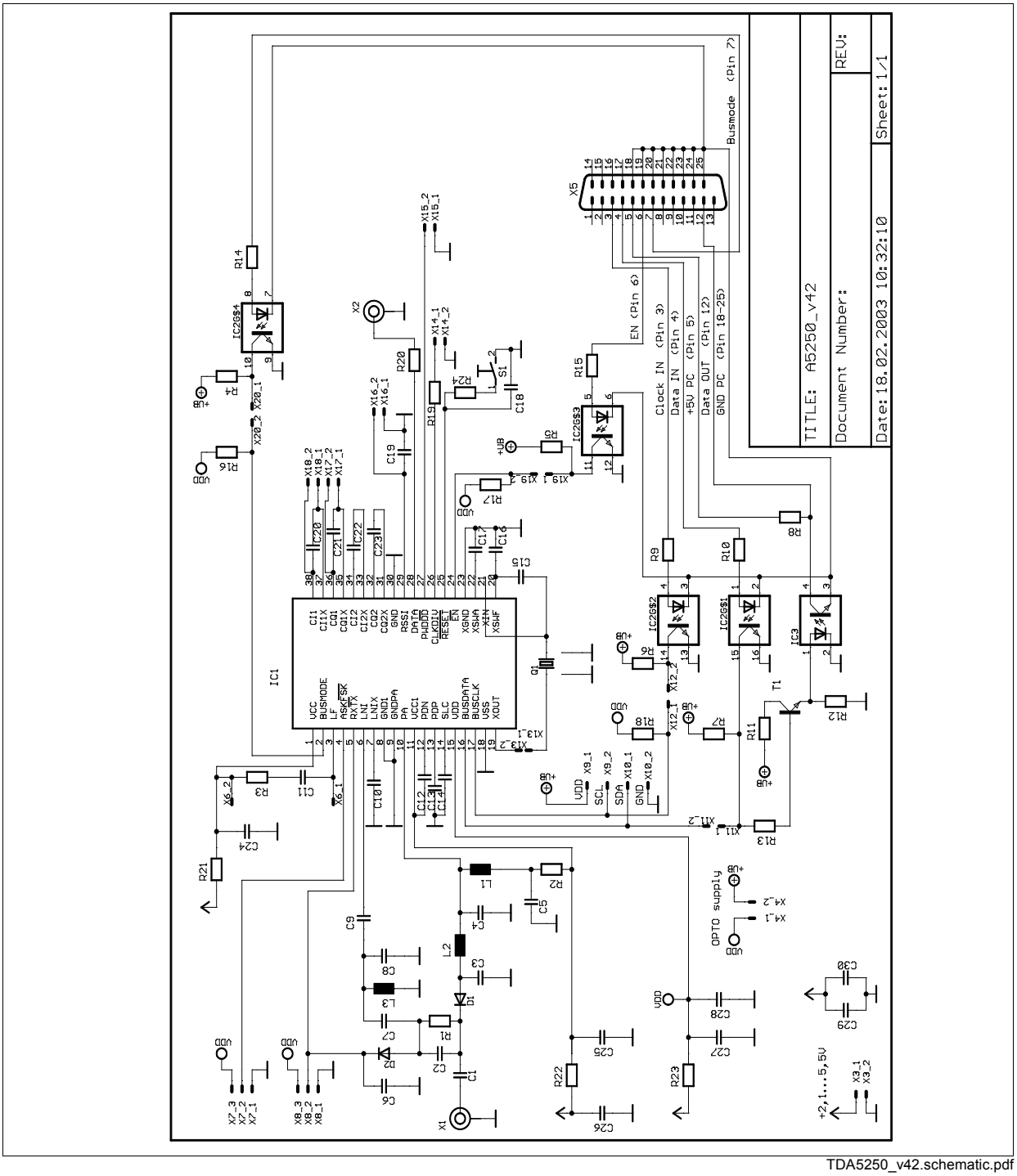
Table 4-5 Digital Characteristics with T_A = 25 °C, V_{Vdd} = 2.1 ... 5.5 V

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
14	LOW period of BusCLK clock	t_{LOW}	1.3			µs	V_{dd}=5V	X	
15	HIGH period of BusCLK clock	t_{HIGH}	0.6			µs	V_{dd}=5V	X	
16	Setup time for a repeated START condition	$t_{SU.STA}$	0.6			µs	only I^2C mode	X	
17	Data hold time	$t_{HD.DAT}$	0			ns	V_{dd}=5V	X	
18	Data setup time	$t_{SU.DAT}$	100			ns	V_{dd}=5V	X	
19	Rise, fall time of both BusData and BusCLK signals	t_R, t_F	20+ 0.1C_b		300	ns	V_{dd}=5V	X	2
20	Setup time for STOP condition	$t_{SU.STO}$	0.6			µs	only I^2C mode V_{dd}=5V	X	
21	Capacitive load for each bus line	C_b			400	pF	V_{dd}=5V	X	
22	Setup time for BusCLK to EN	$t_{SU.SCLEN}$	0.6			µs	only 3-wire mode V_{dd}=5V	X	
23	H-pulsewidth (EN)	t_{WHEN}	0.6			µs	V_{dd}=5V	X	

X: Not part of the production test - either verified by design or measured in an Infineon Evalboard as described in Section 4-2.
1: limited by transmission channel bandwidth and depending on transmit power level; ETSI regulation EN 300 220 fullfilled.
2: C_b= capacitance of one bus line

4.2 Test Circuit

The device performance parameters marked with X in **Section 4.1.3** were either verified by design or measured on an Infineon evaluation board (IFX board).

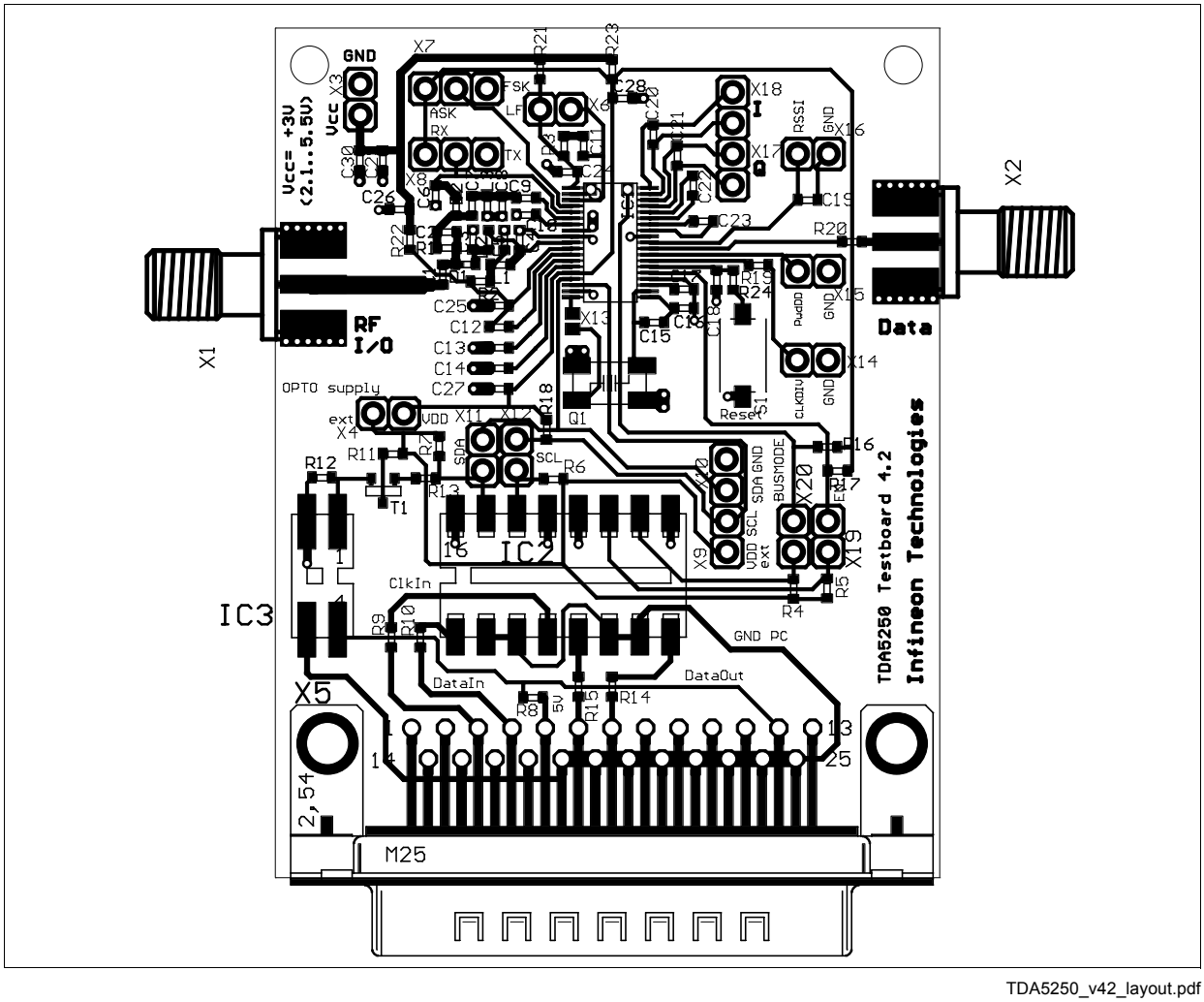


TDA5250_v42.schematic.pdf

Figure 4-3 Schematic of the Evaluation Board

4.3 Test Board Layout

Gerberfiles for this Testboard are available on request.



TDA5250_v42_layout.pdf

Figure 4-4 Layout of the Evaluation Board

Note 1: The LNA and PA matching network was designed for minimum required space and maximum performance and thus via holes were deliberately placed into solder pads.

In case of reproduction please bear in mind that this may not be suitable for all automatic soldering processes.

Note 2: Please keep in mind not to layout the CLKDIV line directly in the neighborhood of the crystal and the associated components.

Note 3: The opto part (X4) should be supplied by connecting to X3.

4.4 Bill of Materials

Table 4-6 Bill of Materials

Reference	Value	Specification	Tolerance
R1	4k7	0603	+/-5%
R2	10R	0603	+/-5%
R3	---	---	---
R4	1M	0603	+/-5%
R5	4k7	0603	+/-5%
R6	4k7	0603	+/-5%
R7	4k7	0603	+/-5%
R8	6k8	0603	+/-5%
R9	180	0603	+/-5%
R10	180	0603	+/-5%
R11	270	0603	+/-5%
R12	15k	0603	+/-5%
R13	10k	0603	+/-5%
R14	180	0603	+/-5%
R15	180	0603	+/-5%
R16	1M	0603	+/-5%
R17	1M	0603	+/-5%
R18	1M	0603	+/-5%
R19	560	0603	+/-5%
R20	1k	0603	+/-5%
R21	10	0603	+/-5%
R22	0	0603	+/-5%
R23	10	0603	+/-5%
R24	180	0603	+/-5%
C1	22p	0603	+/-5%
C2	1p	0603	+/-0,1pF
C3	4p7	0603	+/-0.1pF
C4	1p8	0603	+/-0,1pF
C5	1nF	0603	+/-5%
C6	1nF	0603	+/-5%
C7	6p8	0603	+/-0,1pF
C8	---	---	---
C9	18p	0603	+/-1%
C10	22pF	0603	+/-5%
C11	---	---	---
C12	10nF	0603	+/-10%
C13	10nF	0603	+/-10%

Table 4-6 Bill of Materials

Reference	Value	Specification	Tolerance
C14	10nF	0603	+/-10%
C15	8.2pF	0603	+/-1%
C16	6.8pF	0603	+/-0,1pF
C17	22pF	0603	+/-1%
C18	10nF	0603	+/-10%
C19	2,2nF	0603	+/-10%
C20	47nF	0603	+/-10%
C21	47nF	0603	+/-10%
C22	47nF	0603	+/-10%
C23	47nF	0603	+/-10%
C24	100nF	0603	+/-10%
C25	100nF	0603	+/-10%
C26	---	---	---
C27	100nF	0603	+/-10%
C28	100nF	0603	+/-10%
C29	100nF	0603	+/-10%
C30	---	0603	+/-10%
L1	68n	SIMID 0603-C (EPCOS)	+/-2%
L2	12n	SIMID 0603-C (EPCOS)	+/-2%
L3	8.2n	SIMID 0603-C (EPCOS)	+/-2%
IC1	TDA5252	PTSSOP38	
IC2	ILQ74		
IC3	SFH6186		
Q1	19.0625MHz	Hz HDG0647 CL= 20pF Spec.No. 1054-003	Freq. Tolerance +/- 10ppm Temp. Tolerance +/- 20ppm
S1	1-pol.		
T1	BC847B	SOT-23 (Infineon)	
D1, D2	BAR63-02W	SCD-80 (Infineon)	
X1, X2	SMA-socket		
X5	SubD 25p.		

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