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National Semiconductor

May 1995

54F/74F373
Octal Transparent Latch with TRI-STATE® Outputs

General Description

The 'F373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

Features

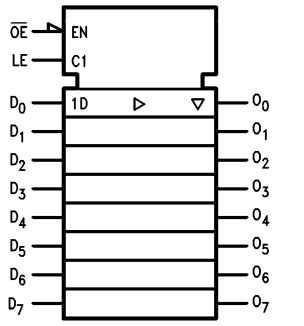
- Eight latches in a single package
- TRI-STATE outputs for bus interfacing
- Guaranteed 4000V minimum ESD protection

Commercial	Military	Package Number	Package Description
74F373PC		N20A	20-Lead (0.300″ Wide) Molded Dual-In-Line
	54F373DM (QB)	J20A	20-Lead Ceramic Dual-In-Line
74F373SC (Note 1)		M20B	20-Lead (0.300″ Wide) Molded Small Outline, JEDEC
74F373SJ (Note 1)		M20D	20-Lead (0.300″ Wide) Molded Small Outline, EIAJ
74F373MSA (Note 1)		MSA20	20-Lead Molded Shrink Small Outline, EIAJ Type II
	54F373FM (QB)	W20A	20-Lead Cerpack
	54F373LM (QB)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

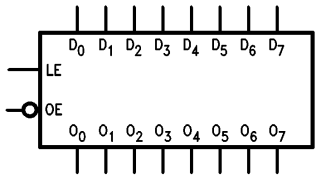
Note 1: Devices also available in 13″ reel. Use suffix = SCX, SJX, and MSAX.

Logic Symbols

IEEE/IEC



TL/F/9523–4



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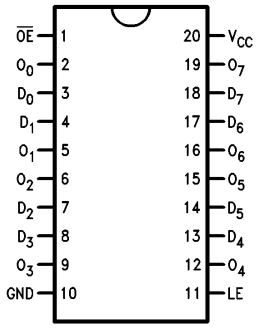
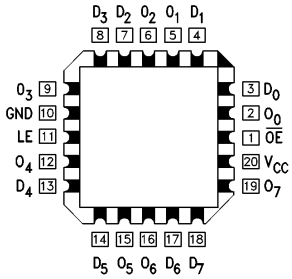
Connection Diagrams

Pin Assignment for DIP, SOIC, SSOP and Flatpak



TL/F/9523–2

Pin Assignment for LCC



TL/F/9523–3

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RRD-B30M75/Printed in U. S. A.

Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0–D_7	Data Inputs	1.0/1.0	20 μA/ −0.6 mA
LE	Latch Enable Input (Active HIGH)	1.0/1.0	20 μA/ −0.6 mA
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/1.0	20 μA/ −0.6 mA
O_0–O_7	TRI-STATE Latch Outputs	150/40 (33.3)	−3 mA/24 mA (20 mA)

Functional Description

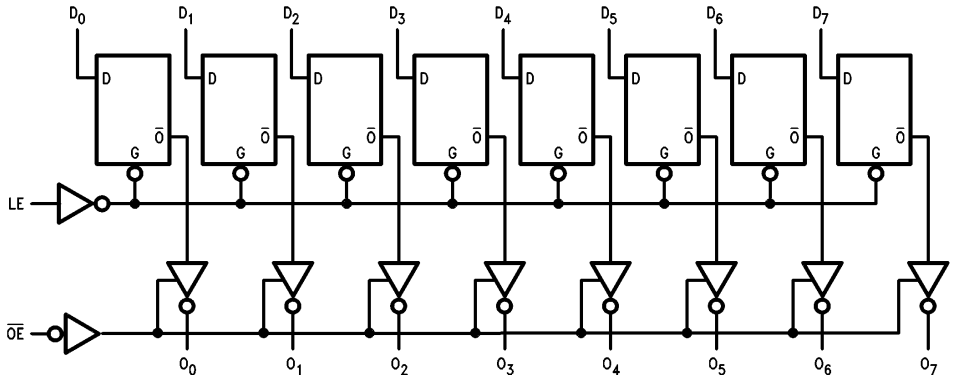
The ’F373 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Output
LE	$\overline{OE}$	D_n	O_n
H	L	H	H
H	L	L	L
L	L	X	O_n (no change)
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance State

Logic Diagram



TL/F/9523–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		54F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		74F 10% V_{CC}			0.5			I_{OL} = 24 mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current				50	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	μA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25V
I_{CCZ}	Power Supply Current			38	55	mA	Max	V_O = HIGH Z

AC Electrical Characteristics

Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54F T_A, V_{CC} = Mil, $C_L = 50$ pF		74F T_A, V_{CC} = Com, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	3.0	5.3	7.0	3.0	8.5	3.0	8.0	ns
t_{PHL}	D_n to O_n	2.0	3.7	5.0	2.0	7.0	2.0	6.0	
t_{PLH}	Propagation Delay	5.0	9.0	11.5	5.0	15.0	5.0	13.0	ns
t_{PHL}	LE to O_n	3.0	5.2	7.0	3.0	8.5	3.0	8.0	
t_{PZH}	Output Enable Time	2.0	5.0	11.0	2.0	13.5	2.0	12.0	ns
t_{PZL}		2.0	5.6	7.5	2.0	10.0	2.0	8.5	
t_{PHZ}	Output Disable Time	1.5	4.5	6.5	1.5	10.0	1.5	7.5	ns
t_{PLZ}		1.5	3.8	5.0	1.5	7.0	1.5	6.0	

AC Operating Requirements

Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$		54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units
		Min	Max	Min	Max	Min	Max	
$t_s(H)$	Setup Time, HIGH or LOW	2.0		2.0		2.0		ns
$t_s(L)$	D_n to LE	2.0		2.0		2.0		
$t_h(H)$	Hold Time, HIGH or LOW	3.0		3.0		3.0		
$t_h(L)$	D_n to LE	3.0		4.0		3.0		
$t_w(H)$	LE Pulse Width, HIGH	6.0		6.0		6.0		ns

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74F 373 S C X

Temperature Range Family
74F = Commercial
54F = Military

Device Type

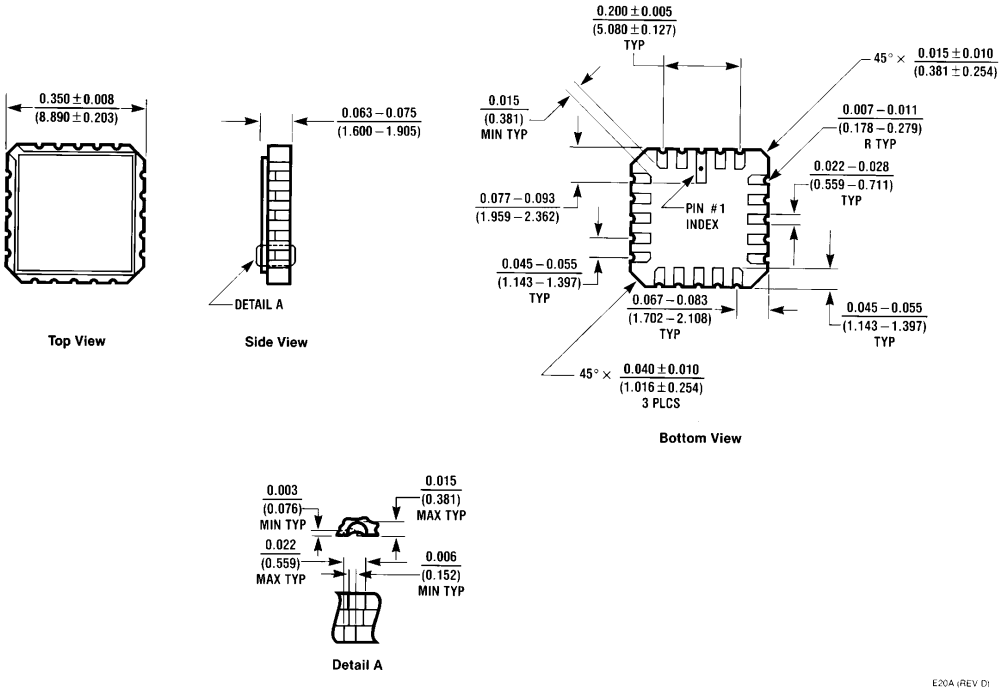
Package Code
P = Plastic DIP
D = Ceramic DIP
F = Flatpak
L = Leadless Chip Carrier (LCC)
S = Small Outline SOIC JEDEC
SJ = Small Outline SOIC EIAJ
MSA = Shrink Small Outline (EIAJ SSOP)

Special Variations
QB = Military grade device with environmental and burn-in processing
X = Devices shipped in 13″ reel

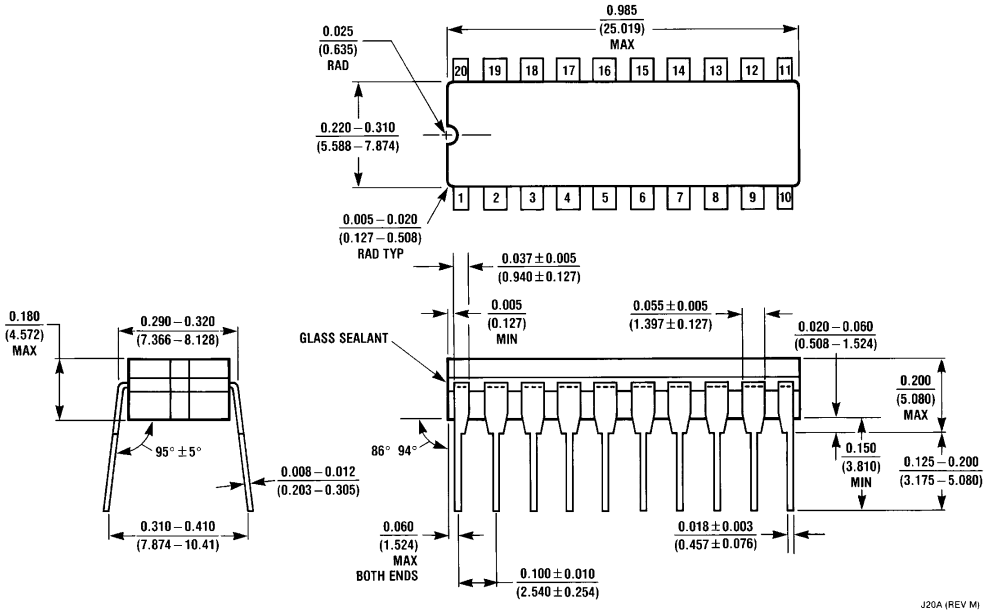
Temperature Range
C = Commercial (0°C to +70°C)
M = Military (−55°C to +125°C)

NOTE:
Not required for MSA package code

Physical Dimensions inches (millimeters)

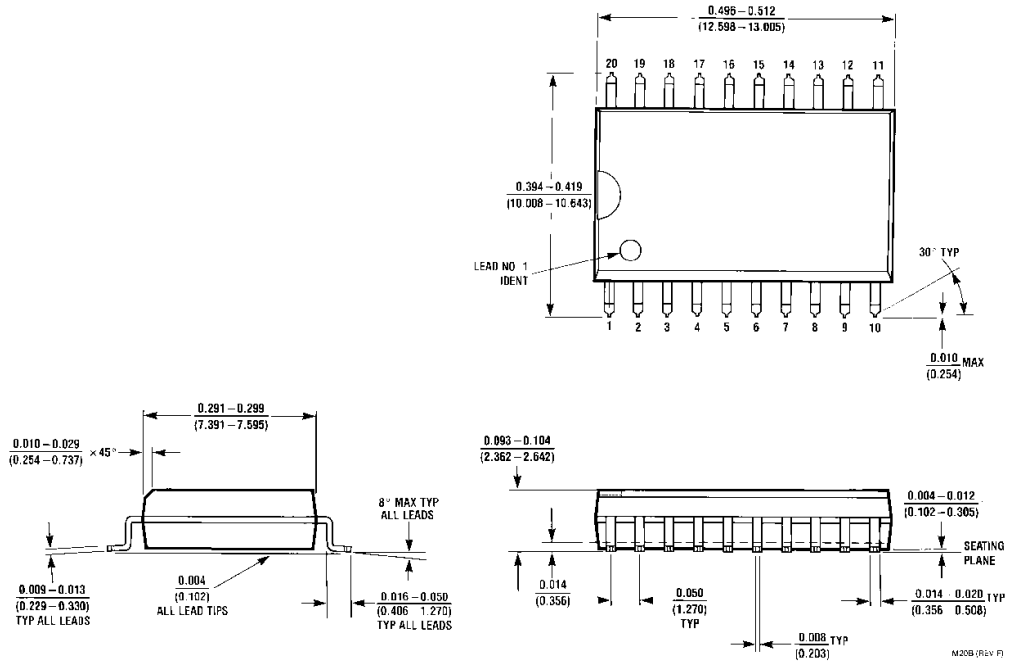


20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

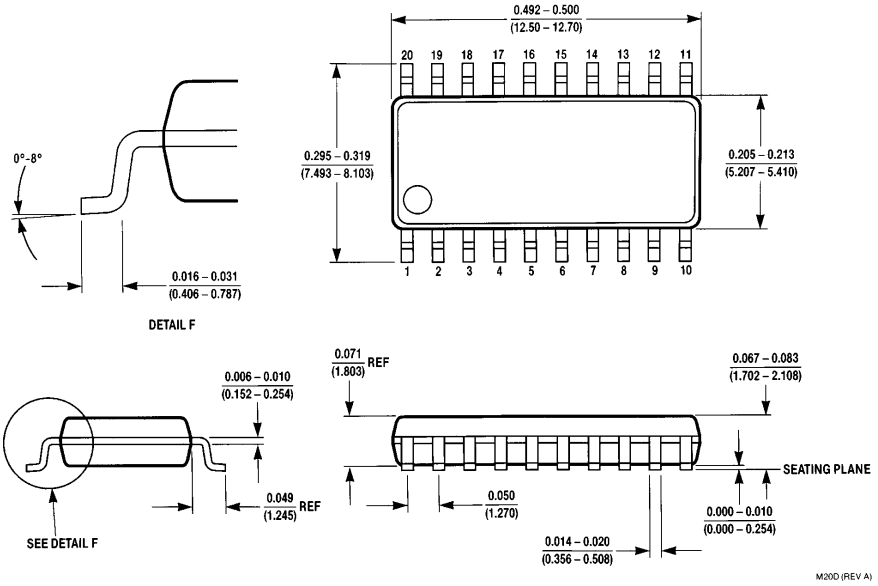


20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

Physical Dimensions inches (millimeters) (Continued)

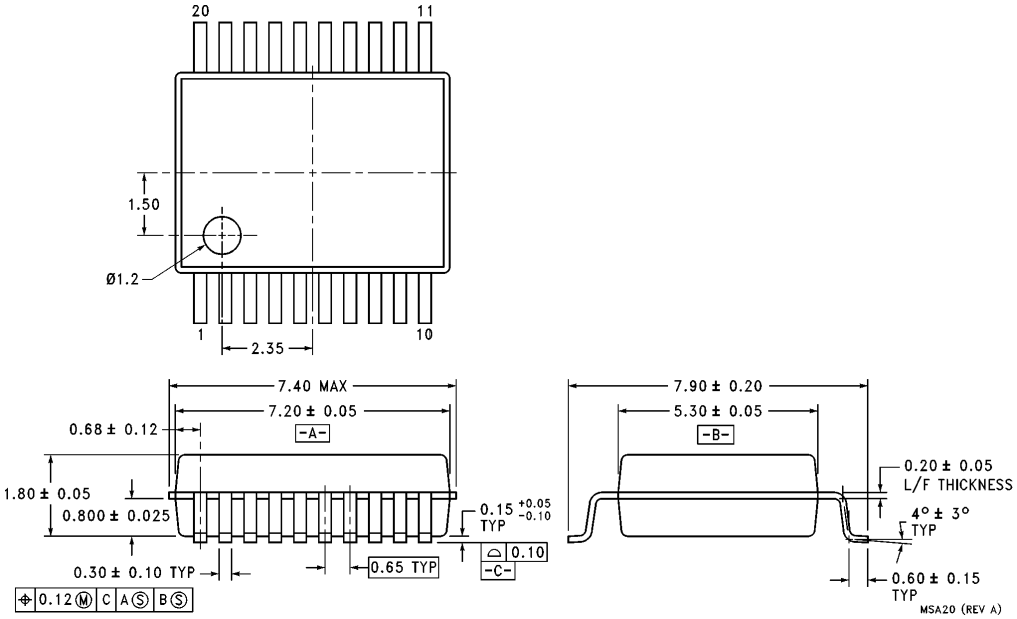


20-Lead (0.300″ Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M20B

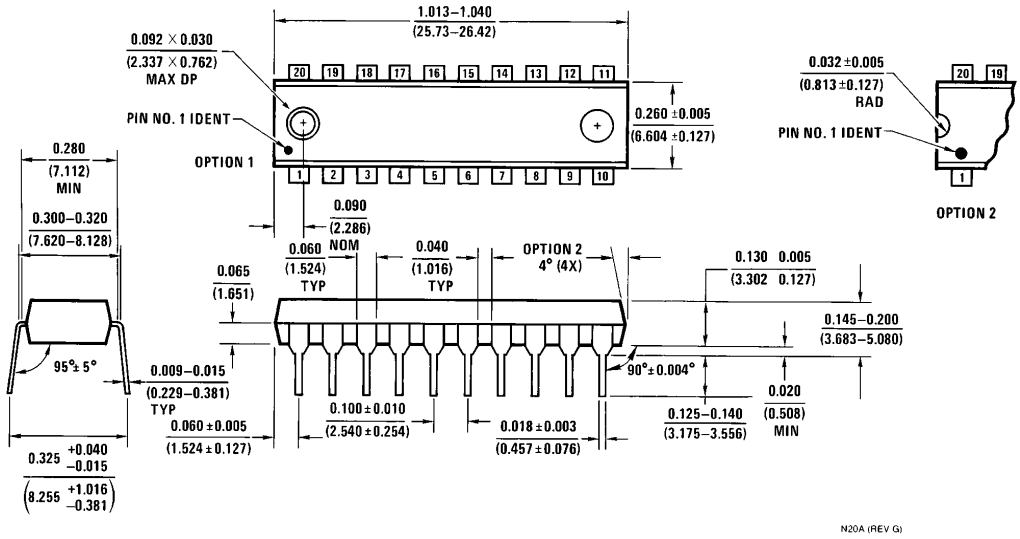


20-Lead (0.300″ Wide) Small Outline Package, EIAJ (SJ)
NS Package Number M20D

Physical Dimensions inches (millimeters) (Continued)

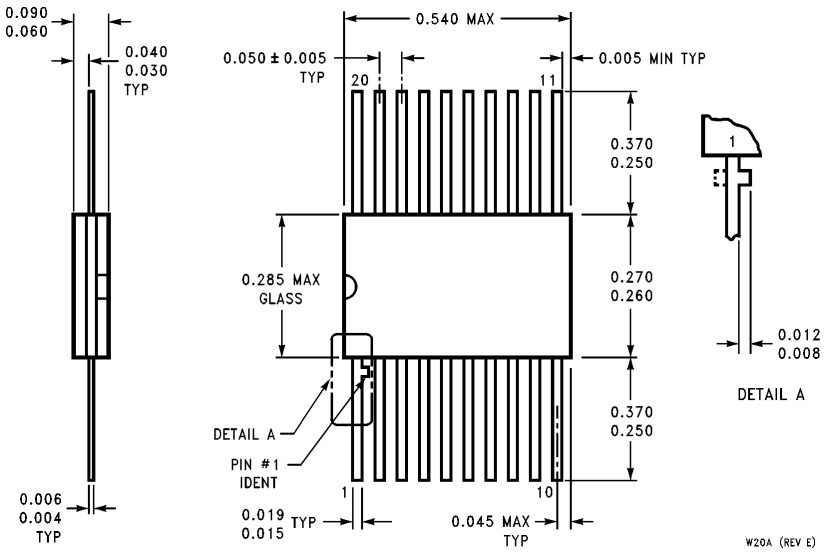


20-Lead Molded Shrink Small Outline Package, EIAJ, Type II (MSA)
NS Package Number MSA20



20-Lead (0.300″ Wide) Molded Dual-In-Line Package (P)
NS Package Number N20A

Physical Dimensions inches (millimeters) (Continued)



20-Lead Ceramic Flatpak (F)
NS Package Number W20A

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54F373 Product Folder

Octal Transparent Latch with TRI-STATE Outputs

General Description | Features | Datasheet | Package & Models | Samples & Pricing

Datasheet

Title	Size in Kbytes	Date	View Online	Download	Receive via Email
54F373 Octal Transparent Latch with TRI-STATE(RM) Outputs	174 Kbytes	9-Dec-97	View Online	Download	Receive via Email
54F373 Mil-Aero Datasheet MN54F373-X	14 Kbytes		View Online	Download	Receive via Email

If you have trouble printing or viewing PDF file(s), see Printing Problems.

Package Availability, Models, Samples & Pricing

Part Number	Package			Status	Models		Samples & Electronic Orders	Budgetary Pricing		Std Pack Size	Package Marking
	Type	Pins	MSL		SPICE	IBIS		Qty	$US each		
54F373LMQB	LCC	20	MSL	Full production	N/A	N/A		50+	$4.4000	rail of 50	[logo]¢Z¢S¢4¢A 54F373 LMQB /Q¢M $E
54F373DMQB	CERDIP	20	MSL	Full production	N/A	N/A	Buy Now	50+	$2.2000	rail of 20	[logo]¢Z¢S¢4¢A$E 54F373DMQB Q¢M
54F373FMQB	CERPACK	20	MSL	Full production	N/A	N/A		50+	$4.0000	rail of 19	[logo]¢Z¢S¢4¢A$E 54F373FMQB Q¢M
JM38510/34601B2	LCC	20	MSL	Full production	N/A	N/A		50+	$4.7500	rail of 50	[logo] JM38510 /34601B2A 27014 QS ¢Z¢S¢4¢A$E
JM38510/34601BR	CERDIP	20	MSL	Full production	N/A	N/A		50+	$2.3200	rail of 20	[logo] ¢Z¢S¢4¢A$E JM38510/34601BRA 27014 QS
JM38510/34601BS	CERPACK	20	MSL	Full production	N/A	N/A		50+	$4.5000	rail of 19	[logo]¢Z¢S¢4¢A$E JM38510/ 34601BSA 27014 QS

JD54F373SRA	CERDIP	20	MSL	Full production	N/A	N/A				rail of N/A	[logo]¢Z¢S¢4¢A$E JM38510/34601SRA 27014 Q
JM38510/34601SS	CERPACK	20	MSL	Full production	N/A	N/A		50+	$145.0000	rail of 19	[logo]¢Z¢S¢4¢A$E 27014 JM38510/ 34601SSA Q

General Description

The 'F373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (OE#) is LOW. When OE# is HIGH the bus output is in the high impedance state.

Features

- Eight latches in a single package
- TRI-STATE outputs for bus interfacing
- Guaranteed 4000V minimum ESD protection

[Information as of 5-Aug-2002]