FS1412 µPOL™

DATASHEET 12A Rated µPOL™ Buck Regulator with Integrated Inductor and Digital Power System Management

Features

- µPOL™ package with output inductor included
- Small size: **5.8mm x 4.9mm x 1.6mm**
- Continuous 12A load capability
- Plug and play: no external compensation required
- Programmable operation using I²C and PMBus™
- Wide input voltage range: 4.5–16V
- Adjustable output voltage: 0.6–1.8V
- Enabled input, programmable under-voltage lock-out (UVLO) circuit
- Open-drain power-good indicator
- Built-in protection features
- Operating temperature from -40°C to +125°C
- Lead-free and halogen-free
- Compliant with EU REACH and RoHS

Applications

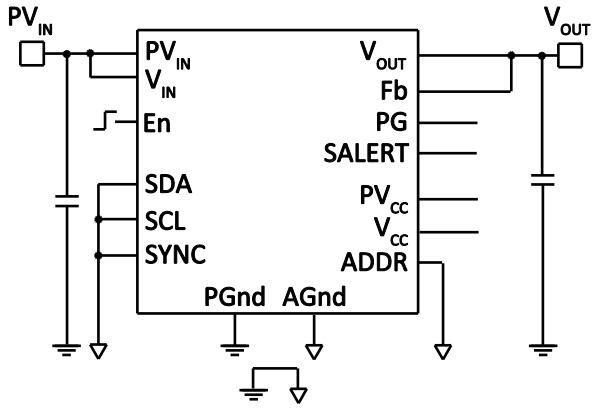
- Telecom, wireless and 5G applications
- Networking and datacenter applications
- Storage applications
- Industrial applications
- Distributed point-of-load power architectures
- Computing peripheral voltage regulation
- General DC-DC conversion

Description

The FS1412 is an easy-to-use, fully integrated and highly efficient micro-point-of-load (µPOL™) voltage regulator. The on-chip pulse-width modulation (PWM) controller and integrated MOSFETs, plus incorporated inductor and capacitors, result in an extremely compact and accurate regulator. The low-profile package is suitable for automated assembly using standard surface-mount equipment.

Developed by a cross-functional engineering team, the design exemplifies best practice and uses class-leading technologies. From early in the integrated circuit design phase, designers worked with application and packaging engineers to select compatible technologies and implement them in ways that reduce compromise. The ability to program aspects of the FS1412's operation using the I²C and PMBus™ protocols is unique in this class of product. Developing and optimizing all these elements together has yielded the smallest, most efficient and fully featured 12A µPOL™ currently available.

The built-in protection features include soft-start protection, over-voltage protection, thermally compensated over-current protection with hiccup mode, thermal shut-down with auto-recovery.



Rev 2.5, July 27, 2022

Pin configuration

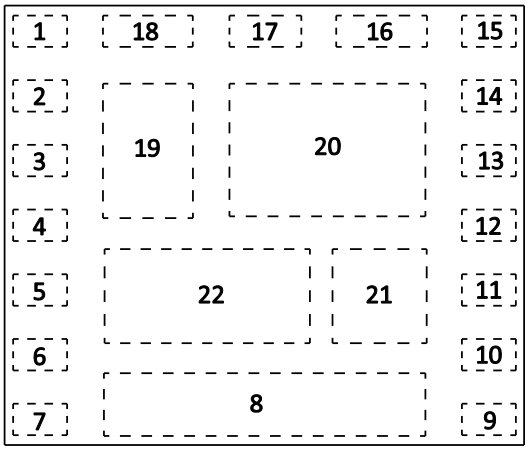


Figure 1 ***Pin layout (top view)***

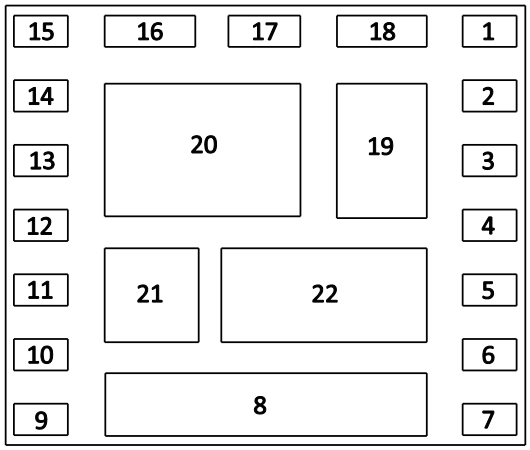


Figure 2 ***Pin layout (bottom view)***

Pin functions

Pin Number	Name	Description
1	SW2	**Test pin**
2	V_{IN}	**Input voltage.** Input for the internal LDO regulator.
3	En	**Enable.** Switches the FS1412 on and off. Can be used with two external resistors to set an external UVLO (Figure 5).
4	PV_{CC}	**Input supply** for the drivers. Connect to V_{CC} on the application board.
5	V_{CC}	**Supply voltage.** May be an input bias for an external V_{CC} voltage or the output of the internal LDO regulator.
6	V_{FB}	**Feedback voltage** to the device. Connect to V_{OUT} on the application board using an external resistor divider to set desired output voltage.
7,22	AGnd	**Signal ground.** Serves as the ground for the internal reference and control circuitry. Connect pins to the PGnd plane through vias.
8	V_{OUT}	**Regulator output voltage.** Place output capacitors and a 100Ω resistor between V_{OUT} and PGnd.
9	PG	**Power Good status.** Open drain of an internal MOSFET. Pull up to V_{CC} – Pin 5 or an external bias voltage with a 49.9kΩ resistor.
10	ADDR	**Address.** Connect to AGnd through a resistor to program FS1412 address.
11	SYNC	**Synchronize** device with external clock. Connect to AGnd if unused.
12	SDA	**I2C/PMBus™ Serial Input/Output line.** Pull up to bus voltage with 4.99kΩ resistor. Connect to AGnd if unused.
13	SCL	**I2C/PMBus™ Clock line.** Pull up to bus voltage with 4.99kΩ resistor. Connect to AGnd if unused.
14	ALERT	SMBAlert# line. Pull up to bus voltage with 4.99kΩ resistor.
15	SW1	An optional external capacitor may be connected between SW1 and Cb.
16,20,21	PGnd	**Power Ground.** Serves as a separate ground for the MOSFETs. Connect to the power ground plane in the application.
17	Cb	An optional external capacitor may be connected between Cb and SW1.
18,19	PV_{IN}	**Power input voltage.** Input for the MOSFETs.

Block diagram

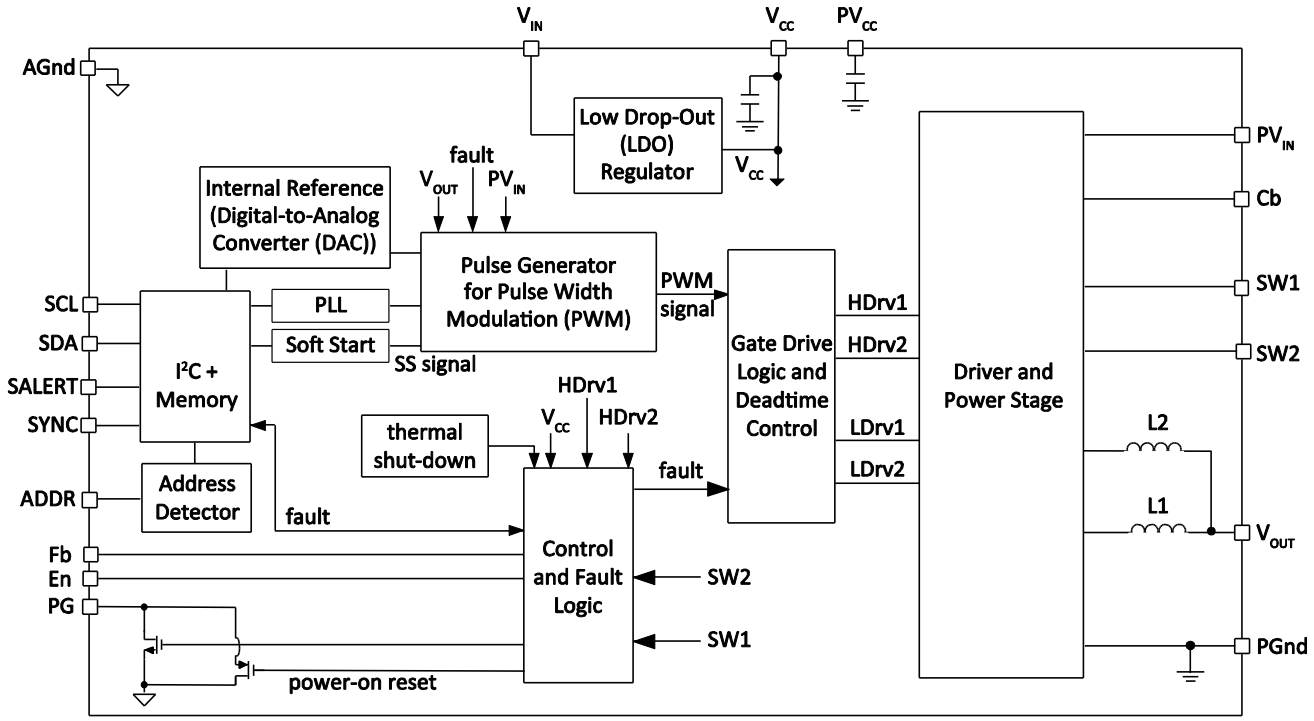


Figure 3 FS1412 µPOL™

Typical application

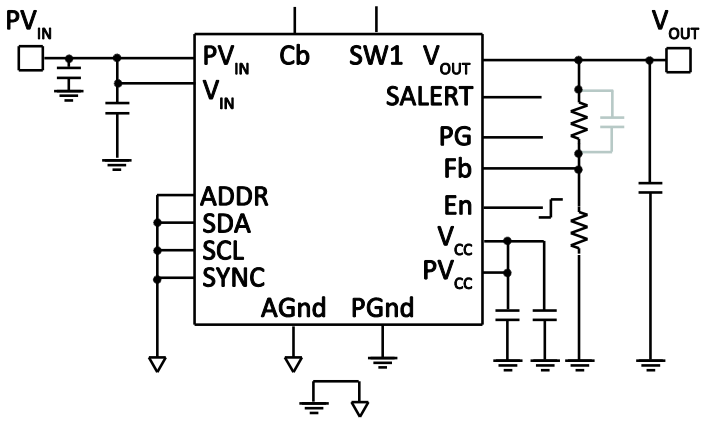


Figure 4 Applications circuit for using an external resistor to set the output voltage

Absolute maximum ratings

Warning: Stresses beyond those shown may cause permanent damage to the FS1412.

Note: Functional operation of the FS1412 is not implied under these or any other conditions beyond those stated in the FS1412 specification.

Reference	Range
PV_{IN}, V_{IN}, En to PGnd, Cb to SW1	-0.3V to 18V
V_{CC} to PGnd (Note 1)	-0.3V to 6V
SW1, SW2	-0.3V to 15V
Fb, Sync, Addr, SCL, SDA, SALERT to AGnd (Note1)	-0.3V to V_{CC}
PG to AGnd (Note 1)	-0.3V to V_{CC}
PGnd to AGnd	-0.3V to +0.3V
ESD Classification (HBM JESD22-A114)	Class 1C
Moisture Sensitivity Level	MSL 3 (per JEDEC J-STD-020D)

Thermal Information	Range
Junction-to-Ambient Thermal Resistance Θ_{JA}	20.5°C/W
Junction to PCB Thermal Resistance $\Theta_{J\text{-}PCB}$	5.5°C/W
Storage Temperature Range	-55°C to 150°C
Junction Temperature Range	-40°C to 150°C
Note: Θ_{JA} : FS1412 evaluation board and JEDEC specifications JESD 51-2A $\Theta_{J\text{-}c\ (bottom)}$: JEDEC specification JESD 51-8	

Order information

Package details

The FS1412 uses a µPOL™ 5.8mm x 4.9mm package delivered in tape-and-reel format, with either 250 or 3900 devices on a reel.

Part Number	V_{OUT}	Quantity per Reel	Package Description	Package Code
FS1412-0600-AS	0.60	250	22-pin LGA SiP (5.8mm x 4.9mm)	P24
FS1412-0600-AL	0.60	3900	22-pin LGA SiP (5.8mm x 4.9mm)	P24

For more information on the tape-and-reel specification, go to:

https://product.tdk.com/en/products/power/switching-power/micro-pol/designtool.html

Recommended operating conditions

Definition	Symbol	Min	Max	Units
Input Voltage Range with External V_{CC} (Note 3, Note 5)	PV_{IN}	6*V_{OUT}	16	V
Input Voltage Range with Internal LDO (Note 4, Note 5)	PV_{IN}	6*V_{OUT}	16	
Bias Input Voltage Range (Note 4)	V_{IN}	4.5	16	
Supply Voltage Range (Note 2)	V_{CC}	4.5	5.5	
Output Voltage Range	V_{OUT}	0.6	1.8	
Continuous Output Current Range	I_O	0	12	A
Operating Junction Temperature	T_J	-40	125	°C

Electrical characteristics

ELECTRICAL CHARACTERISTICS						
Unless otherwise stated, these specifications apply over: 6*V_{OUT} <PV_{IN} <16V, 4.5V < V_{IN} < 16V, 0°C < T < 125°C **Typical values are specified at T_A = 25°C**						
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Supply Current						
V_{IN} Supply Current (Standby)	$I_{IN\ (STANDBY)}$	Enable low		7	8	mA
V_{IN} Supply Current (Dynamic)	$I_{IN\ (DYN)}$	En high, V_{IN} = 12V, F_{SW} =470kHz		16	18	
Soft-Start						
Soft-Start Rate	SS_{RATE}	Default (Note 7), V_{OUT} = 0.6V, T_{ON_RISE}=2ms	0.17	0.28	0.37	V/ms
Output Voltage						
Output Voltage Range	V_{OUT} (default)			0.6		V
	range		0.6		1.8	V
	Resolution			5		mV
Accuracy		T_J = 25°C, V_{OUT} = 0.6V		±0.75		%
		-40°C < T_J < 125°C (Note 6)	-1		+1	
On-Time Timer Control						
On Time	T_{ON}	PV_{IN} = 12V, V_{OUT} = 0.6V, F_{SW} = 470kHz	185	211	235	ns
Minimum On-Time	$T_{ON(MIN)}$	(Note 7)		50		
Internal Low Drop-Out (LDO) Regulator						
LDO Regulator Output Voltage	V_{CC}	5.5V ≤ V_{IN} ≤ 16V, 0 – 40mA	4.89	5.2	5.4	V
		4.5V ≤ V_{IN} < 5.5V, 0 – 40mA	4.19	4.26		
Load Regulation	V_{LD}	0 – 40mA			0.19	
Thermal Shut-Down						
Thermal Shut-Down	Default	(Note 7)		145		°C
Hysteresis		(Note 7)		25		

ELECTRICAL CHARACTERISTICS						
Unless otherwise stated, these specifications apply over: 6*V_{OUT} <PV_{IN} <16V, 4.5V < V_{IN} < 16V, 0°C < T < 125°C Typical values are specified at T_A = 25°C						
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Under-Voltage Lock-Out						
V_{CC} Start Threshold	$V_{CC\_UVLO(START)}$	V_{CC} Rising Trip Level	4.0	4.2	4.4	V
V_{CC} Stop Threshold	$V_{CC\_UVLO(STOP)}$	V_{CC} Falling Trip Level	3.6	3.8	4.1	
Enable Threshold	$En_{(HIGH)}$	Ramping Up	1.05	1.20	1.34	
	$En_{(LOW)}$	Ramping Down	0.92	1.00	1.11	
Input Impedance	R_{EN}		500	1000	1500	kΩ
Current Limit						
Current Limit Threshold	I_{OC} (default)	T_J = 25°C	14.5	16	17.5	A
	I_{OC} (range)		10		16	
Hiccup Blanking Time	$T_{BLK(HICCUP)}$			20		ms
Over-Voltage Protection						
Output Over-Voltage Protection Threshold	V_{OVP} (default)	OVP Detect (Note 7)	115	120	125	Fb%
	V_{OVP} (range)		105		120	
	V_{OVP} (resolution)			5		
Output Over-voltage Protection Delay	T_{OVPDEL}			5		µs
Power Good (PG)						
Power Good Upper Threshold	$V_{PG(UPPER)}$ (default)	V_{OUT} Rising	85	90	95	Fb%
Power Good Hysteresis	$V_{PG(LOWER)}$	V_{OUT} Falling		7		
Power Good Sink Current	I_{PG}	PG = 0.5V, En = 2V		9		mA
Telemetry						
Input voltage reporting accuracy	PV_{IN}_report_err	PV_{IN}=12V, -40°C < T_J < 125°C	-2		2	%
		5V<PV_{IN}<16V, -40°C < T_J <125°C	-5		5	
Output voltage reporting accuracy	V_{OUT}_report_err	V_{OUT} = V_{FB} =0.6V, -40°C < T_J < 125°C	-18		18	mV
Temperature reporting accuracy	T_report_err	-40°C < T_J <125°C (Note 7)	-20		20	°C

ELECTRICAL CHARACTERISTICS							
Unless otherwise stated, these specifications apply over: 6*V_{OUT} < PV_{IN} = V_{IN} < 16V, 0°C < T < 125°C Typical values are specified at T_A = 25°C							
Parameter	**Symbol**	**Conditions**	**Fast-mode**		**Fast-mode Plus**		**Unit**
I^2C parameters		**(Note 7 for all parameters)**	**Min**	**Max**	**Min**	**Max**	
I^2C bus voltage	V_{BUS}		1.8	5.5	1.8	5.5	V
LOW-level input voltage	V_{IL}		−0.5	$0.3V_{BUS}$	−0.5	$0.3V_{BUS}$	
HIGH-level input voltage	V_{IH}		$0.7V_{BUS}$		$0.7V_{BUS}$		
Hysteresis	V_{HYS}		$0.05V_{BUS}$		$0.05V_{BUS}$		
LOW-level output voltage 1	V_{OL1}	(open-drain or open-collector) at 3mA sink current; V_{DD} > 2 V,	0	0.4	0	0.4	V

ELECTRICAL CHARACTERISTICS							
Unless otherwise stated, these specifications apply over: 6*V_{OUT} < PV_{IN} = V_{IN} < 16V, 0°C < T < 125°C Typical values are specified at T_A = 25°C							
Parameter	**Symbol**	**Conditions**	**Fast-mode**		**Fast-mode Plus**		**Unit**
I^2C parameters		**(Note 7 for all parameters)**	**Min**	**Max**	**Min**	**Max**	
LOW-level output voltage 2	V_{OL2}	(open-drain or open-collector) at 2mA sink current; V_{DD} ≤ 2 V,	0	0.2V_{BUS}	0	0.2V_{BUS}	
LOW-level output current	I_{OL}	V_{OL} = 0.4 V,	3	-	3	-	mA
		V_{OL} = 0.6 V	6	-	6	-	
Output fall time	T_{OF}	From V_{IHmin} to V_{ILmax}	20 × (V_{BUS}/5.5 V)	250	20 × (V_{BUS}/5.5 V)	125	ns
Pulse width of spikes that must be suppressed by the input filter	T_{SP}		0	50	0	50	ns
Input current each I/O pin	I_I		−10	10	−10	10	µA
Capacitance for each I/O pin	C_I		-	10	-	10	pF
SCL clock frequency	F_{SCL}		0	400	0	1000	kHz
Hold time (repeated) START condition	$T_{HD;STA}$	After this time, the first clock pulse is generated	0.6	-	0.26	-	µs
LOW period of the SCL clock	T_{LOW}		1.3	-	0.5	-	
HIGH period of the SCL clock	T_{HIGH}		0.6	-	0.26	-	
Set-up time for a repeated START condition	$T_{SU;STA}$		0.6	-	0.26	-	
Data hold time	$T_{HD;DAT}$	I^2C-bus devices	0	-	0	-	
Data set-up time	$T_{SU;DAT}$		100	-	50	-	ns
Rise time of SDA and SCL signals	T_R		20	300	-	120	
Fall time of SDA and SCL signals	T_F		20 × (V_{DD}/5.5 V)	300	20 × (V_{DD}/5.5 V)	120	
Set-up time for STOP condition	$T_{SU;STO}$		0.6	-	0.26	-	µs
Bus free time between a STOP and START condition	T_{BUF}		1.3	-	0.5	-	
Capacitive load for each bus line	C_{BUS}		-	400	-	550	pF
Data valid time	$T_{VD;DAT}$		-	0.9	-	0.45	µs
Data valid acknowledge time	$T_{VD;ACK}$		-	0.9	-	0.45	
Noise margin at the LOW level	V_{NL}	For each connected device, including hysteresis	0.1V_{DD}	-	0.1V_{DD}	-	V
Noise margin at the HIGH level	V_{NH}		0.2V_{DD}	-	0.2V_{DD}	-	
SDA timeout	T_{TO}		200		200		µs

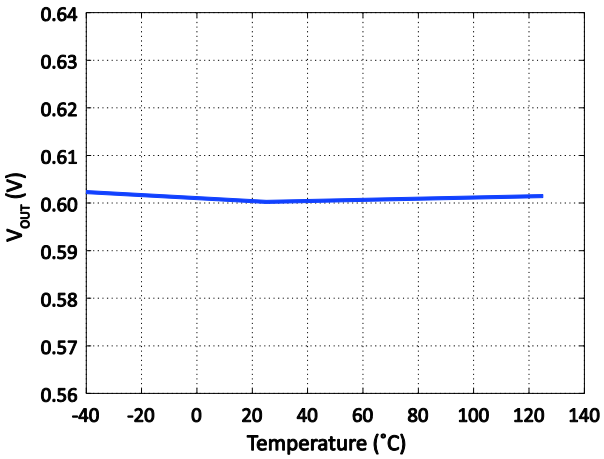
For supported PMBus™ commands, see page 37.

Notes

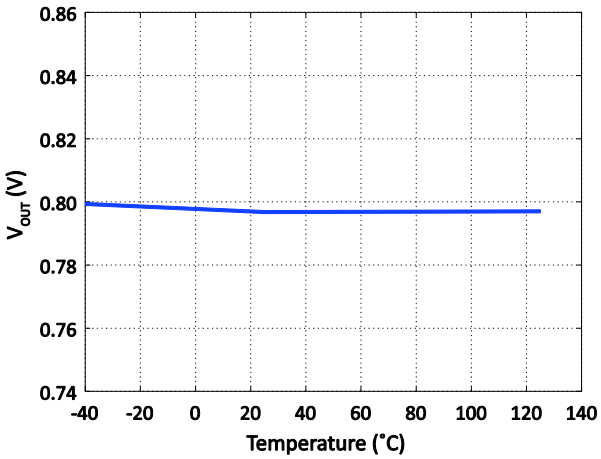
1 PGnd pin and AGnd pin are connected together
2 Must not exceed 6V
3 V_{IN} is connected to V_{CC} to bypass the internal Low Drop-Out (LDO) regulator
4 V_{IN} is connected to PV_{IN} (for single-rail applications with PV_{IN}=V_{IN}=4.5V–16V)
5 Maximum switch node voltage should not exceed 15V
6 Hot and cold temperature performance is assured by correlation using statistical quality control, but not tested in production; performance at 25°C is tested and guaranteed in production environment
7 Guaranteed by design but not tested in production

Temperature characteristics

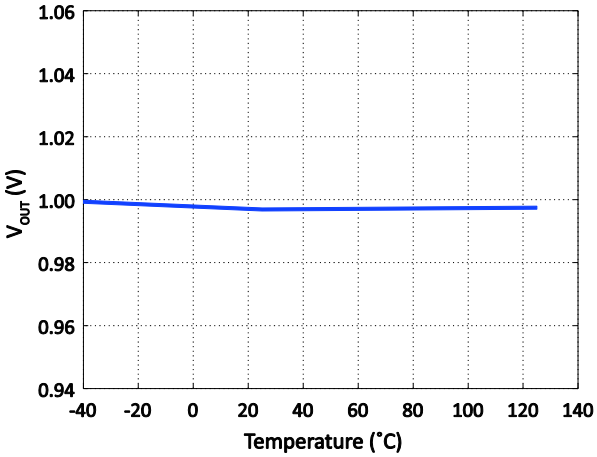
Output Voltage: 0.6V



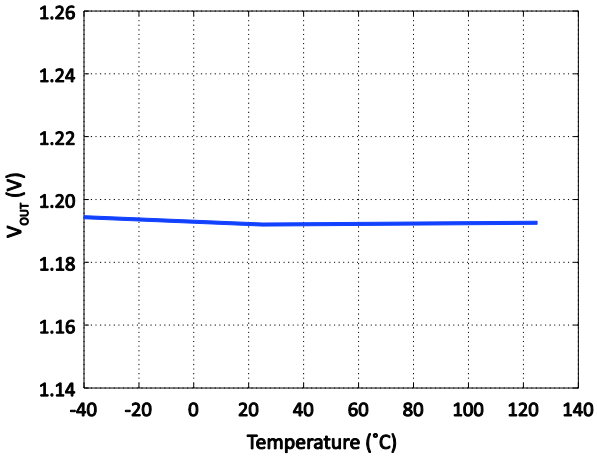
Output Voltage: 0.8V



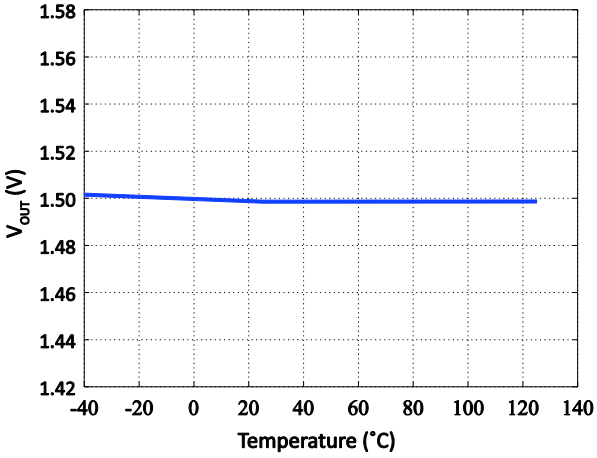
Output Voltage: 1.0V



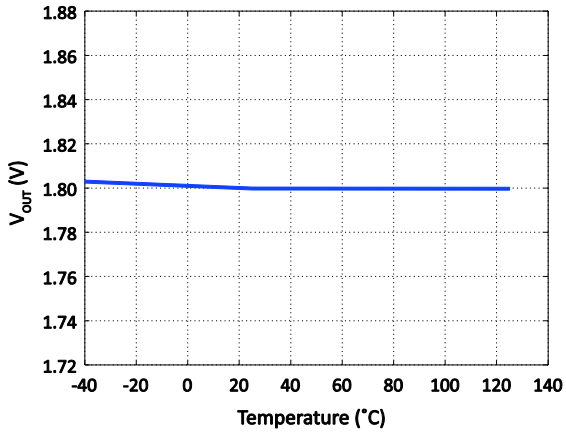
Output Voltage: 1.2V



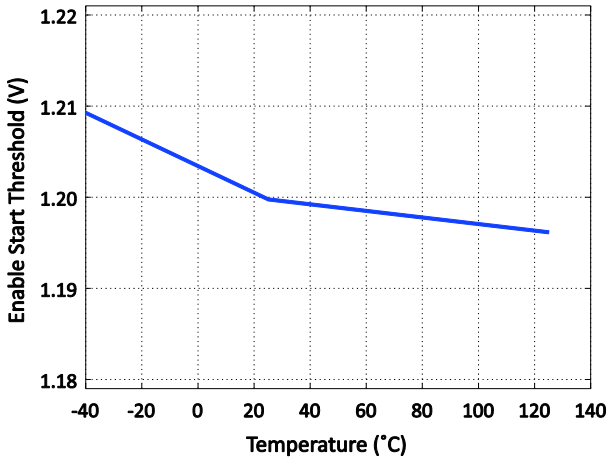
Output Voltage: 1.5V



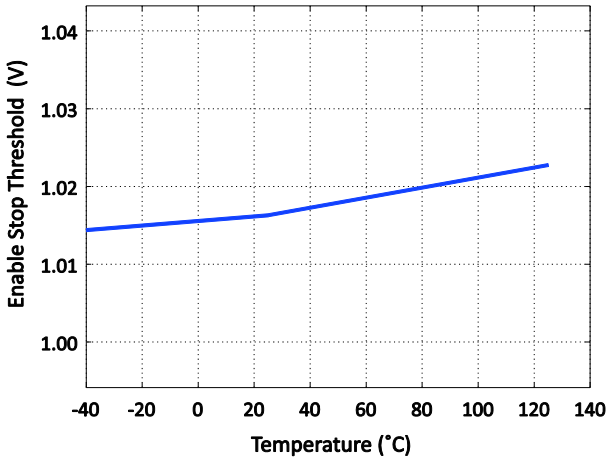
Output Voltage: 1.8V



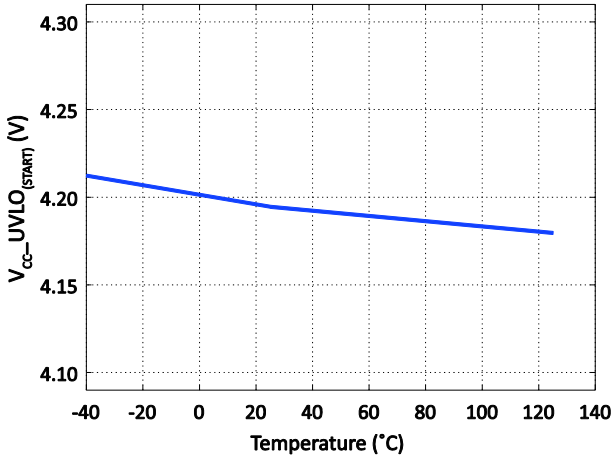
Enable Start Threshold



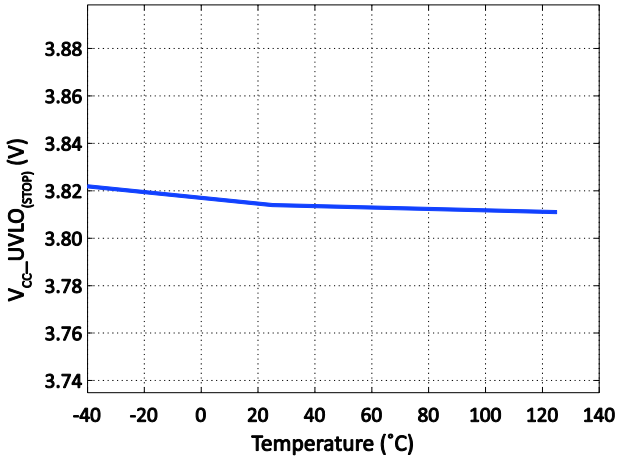
Enable Stop Threshold



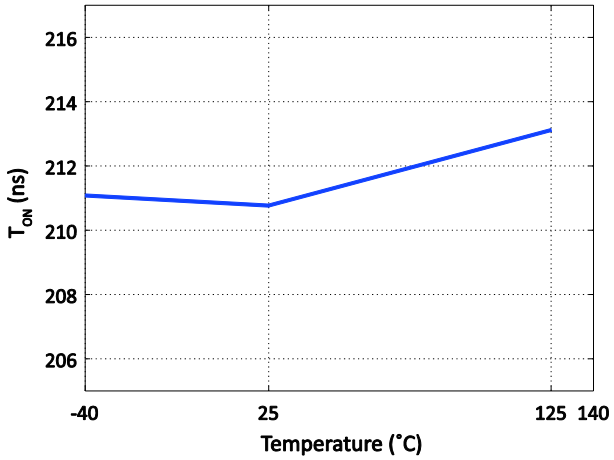
V_{CC} Start Threshold



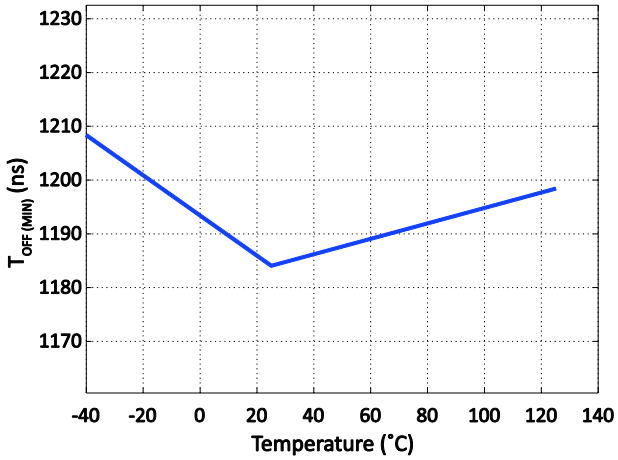
V_{CC} Stop Threshold



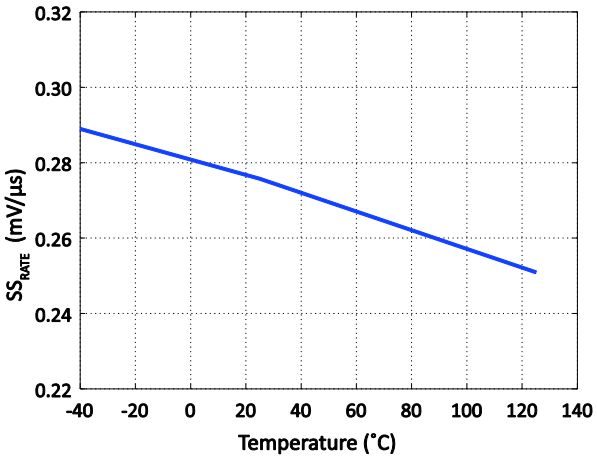
On Time



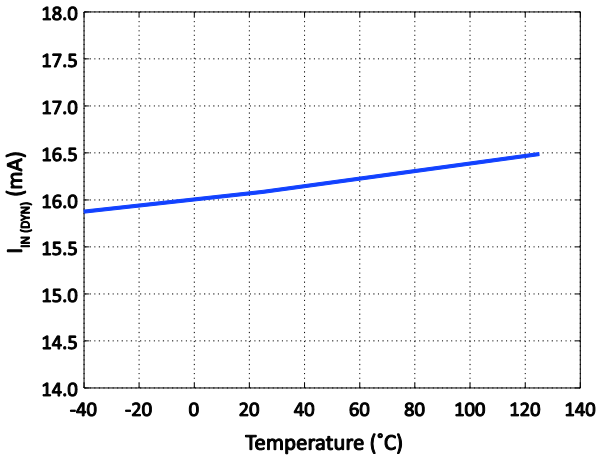
Off Time



Soft-Start Rate



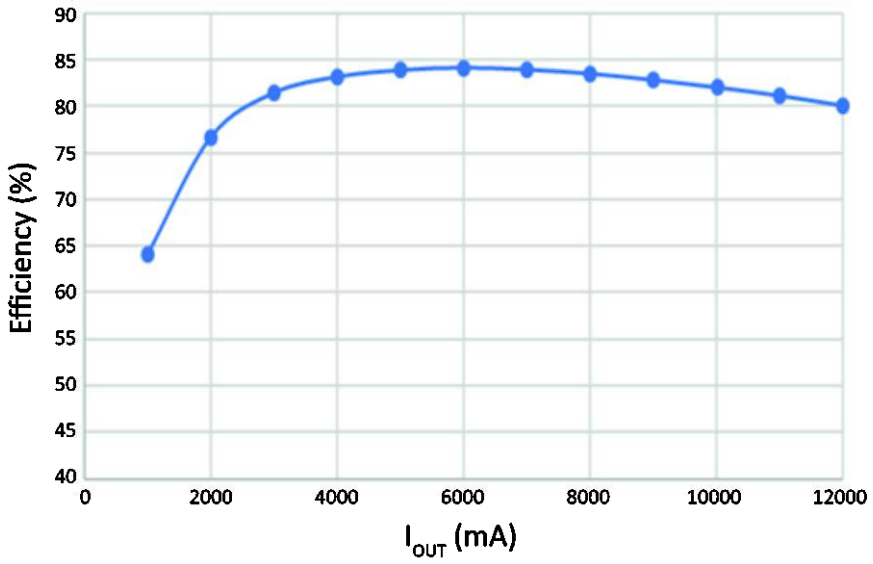
V_{IN} Supply Current (Dynamic)



Efficiency characteristics

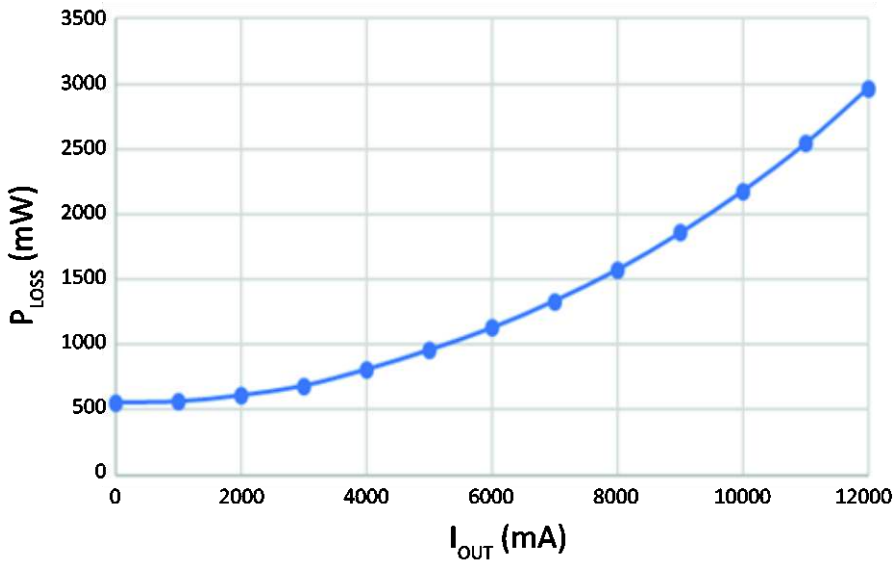
Typical efficiency

PV_{IN} = 12V,V_{OUT} = 1V, I_O = 0–12A, room temperature, no air flow, all losses included



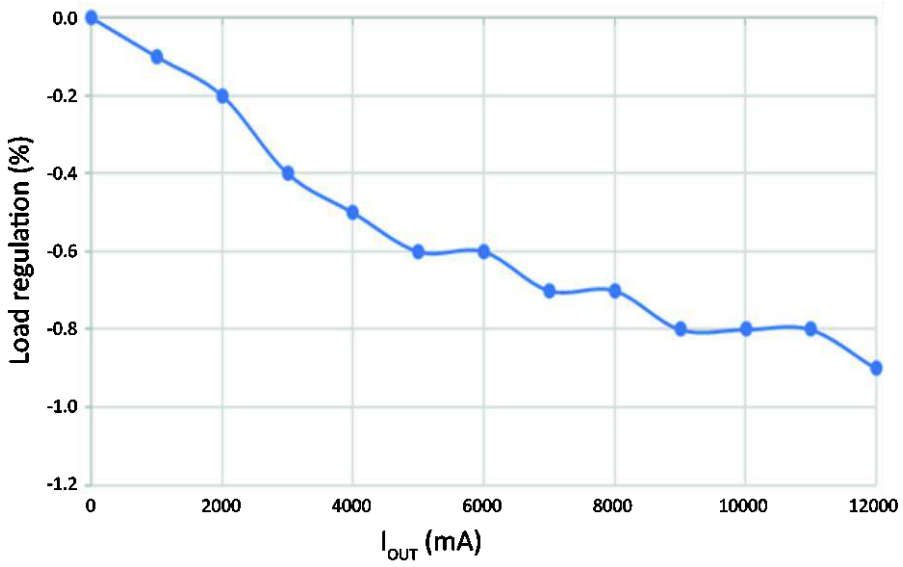
Typical power loss

PV_{IN} = 12V,V_{OUT} = 1V, I_O = 0–12A, room temperature, no air flow, all losses included



Typical load regulation

PV_{IN} = 12V,V_{OUT} = 1V, I_O = 0–12A, room temperature, no air flow, all losses included



Applications information

Overview

The FS1412 is an easy-to-use, fully integrated and highly efficient DC/DC regulator. Aspects of its operation, including output voltage and system optimization parameters, can be programmed using the I²C/PMBus™ protocol. It uses a proprietary modulator to deliver fast transient responses. The modulator has internal stability compensation so that it can be used in a wide range of applications, with various types of output capacitors, without loop stability issues.

The FS1412 is a versatile device offering great flexibility for configuration and system monitoring using the I²C/PMBus™ interface. At the same time, it allows standalone operation without any digital interface by making it easy for the designer to configure output voltages using simple resistor divider changes, and to monitor the system using the Power Good output.

Operation and topology

The FS1412 uses an interleaved buck converter topology. It shows reduced voltage stresses on the internal power devices, resulting in smaller size and switching losses comparable to an equivalently rated conventional interleaved buck converter. Another advantage is a natural current-sharing mechanism between the two phases.

Bias voltage

The FS1412 has an integrated Low Drop-Out (LDO) regulator, providing the DC bias voltage for the internal circuitry. The typical LDO regulator output voltage is 5.2V. For internally biased single-rail operation, the V_{IN} pin should be connected to the PV_{IN} pin (Figure 5). If an external bias voltage is used, the V_{IN} pin should be connected to the V_{CC} pin to bypass the internal LDO regulator (Figure 6). There is a separate pin to provide bias for the drivers (PV_{CC}); this should be connected to V_{CC} in the application circuit.

The supply voltage (internal or external) rises with V_{IN} and does not need to be enabled using the En pin. Consequently, I²C/PMBus™ communication can begin as soon as:

- V_{CC}_UVLO start threshold is exceeded
- Memory contents are loaded
- Initialization is complete
- Address offset is read

Note: Until initialization is complete, a small leakage current (≈3.4µA) will flow from the device into the output. This may significantly pre-bias the output voltage in applications with long V_{IN}/V_{CC} rise times. To prevent this, a small load capable of sinking 3.4µA should be connected in such applications.

The I²C bus may be pulled up either to V_{CC} or to a system I²C bus voltage. The FS1412 offers two ranges for the I²C bus voltage, defined by the user register bit **Bus_voltage_sel**.

Register	Bits	Name/Description
0x7A	[2]	**Bus_voltage_sel** 0:1.8–2.5V, 1: 3.3–5V

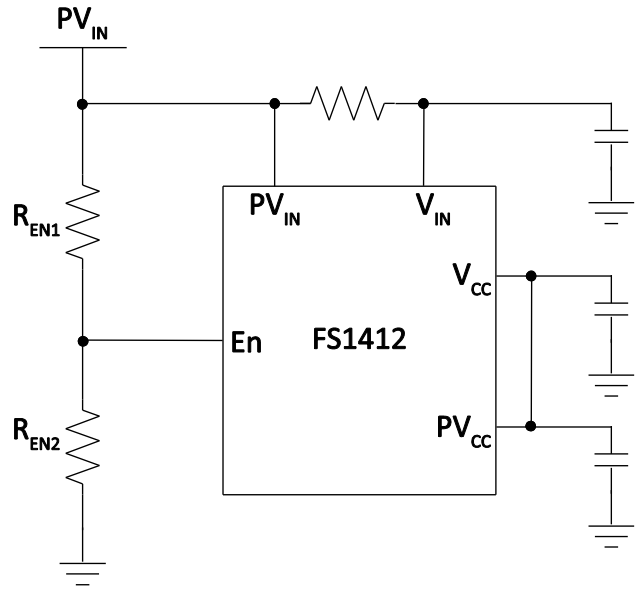


Figure 5 Single supply configuration: internal LDO regulator, adjustable PV_{IN}_UVLO

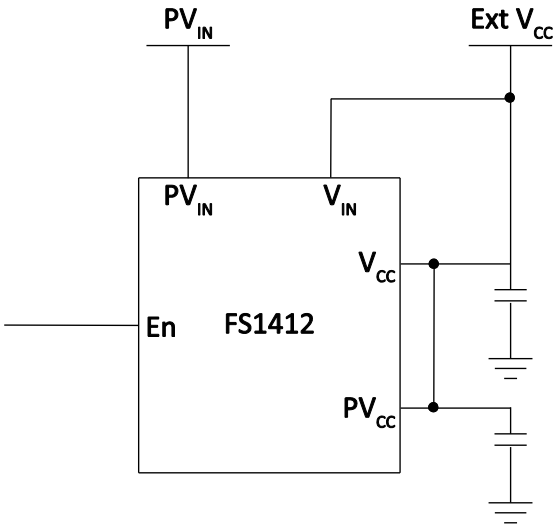


Figure 6 Using an external bias voltage

I²C base address and offsets

The FS1412 has user registers to set its I²C base address and PMBus™ base address. The default I²C base address is 0x08, and the default PMBus™ base address is 0x70. An offset of 0–15 is then defined by connecting the ADDR pin to the AGnd pin, either directly or through a resistor. An address detector reads the resistance of the connection at startup and uses it to set the offset, which is added to the base I²C address to set the address at which the I²C master device will communicate with the FS1412. The same offset is added to the base PMBus™ address to determine the PMBus™ address at which PMBus™ communication will be established.

To select offsets of 0–15, connect the pins as follows:

- **0** – 0Ω (short ADDR to AGnd)
- **+1** – 1.13kΩ
- **+2** – 1.87kΩ
- **+3** – 2.61kΩ
- **+4** – 3.4kΩ
- **+5** – 4.12kΩ
- **+6** – 4.87kΩ
- **+7** – 5.62kΩ
- **+8** – 6.34kΩ
- **+9** – 7.15kΩ
- **+10** – 7.87kΩ
- **+11** – 8.66kΩ
- **+12** – 9.31kΩ
- **+13** – 10.2kΩ
- **+14** – 11kΩ
- **+15** – 12.1kΩ

Note: Do not use the 7-bit address 0x0C; this corresponds to the Alert Response Address in the SMBus™ protocol.

Soft-start and target output voltage

The FS1412 has an internal digital soft-start circuit to control output voltage rise-time and limit current surge at start-up. When V_{CC} exceeds its start threshold (V_{CC}_UVLO$_{(START)}$), the FS1412 exits reset mode; this initiates loading of the contents of the non-volatile memory into the working registers and calculates the address offset as described above.

Once initialization is complete, the internal soft start begins to ramp towards the set reference voltage at a rate determined by the TON_RISE registers (corresponding to the TON_RISE command), provided these conditions are met:

a) A valid enable signal is recognized (as defined by the Enable pin, Operation register, ON_OFF_CONFIG register, input voltage PV_{IN}, and PV_{IN} UVLO threshold corresponding to the VIN_ON registers).

b) The internal pre-charge circuit has ensured that, when the device starts to switch, it does so with balanced PV_{IN}/2 voltages across all FETs.

During initial start-up, the FS1412 operates with a minimum of high-drive (HDrv) pulses until the output voltage increases (see Switching frequency and minimum values for on-time, off-time on page 19). On-time is increased until V_{OUT} reaches the target value defined by the VOUT_COMMAND registers. For proper start-up operation of the FS1412, fitting a 100Ω resistor in parallel with the output capacitors (C_{OUT}) is recommended. A minimum wait time of 600*C_{OUT} is recommended between successive power or Enable cycling operations. For example, with the recommended 100Ω resistor across four 47µF output capacitors, a new Enable assertion should not happen for a minimum of 78ms after disabling the FS1412.

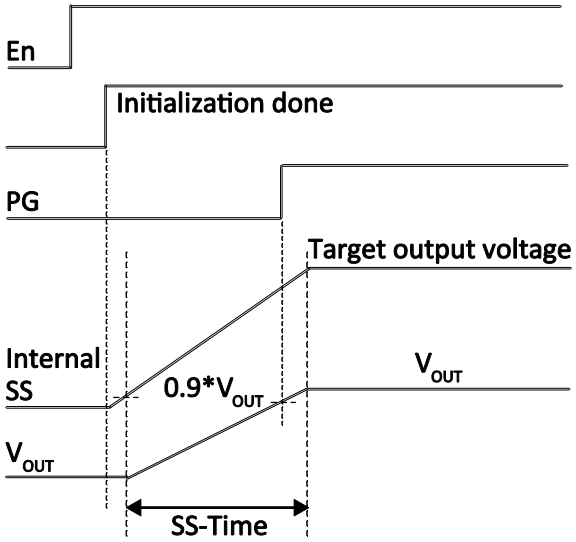


Figure 7 Theoretical operational waveforms during soft-start

Over-current protection (OCP) and over-voltage protection (OVP) are enabled during soft-start to protect the FS1412 from short circuits and excess voltages respectively.

A resistor divider may be used with a standard FS1412-0600 device to set the desired output voltage (Figure 8). This gives system designers the flexibility to design all the power rails in the system across the entire output voltage range (0.6–1.8V) using a single part.

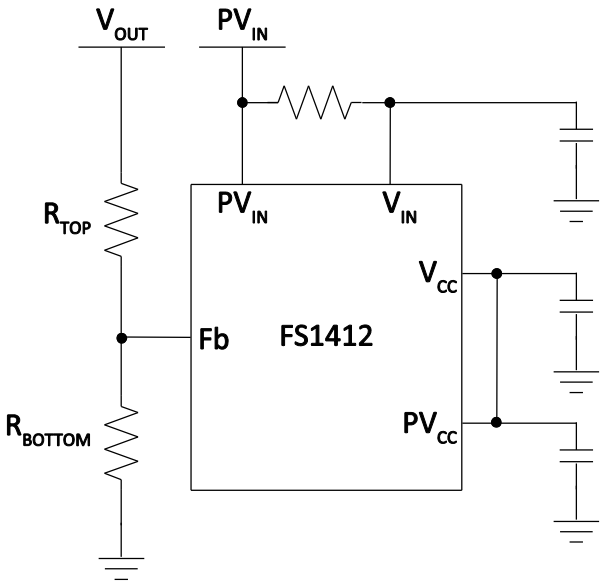


Figure 8 Setting the output voltage with an external resistor divider

The equation below describes the appropriate resistor divider selection to set the output voltage using a FS1412 programmed to 0.6V.

$$R_{BOTTOM} = \frac{R_{TOP}}{1.7975V_o - 1.0639 - 0.00894R_{TOP}}$$

where, R_{TOP} and R_{BOT} are in kΩ. It is recommended that system designers place a capacitor (C_{FF} in Figure 18) of 47pF to 470pF in parallel with R_{TOP}, for which a value of 4.12kΩ is recommended. The recommended value for R_{BOTTOM} depends on the output voltage, as shown in the table below. It is also recommended that designers validate these values in their own applications.

V_{OUT} (V)	R_{BOTTOM} (kΩ)
0.72V	21
0.85V	9.76
0.9V	8.06
0.95V	6.81
1V	5.9
1.05V	5.23
1.1V	4.75
1.2V	3.92
1.5V	2.55
1.8V	1.91

Instead of an external resistor divider, the output voltage can be set using I²C/PMBus™ commands (see page 24) or the corresponding user registers. The table below lists VOUT_COMMAND codes to set the voltages shown above. FS1412 supports this command with a resolution of 1/256V.

V_{OUT} (V)	VOUT_COMMAND	V_{OUT} (V)	VOUT_COMMAND
0.65	00A7	1.20	0134
0.70	00B4	1.25	0140
0.72	00B9	1.25	014D
0.75	00C0	1.30	015A
0.78	00C8	1.35	0167
0.80	00CD	1.40	0174
0.85	00DA	1.45	0127
0.88	00E2	1.50	0180
0.90	00E7	1.55	018D
0.95	00F4	1.60	019A
1.00	0100	1.65	01A7
1.05	010D	1.70	01B4
1.10	011A	1.75	01C0
1.15	0127	1.80	01CD

Shut-down mechanisms

The FS1412 has two shut-down mechanisms:

- *Hard shut-down or decay according to load*
  A valid hard-disable is recognized (as defined by the Enable pin, Operation register, ON_OFF_CONFIG register, input voltage PV_{IN},

and PV_{IN} UVLO threshold corresponding to the VIN_ON registers). Both drivers switch off and soft-start is pulled down instantaneously.

- *Soft-Stop or controlled ramp down*
  A valid soft-off request is recognized (as defined by the Enable pin, Operation register and ON_OFF_CONFIG register). Then, following a delay corresponding to the TOFF_DELAY registers, the SS signal falls to 0 in a time defined by the TOFF_FALL registers; the drivers are disabled only when it reaches 0. The output voltage follows the SS signal down to 0.

By default, the device is configured for hard shut-down. Shut-down with PV_{IN} is always a hard shut-down.

Switching frequency and minimum values for on-time, off-time and PV_{IN}

The switching frequency of the FS1412 depends on the output voltage. There are two possible modes of operation:

a) Pseudo constant-frequency COT mode (default)

b) PLL-modulated COT mode

For the default output voltage of 0.6V, the switching frequency is nominally 470kHz, and the device operates in mode a). In this mode, when the output voltage is set using an external resistor divider, the switching frequency automatically adjusts to the appropriate value:

$$F_{sw} = 470kHz \times \frac{V_{OUT}}{0.6}$$

When output voltage is set by programming the VOUT_COMMAND user registers, rather than using an external resistor divider, mode b) should be used. To do this, the user must also enable the PLL (phase-locked loop), which is disabled by default, and cycle the Enable pin. This automatically sets the switching frequency to factory-programmed values shown in the table below. The PLL modulates the on-time to maintain a constant switching frequency irrespective of the load.

V_{OUT} range (V)	F_{SW} (MHz)
$V_{OUT} < 0.65$	0.50
$0.65 < V_{OUT} < 1.10$	1.00
$1.10 < V_{OUT} < 1.32$	1.25
$1.32 < V_{OUT} < 1.80$	1.50

Therefore, with either method, system designers need not concern themselves with selecting the switching frequency and have one fewer design task to manage.

When input voltage is high relative to target output voltage, the Control MOSFETs are switched on for shorter periods. The shortest period for which it can reliably be switched on is defined by minimum on-time ($T_{ON(MIN)}$). During start-up, when the output voltage is very small, the FS1412 operates with minimum on-time.

The maximum conversion ratio, on the other hand, is determined by two factors:

a) When input voltage is low relative to target output voltage, the Control MOSFET is switched on for longer periods. The shortest period for which it can be switched off is defined by minimum off-time ($T_{OFF(MIN)}$). The Synchronous MOSFET stays on during this period and its current is detected for over-current protection. This dictates the minimum input voltage that can still allow the device to regulate its output at the target voltage.

b) To maintain balanced switching amplitudes in both phases, this topology requires there to be no overlap between the high sides of the two phases (unlike a conventional buck topology). This effectively imposes theoretical maximums of 50% on the duty cycle of each phase and 25% on the conversion ratio; in practice, allowing for circuit delays and dead-times, the conversion ratio must not exceed 16% at full load.

The maximum conversion ratio is affected by both system efficiency and load transient requirements. It is recommended that system designers validate the values in their own applications.

Enable (En) pin

The Enable (En) pin has several functions:

- In the default setting of the ON_OFF_CONFIG command, it is used to switch the FS1412 on and off. It has a precise threshold, which is internally monitored by the UVLO circuit. If it is left floating, an internal 1MΩ resistor pulls it down to prevent the FS1412 being switched on unintentionally.
- It can be used to implement a precise input voltage UVLO. The input of the En pin is derived from the PV_{IN} voltage by a set of resistive dividers, R_{EN1} and R_{EN2} (Figure 5). Users can program the UVLO threshold voltage by selecting different ratios. A useful feature that stops the FS1412 regulating when PV_{IN} is lower than the desired voltage, this may be used for finer control over the PV_{IN} UVLO voltage levels than is provided by the VIN_ON/VIN_OFF commands.
- It can be used to monitor other rails for a specific power sequencing scheme (Figure 9).

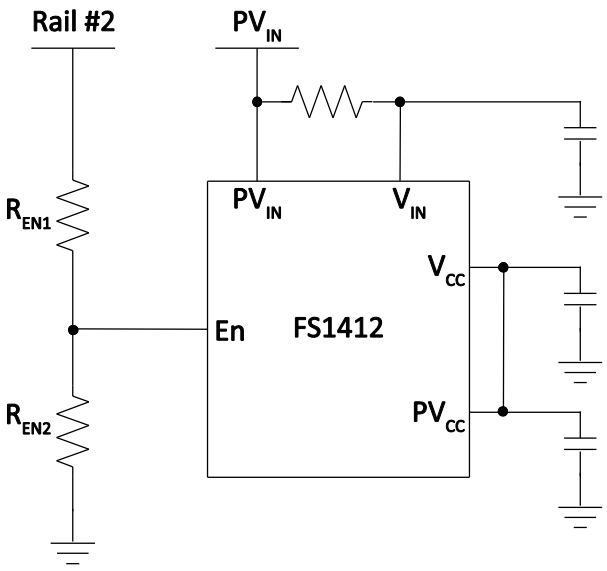


Figure 9 En pin used to monitor other rails for sequencing purposes

Over-current protection (OCP)

Over-current protection (OCP) is provided by sensing the current through the $R_{DS(on)}$ of the Synchronous MOSFET. When this current exceeds the OCP threshold, a fault condition is generated. This method provides several benefits:

- Provides accurate over-current protection without reducing converter efficiency (the current sensing is lossless)
- Reduces cost by eliminating a current-sense resistor
- Reduces any layout-related noise issues.

The OCP threshold is defined by the IOUT_OC_FAULT_LIMIT command (or the corresponding user registers). The over-current limit may be programmed in 0.5A steps, up to a maximum of 16A. The minimum recommended over-current threshold is 10A.

The OCP threshold is internally compensated so that it remains almost constant at different ambient temperatures.

When the current exceeds the OCP threshold, the PG and SS signals are pulled low. The Synchronous MOSFET remains on until the current falls to 0, then the FS1412 enters hiccup mode (Figure 10). Both the Control MOSFET and the Synchronous MOSFET remain off for the hiccup-blanking time. After this time, the FS1412 tries to restart. If an over-current fault is still detected, the preceding actions are repeated. The FS1412 remains in hiccup mode until the over-current fault is remedied. The FS1412 can be re-programmed to enter a latched shut-down mode on encountering an over-current fault.

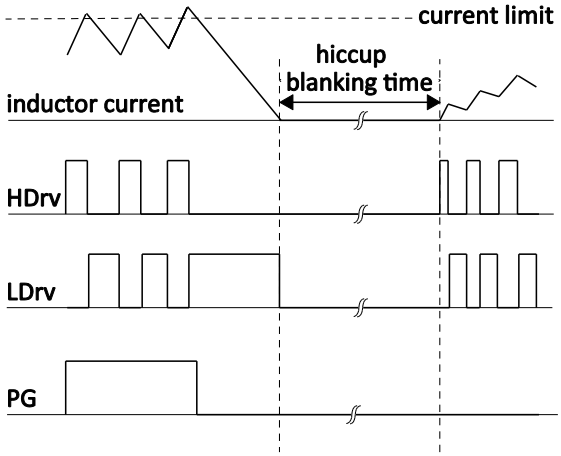


Figure 10 Illustration of OCP in hiccup mode

Over-voltage protection (OVP)

Over-voltage protection (OVP) is provided by sensing the voltage at the FB pin. When FB exceeds the output OVP threshold for longer than the output OVP delay (typically 5µs), a fault condition is generated.

The OVP threshold is defined by the VOUT_OV_FAULT_LIMIT command (or the corresponding user registers). This command allows the over-voltage level to be set relative to the output voltage, with a resolution of 1/256V. However, internally, these are rounded to one of four settings as shown in the table below.

VOUT_OV_FAULT_LIMIT (% of VOUT_COMMAND)	Actual OVP Threshold (% of VOUT_COMMAND)
100 < setting ≤ 105.4	105
105.4 < setting ≤ 110.1	110
110.1 < setting ≤ 114.8	115
114.8 < setting ≤ 100.1	**120**

The default setting is 120%. All the MOSFETs are switched off immediately and the PG pin is pulled low.

The MOSFETs remain latched off until reset by cycling either V_{CC} or En. Figure 11 shows a timing diagram for over-voltage protection.

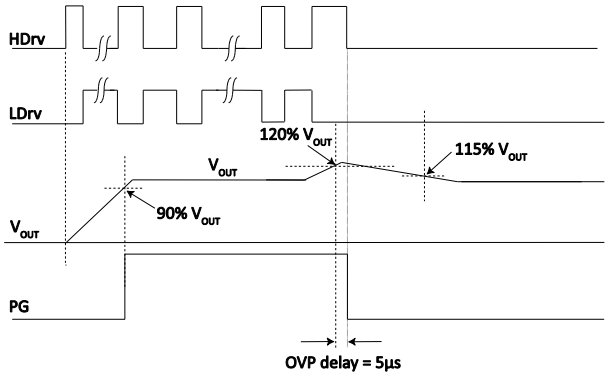


Figure 11 Illustration of latched OVP

The FS1412 provides output over-voltage and under-voltage warnings, as well as output under-voltage fault protection. These are set by three commands, respectively: VOUT_OV_WARN_LIMIT, VOUT_UV_WARN_LIMIT and VOUT_UV_FAULT_LIMIT (or the corresponding user registers). The mechanism for these thresholds is different from the over-voltage protection mechanism: the former rely on a digital comparison of the digitized and processed V_{OUT} telemetry to the thresholds, whereas the latter relies on an all-analog signal path and an internal high-speed comparator.

Over-temperature protection (OTP)

Temperature sensing is provided inside the FS1412. The OTP threshold is defined by the lower of two thresholds:

a) A fixed threshold set internally to 145°C. The comparison with this threshold is analog. If the temperature exceeds the threshold, the device stops switching with all MOSFETs off until the temperature drops below the threshold, after which it restarts automatically.

b) A programmable threshold set to a resolution of 1°C using the OT_FAULT_LIMIT command (or the corresponding user registers). When set lower than the fixed analog threshold (145°C), the programmable threshold determines the temperature at which the device trips, making a digital comparison of reported temperature (READ_TEMPERATURE) and OT_FAULT_LIMIT. When the reported temperature exceeds the programmable threshold, the device either continues power conversion (default) or goes into a latched shutdown, a behavior selected by reprogramming the OT_FAULT_RESPONSE PMBus command (or corresponding registers). Recovery requires either cycling Enable or the Operation command.

By default, the FS1412 relies on the fixed analog threshold with its auto-restart fault response. In this default configuration, the digital threshold is set to 150°C, and the fault response is set to ignore.

Power Good (PG)

Power Good (PG) behavior is defined by the user register bits PGControl **and** by the POWER_GOOD_ON command. When the PGControl bit is set, **t**he PMBus™ command may be used to set the upper power good threshold relative to the output voltage, with a resolution of 1/256V. However, internally, these are rounded to one of four settings as shown in the table below.

POWER_GOOD_ON (% of VOUT_COMMAND)	Actual Power Good Threshold (% of VOUT_COMMAND)
96.1 < threshold ≤ 85.1	80
79.6 < threshold ≤ 85.1	85
85.1 < threshold ≤ 89.8	**90**
89.81 < threshold ≤ 96.1	95

The default is 90%, so the PG signal will be asserted when the voltage at the Fb pin exceeds 90% of the VOUT_COMMAND setting (default 0.6V).

Hysteresis of 5% is applied to this, giving a lower threshold. When the voltage at the Fb pin drops below this lower threshold, the PG signal is pulled low.

PGControl bit set to 1 (default)

Figure 12 shows PG behavior in this situation.

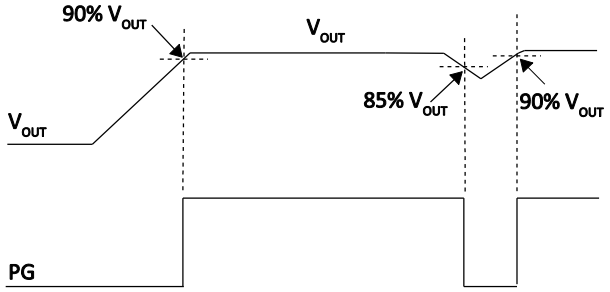


Figure 12 PG signal when PGControl bit=1

The behavior is the same at start-up and during normal operation. The PG signal is asserted when:

- En and V_{CC} are both above their thresholds
- No fault has occurred (including over-current, over-voltage and over-temperature)
- V_{OUT} is within the target range (determined by continuously monitoring whether FB is above the PG threshold)

PGControl bit set to 0

Figure 13 shows PG behavior in this situation.

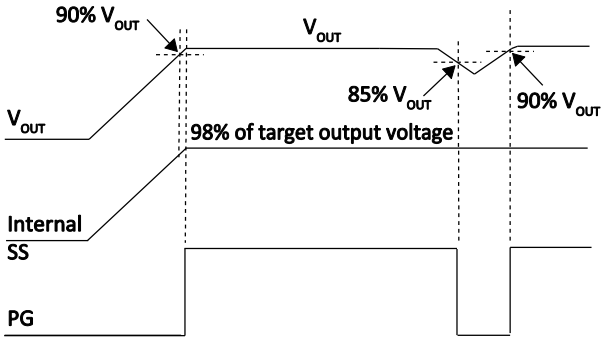


Figure 13 PG signal when PGControl bit=0

In normal operation, the PG signal behaves in the same way as when the **PGControl** bit is 1.

At start-up, however, the PG signal is asserted after Fb is within 2% of target output voltage, not when Fb exceeds the upper PG threshold.

FS1412 also integrates an additional PMOS in parallel to the NMOS internally connected to the PG pin (Figure 3). This PMOS allows the PG signal to stay at logic low, even if V_{CC} is low and the PG pin is pulled up to an external voltage not V_{CC}.

Design example

Let us now consider a simple design example, using the FS1412 for the following design parameters:

- $PV_{IN} = V_{IN} = 12V$
- $V_{OUT} = 1.0V$
- $F_{SW} = 800kHz$
- $C_{OUT} = 4 \times 47\mu F$
- $C_{IN} = 3 \times 22\mu F$
- Ripple Voltage = ± 1% * V_{OUT}
- $\Delta V_{OUT(MAX)}$ = ±3% * V_{OUT}
  (for 50% load transient @ 40A/µs)

Input capacitor

The input capacitor selected for this design must:

- Handle the peak and root mean square (RMS) input currents required by the FS1412
- Have low equivalent series resistance and inductance (ESR and ESL) to reduce input voltage ripple

MLCCs (multi-layer ceramic capacitors) are ideal. Typically, in 0805 case size, they can handle 2A RMS current with less than 5°C temperature rise.

For the FS1412 converter topology operating at duty cycle D and output current I_O, the RMS value of the input current is:

$$I_{RMS} = 0.5 \times Io\sqrt{D(1-D)}$$

In this application, I_O = 12A and $D = \frac{2 \times V_{OUT}}{PV_{IN}} = 0.166$

Therefore, I_{RMS} = 2.23A and we can select three 22µF 25V ceramic capacitors for the input capacitors (C2012X5R1E226M125AC from TDK).

If the FS1412 is not located close to the 12V power supply, a bulk capacitor (68–330µF) may be used in addition to the ceramic capacitors.

For V_{IN}, which is the input to the LDO, it is recommended to use a 1µF capacitor very close to the pin. The V_{IN} pin should be connected to PV_{IN} through a 2.7Ω resistor. Together, the 2.7Ω resistor and 1µF capacitor filter noise on PV_{IN}.

Output voltage and output capacitor

The FS1412 is trimmed at the factory to provide a 0.6V output in closed loop. When not using I2C/PMBus™ and instead employing a resistor divider, as in the application example here, we will choose the resistor values in accordance with the discussion on page 18. Therefore, R_{TOP} = 4.12kΩ, R_{BOTTOM} = 5.9 kΩ and C_{FF} = 220pF.

The design requires minimal output capacitance to meet the target output voltage ripple and target maximum output voltage deviation under load transient conditions.

For the FS1412, the minimum number of output capacitors required to achieve target peak-to-peak V_{OUT} ripple is:

$$N_{MIN} = 5.8 \times \frac{\frac{(1-D)}{8CF_{SW}} + ESR(1-D) + \frac{ESL \times F_{SW} \times (1-D)^2}{D}}{\Delta V_{OUTripple(p-p)}}$$

where:

- N_{MIN} = minimum number of output capacitors
- D = duty cycle
- C = equivalent capacitance of each output capacitor
- F_{SW} = switching frequency
- ESR = equivalent series resistance of each output capacitor
- ESL = equivalent series inductance of each output capacitor
- $\Delta V_{OUTripple(p-p)}$
  = target peak-to-peak V_{OUT} ripple

This design uses C2012X5R0J476M125AC from TDK; this is a 47µF MLCC, 0805 case size, rated at 6.3V. At 1.0V, accounting for DC bias and AC ripple derating, it has an equivalent capacitance of 33µF (C). Equivalent series resistance is 3mΩ (ESR) and equivalent series inductance is 0.44nH (ESL).

Putting these parameters into the equation gives:

N_{MIN} = 2.27

To meet the maximum voltage deviation ΔVo_{max} under a ΔI_o load transient, the minimum required number of output capacitors is:

$$\frac{\mathbf{0.196} \times \Delta \boldsymbol{I_o^2}}{4 \times \Delta V_{omax} \times F_{sw} \times C}$$

where:

- ΔI_o = load step
- ΔV_{OUTmax} = target maximum voltage deviation
- F_{sw} = switching frequency
- C = equivalent capacitance of each output capacitor

Again, using C = 33µF, it can be seen that the minimum number of output capacitors required is 2.22.

In our design intended for space-constrained applications, therefore, we use four C2012X5R0J476M125AC capacitors.

It should be noted here that the calculation for the minimum number of output capacitors under a load transient makes some assumptions:

a) No ESR or ESL

b) Converter can saturate its duty cycle instantly

c) No latency

d) Step load (infinite slew rate)

Assumptions (a), (b) and (c) are liberal, whereas (d) is conservative. Therefore, in a real application, additional capacitance may be required to meet transient requirements and should be carefully considered by the system designer.

It should be noted that even in the absence of a target V_{OUT} ripple or target maximum voltage deviation under load transient, at least one 22µF capacitor is still required in order to ensure stable operation without excessive jitter.

Up to eight 47µF capacitors may be used in the design. If more capacitance is required, it is recommended to use a high value capacitor with relatively high ESR (>3mΩ).

A 100 ohm resistor should be added in parallel with the output capacitors.

Figure 15 to Figure 16 show peak-to-peak voltage deviation as a function of slew rate for different output voltages and load currents.

Figure 17 shows the minimum required output capacitance as a function of the output voltage. For an output voltage of 1V, the minimum capacitor requirement is dictated by the load transient specifications (< ±3% V_{OUT}). For output voltages above 1V, the output voltage ripple specification dominates (< ±1%).

V_{CC} and PV_{CC} capacitor selection

FS1412 uses on-package capacitors for V_{CC} as well as PV_{CC} to ensure effective high-frequency bypassing. However, especially for applications that use an external V_{CC} supply, it is recommended that system designers place 2.2µF/0603/X7R/10V capacitors on the application board as close as possible to the V_{CC} and PV_{CC} pins (Figure 18).

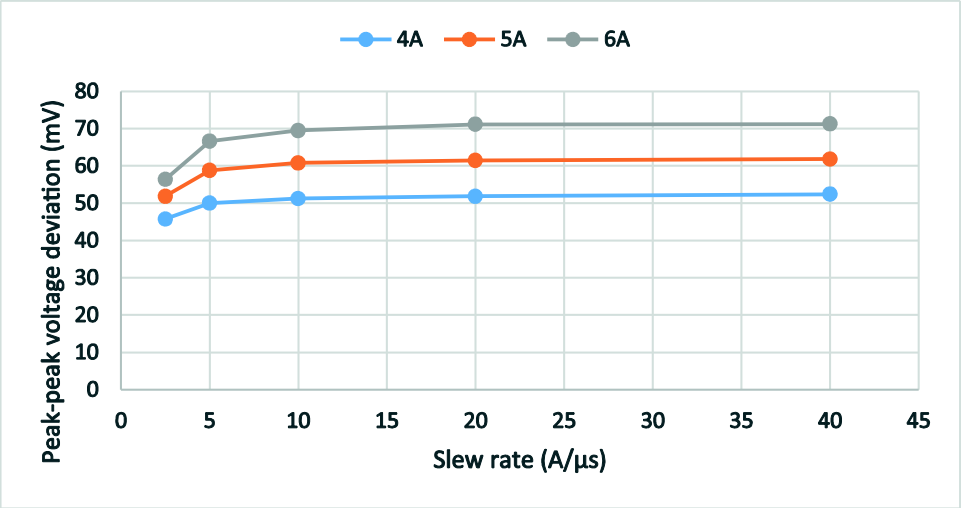


Figure 14 Peak-peak voltage deviation (PV_{IN} = 12V, V_{OUT} = 0.6V, C_{OUT} = 4 x 47 µF)

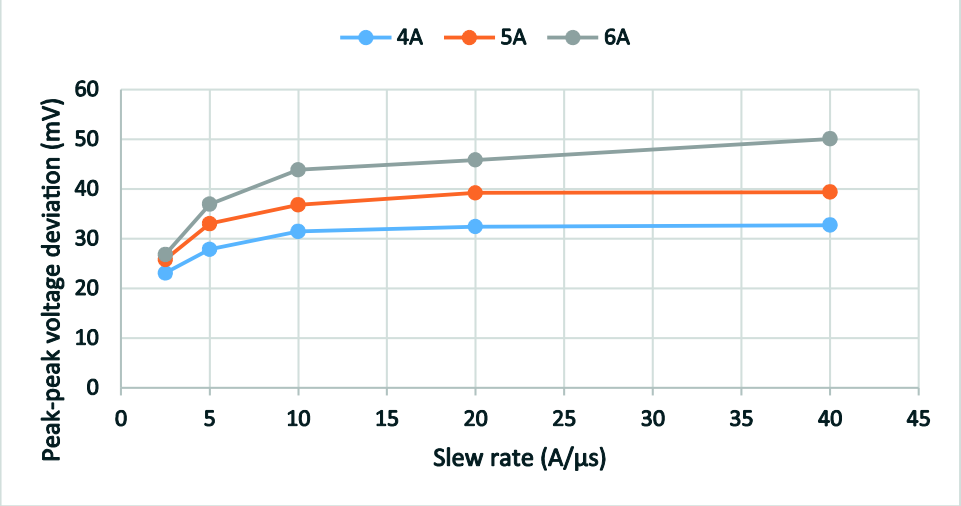


Figure 15 Peak-peak voltage deviation (PV_{IN} = 12V, V_{OUT} = 1.0V, C_{OUT} = 4 x 47 µF)

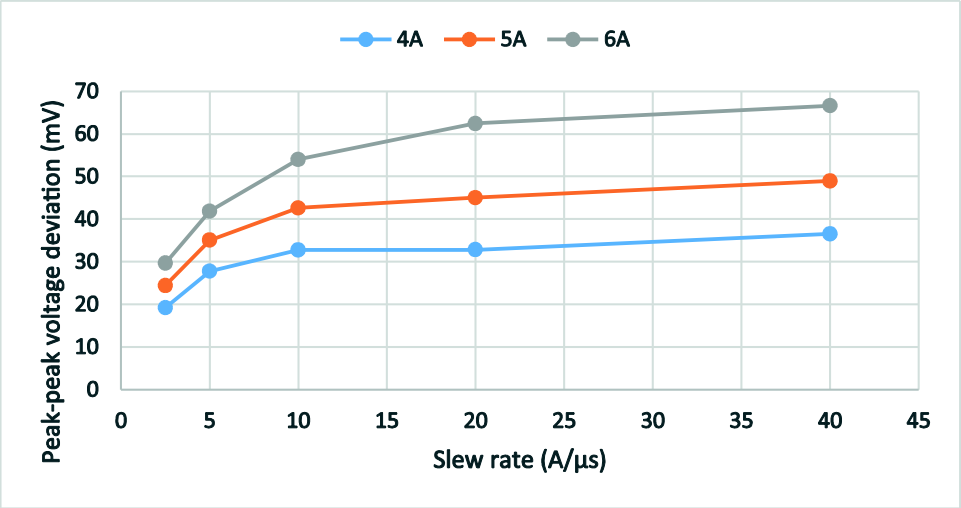


Figure 16 Peak-peak voltage deviation (PV_{IN} = 12V, V_{OUT} = 1.8V, C_{OUT} = 4 x 47 µF)

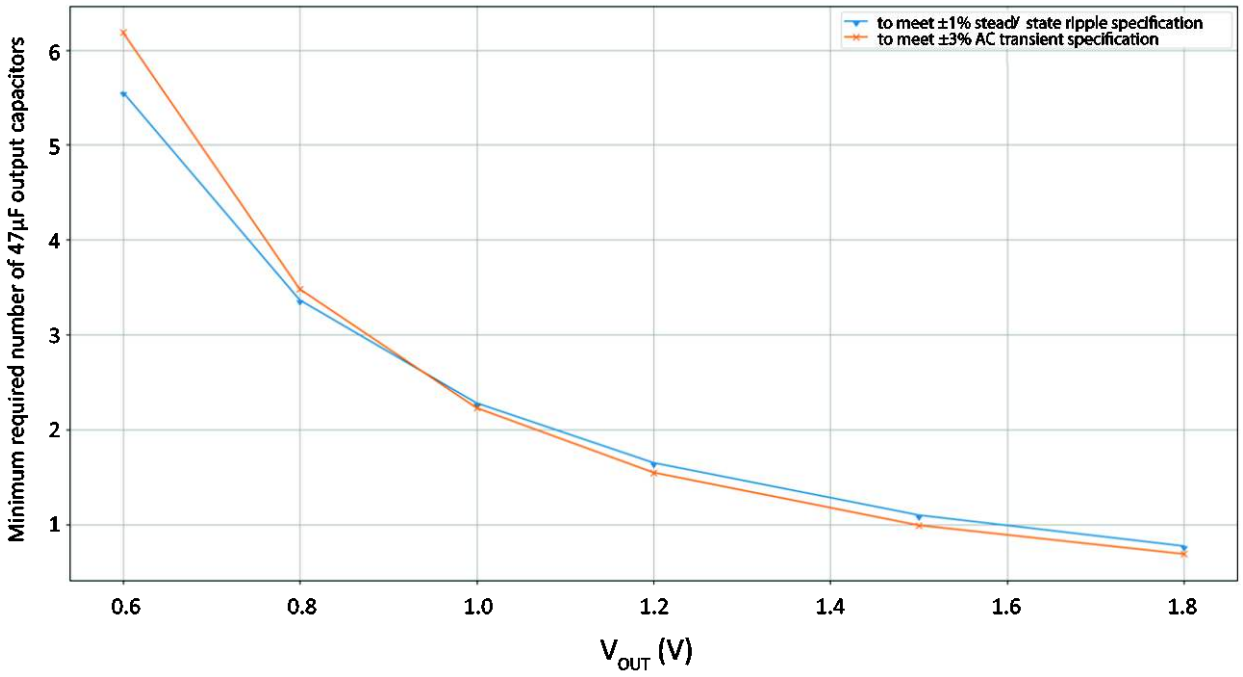
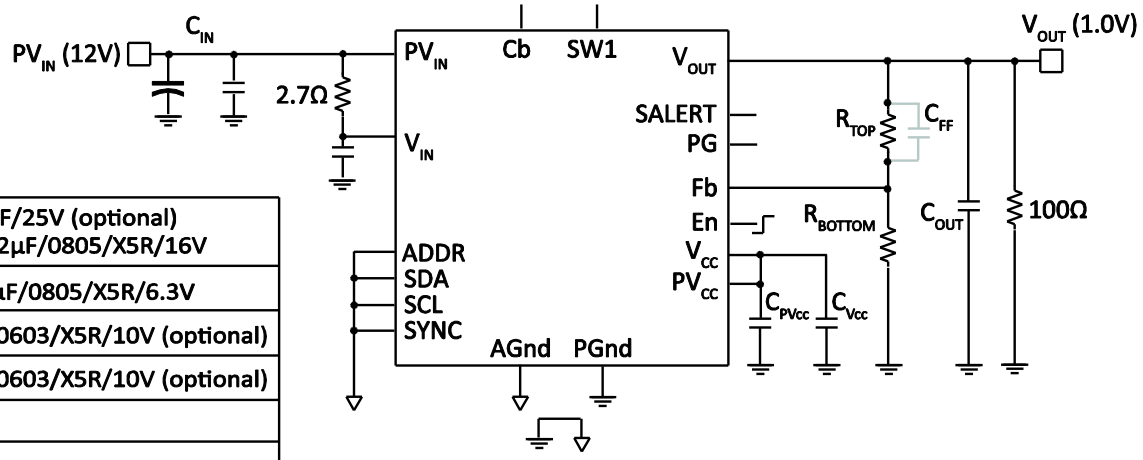


Figure 17 Minimum output capacitance



C_{IN}	1 X68µF/25V (optional) + 2 X 22µF/0805/X5R/16V
C_{OUT}	4 X 47µF/0805/X5R/6.3V
C_{PVcc}	2.2µF/0603/X5R/10V (optional)
C_{Vcc}	2.2µF/0603/X5R/10V (optional)
C_{FF}	220pF
R_{TOP}	4.12kΩ
R_{BOTTOM}	5.9kΩ

Note: SALERT and PG require pull-up resistors when used.

Figure 18 Application circuit for a single supply (PV_{IN} = 12V, V_{OUT} = 1.0V, I_{OUT} = 12A)

Typical operating waveforms

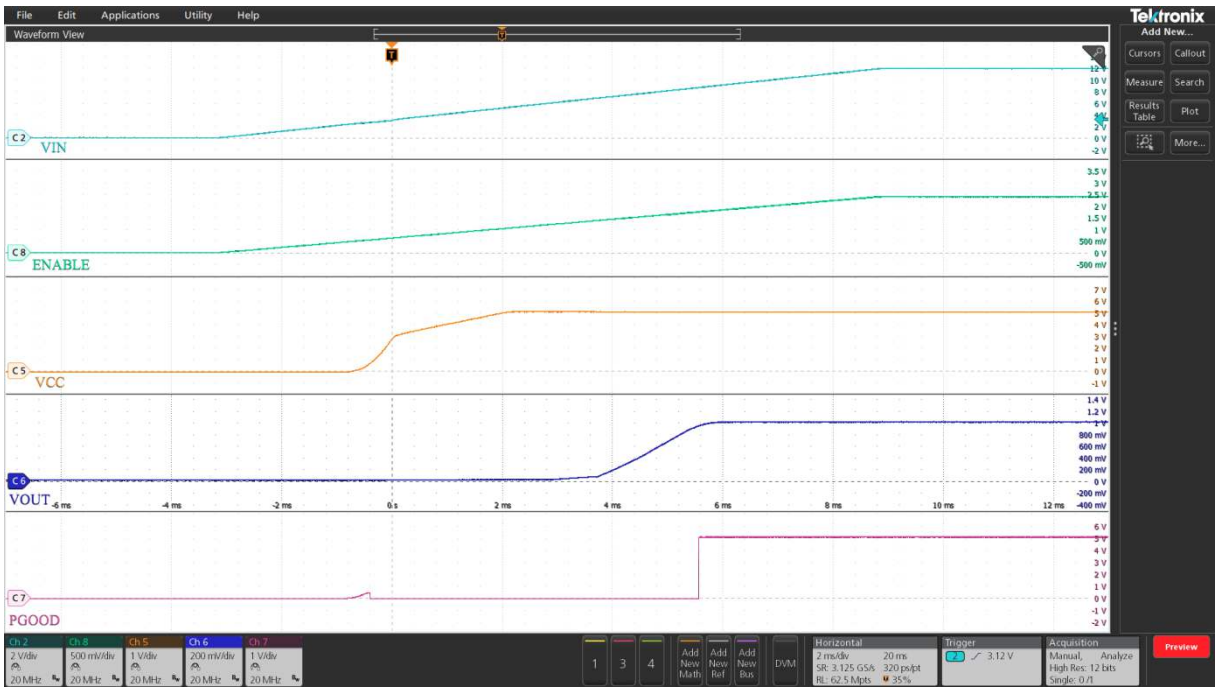


Figure 19 Startup with no load (Ch2:PV_{IN}, Ch5:V_{CC}, Ch6: V_{OUT}, Ch7: PGood, Ch8: Enable)

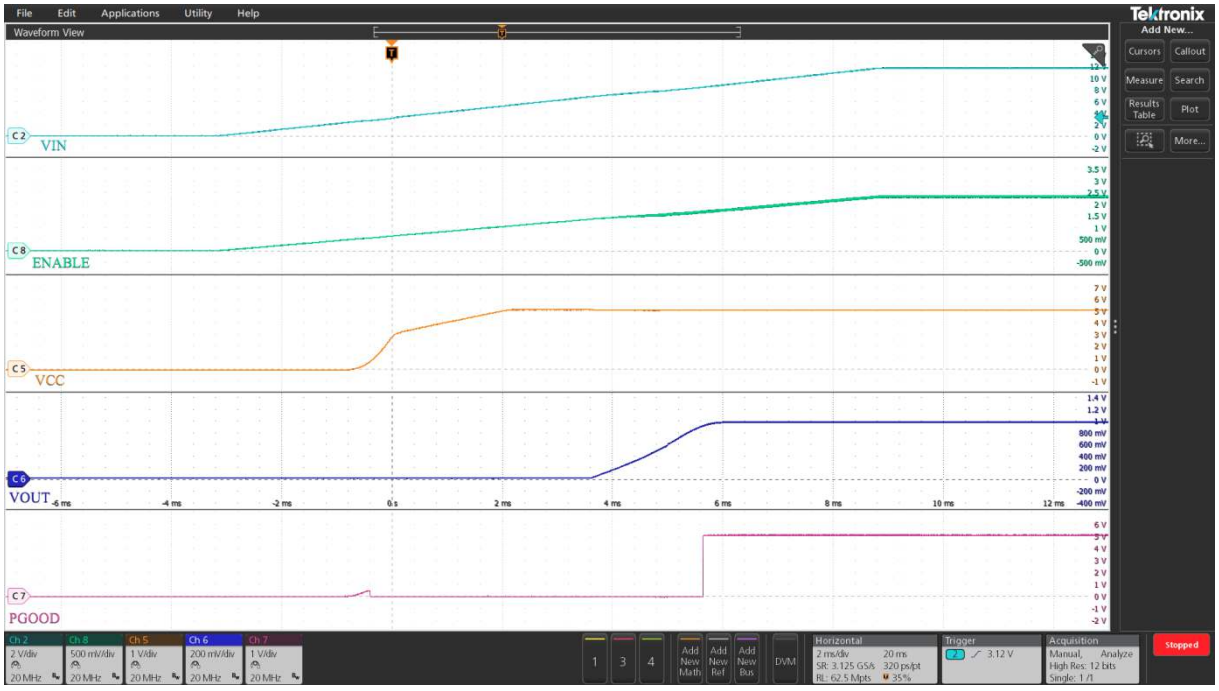


Figure 20 Startup with 12 A load (Ch2:PV_{IN}, Ch5:V_{CC}, Ch6: V_{OUT}, Ch7: PGood, Ch8: Enable)

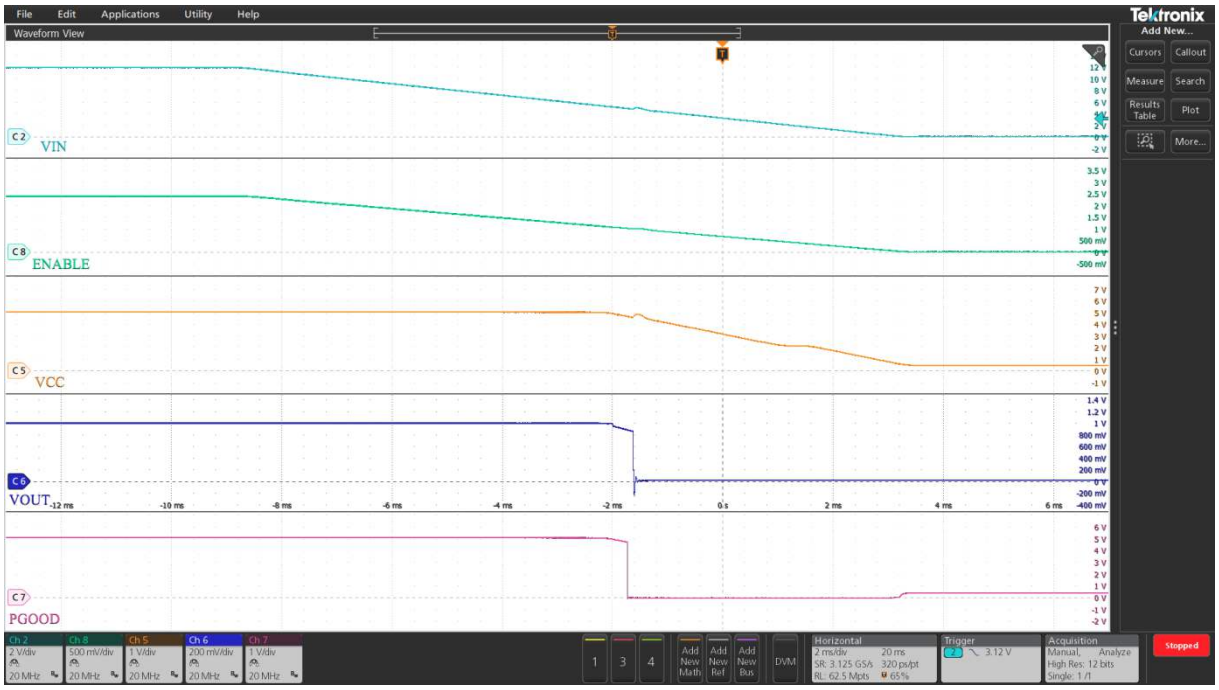


Figure 21 Shutdown with Enable de-assertion at 12A load (Ch2:PV_{IN}, Ch5:V_{CC}, Ch6: V_{OUT}, Ch7: PGood, Ch8: Enable)

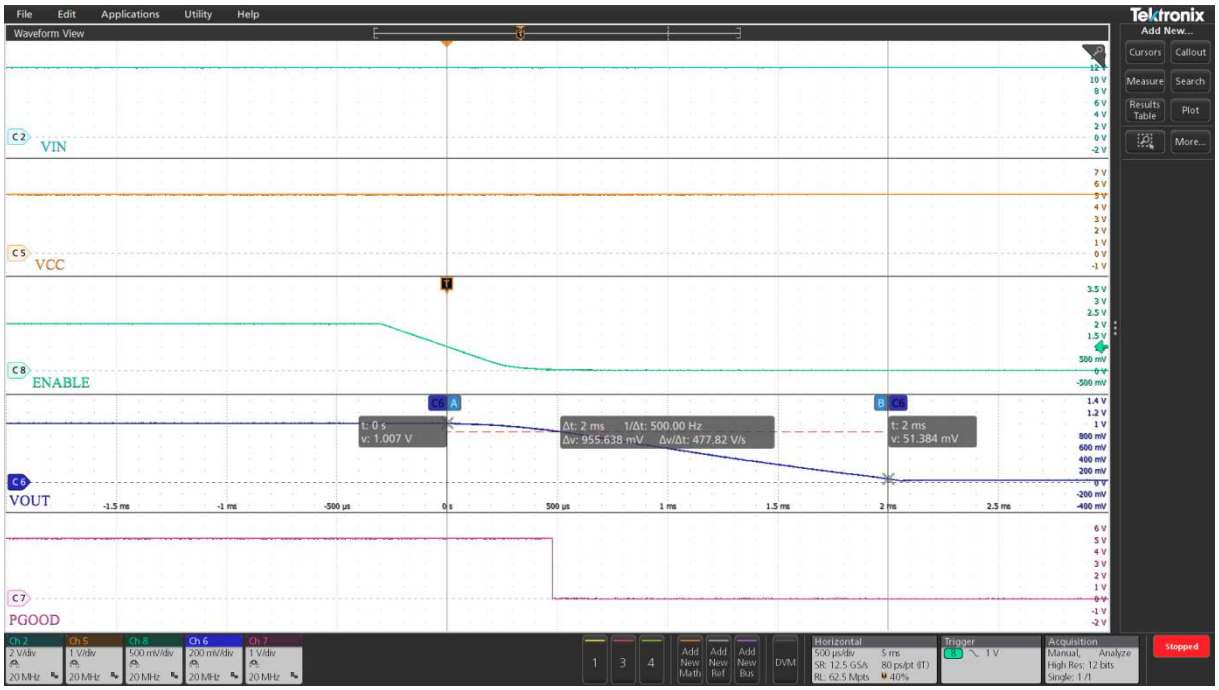


Figure 22 Soft turn off at no load (Ch2:PV_{IN}, Ch5:V_{CC}, Ch6: V_{OUT}, Ch7: PGood, Ch8: Enable)

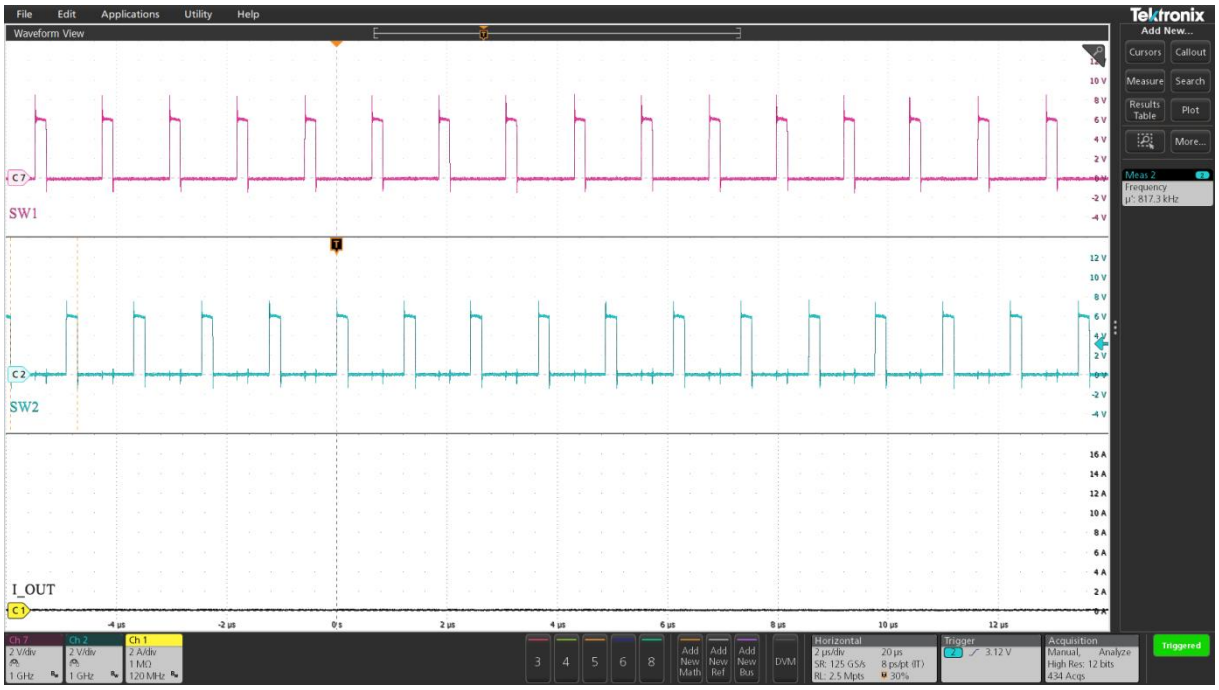


Figure 23 Switch node waveforms at no load

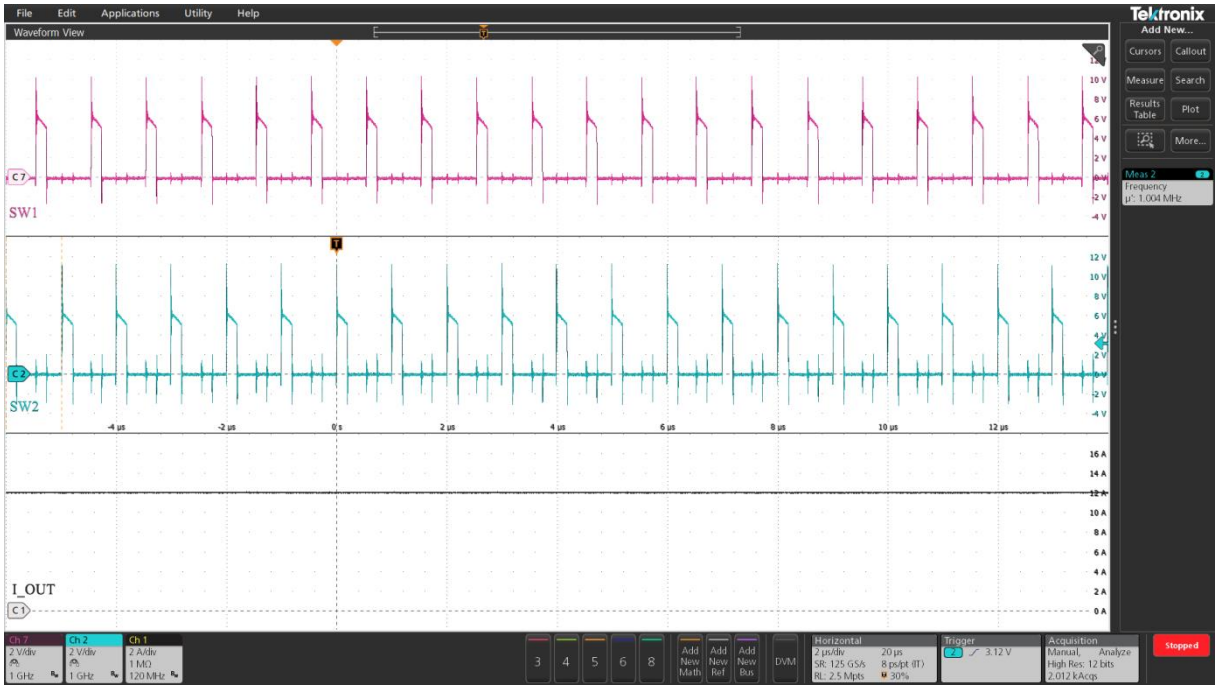


Figure 24 Switch node waveforms at 12A

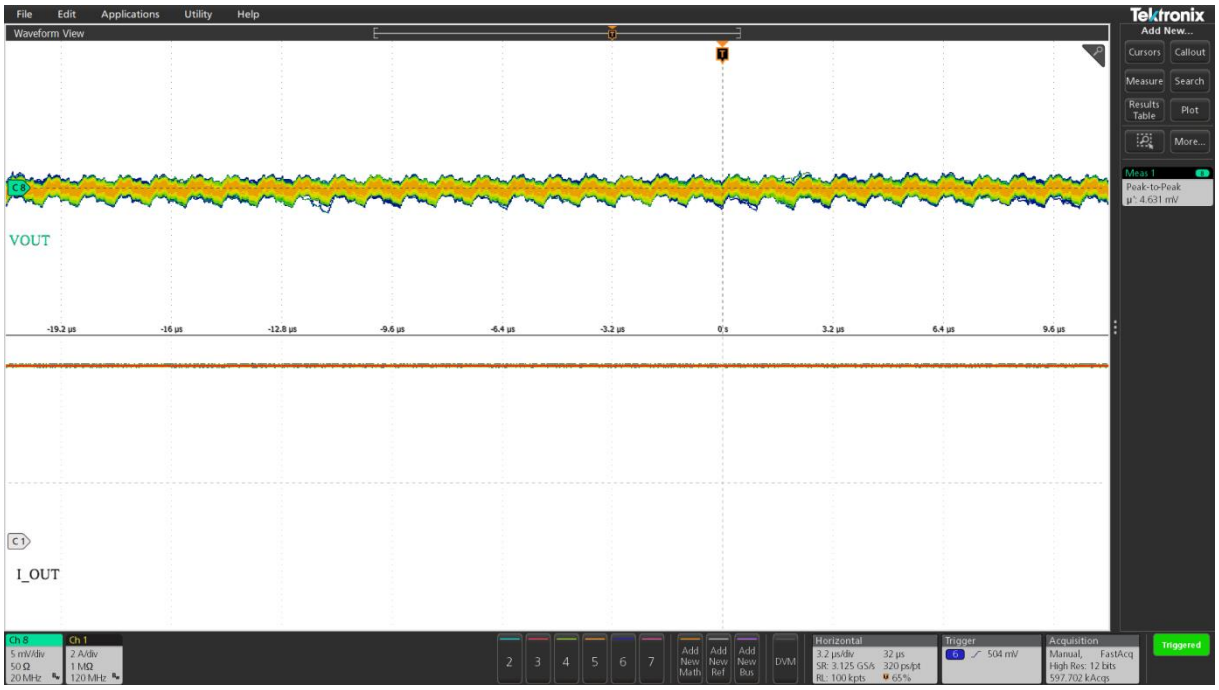


Figure 25 V_O ripple at 12A (Ch1:I_O, Ch8: V_{OUT}), peak-peak V_O ripple = 4.6mV

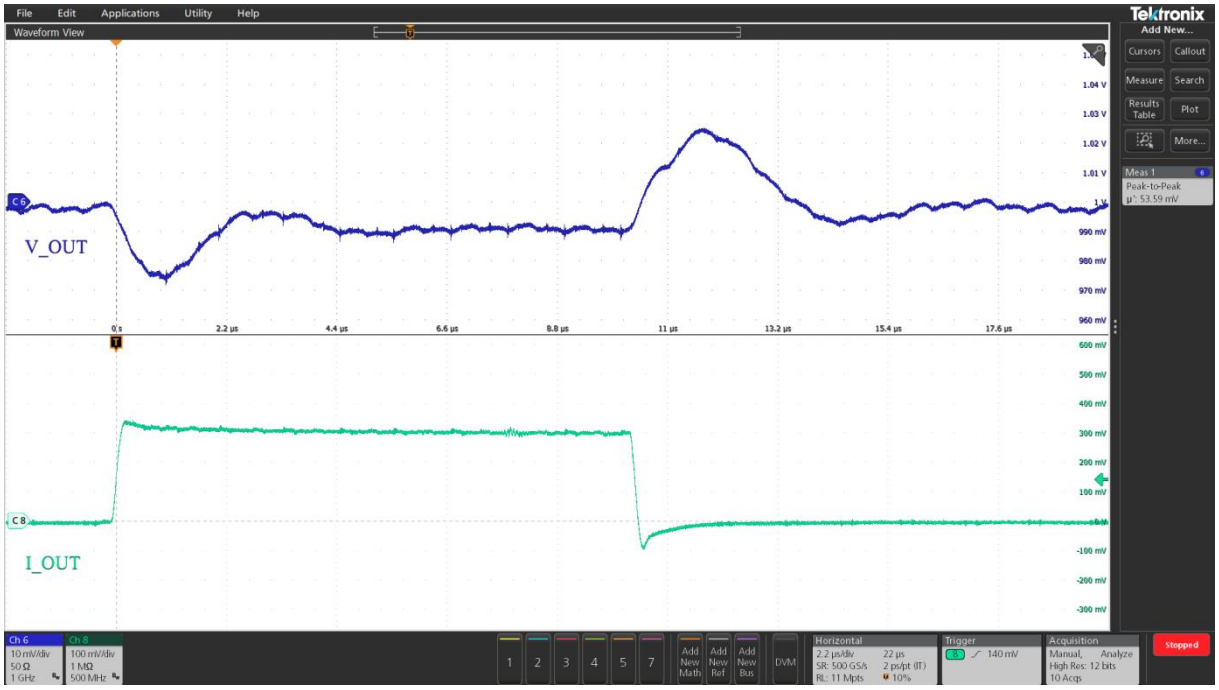


Figure 26 Transient response 0A to 6A (Ch6: V_{OUT}, Ch8:I_O), peak-peak deviation = 53 mV, load slew rate ≈ 40A/µs

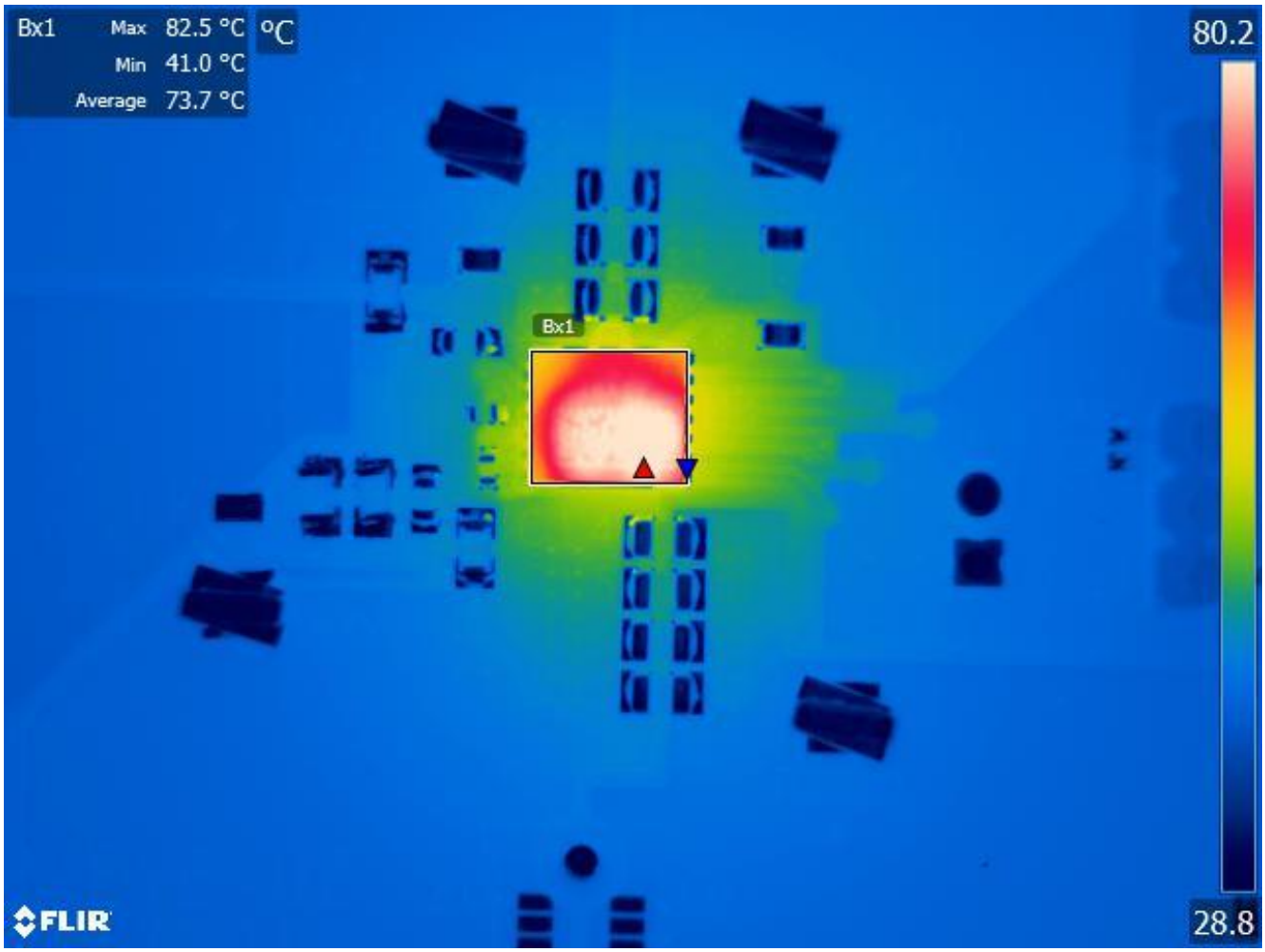


Figure 27 Thermal image at PV_{IN} = 12V, V_{OUT} = 1.0V, I_O = 12A, room temperature, no airflow, FS1412 maximum temperature rise = 55.5°C

Layout recommendations

FS1412 is a highly integrated device with very few external components, which simplifies PCB layout. However, to achieve the best performance, these general PCB design guidelines should be followed:

- Bypass capacitors, including input/output capacitors and the V_{CC} bypass capacitor (if used), should be placed as close as possible to the FS1412 pins.
- Output voltage should be sensed with a separated trace directly from the output capacitor.
- To aid thermal dissipation, the PGnd pad should be connected to the power ground plane using vias. Copper-filled vias are preferred but plated-through-hole vias are acceptable, provided that they are not covered with solder mask. VIPPO techniques are acceptable.
- Adequate numbers of vias should be used to make connections between layers, especially for the power traces.
- AGnd pins should be connected by vias to PGnd copper layer
- To minimize power losses and thermal dissipation, wide copper polygons should be used for input and output power connections.
- SCL and SDA traces must be at least 10mil wide, with 20–30mil spacing between them.

Thermal considerations

The FS1412 has been thermally tested and modelled in accordance with JEDEC specifications JESD 51-2A and JESD 51-8. It has been tested using a 4-layer application PCB, with thermal vias under the device to assist cooling (for details of the PCB, refer to the application notes).

The FS1412 has two significant sources of heat:

- The power MOSFET section of the IC
- The inductor

The IC is well coupled to the PCB, which provides its primary cooling path. Although the inductor is also connected to the PCB, its primary cooling path is through convection. The cooling process for both heat sources is ultimately through convection. The PCB can be seen as a heat-spreader or, to some degree, a heat-sink.

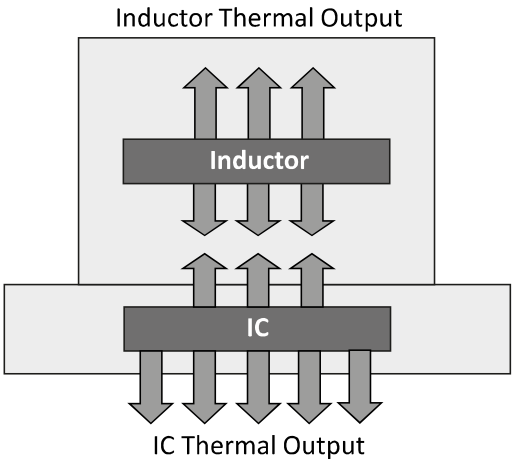


Figure 28 Heat sources in the FS1412

Figure 29 shows the thermal resistances in the FS1412, where:

- Θ_{JA} is the measure of natural convection from the assembled test sample within a confined enclosure of approximately 30x30x30cm. The air is passive within this environment and the only air movement is due to convection from the device on test.
- $\Theta_{JCbottom}$ is the heat flow from the IC to the bottom of the package, to which it is well coupled. The testing method adopts the method outlined in JESD 51-8, where the test PCB is clamped between cold plates at defined distances from the device.
- Θ_{JCtop} is theoretically the heat flow from the IC to the top of the package. This is not representative for the FS1412 for two reasons: firstly, it is not the primary conduction path of the IC and, more importantly, the inductor is positioned directly over the IC. As the inductor is a heat source, generating a similar amount of heat to the IC, a meaningful value for junction-to-case (top) cannot be derived.

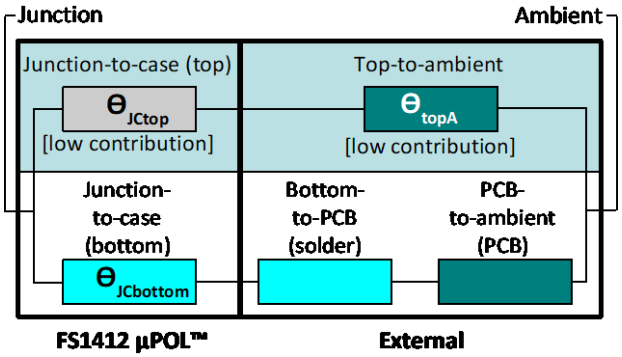


Figure 29 Thermal resistances of the FS1412

The values of the thermal resistances are:

- Θ_{JA} = 20.5°C/W
- $\Theta_{JCbottom}$ = 5.5°C/W

Although these values indicate how the FS1412 compares with similar point-of-load products tested using the same conditions and specifications, they cannot be used to predict overall thermal performance. For accurate modeling of the µPOL™'s interaction with its environment, computational fluid dynamics (CFD) simulation software is needed to calculate combined routes of conduction and convection simultaneously.

Note: In all tests, airflow has been considered as passive or static; applications using forced air may achieve a greater cooling effect.

I²C protocol

S	=	Start bit	W	=	Write bit (‘1’)	White bits	=	Issued by master
P	=	Stop bit	R	=	Read (‘0’)	Grey bits	=	Sent by slave (FS140x)
A	=	Ack	Sr	=	Repeated start			
N	=	Nack						

Write transaction

1	7	1	1	8	1	8	1	1
S	Slave Address	W	A	Register Address	A	Data Byte	A	P

Read transaction

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	W	A	Register Address	A	Sr	Slave Address	R	A	Data Byte	N	P

Supported PMBus™ commands

Code	Command	Code	Command
01	OPERATION	55	VIN_OV_FAULT_LIMIT
02	ON_OFF_CONFIG	56	VIN_OV_FAULT_RESPONSE
03	CLEAR_FAULTS	58	VIN_UV_WARN_LIMIT
15	STORE_USER_ALL	5E	POWER_GOOD_ON
16	RESTORE_USER_ALL	60	TON_DELAY
19	CAPABILITY	61	TON_RISE
1B	SMBALERT_MASK	62	TON_MAX_FAULT_LIMIT
20	VOUT_MODE	63	TON_MAX_FAULT_RESPONSE
21	VOUT_COMMAND	64	TOFF_DELAY
24	VOUT_MAX	65	TOFF_FALL
25	VOUT_MARGIN_HIGH	78	STATUS_BYTE
26	VOUT_MARGIN_LOW	79	STATUS_WORD
27	VOUT_TRANSITION_RATE	7A	STATUS_VOUT
29	VOUT_SCALE_LOOP	7B	STATUS_IOUT
35	VIN_ON	7C	STATUS_INPUT
36	VIN_OFF	7D	STATUS_TEMPERATURE
39	IOUT_CAL_OFFSET	7E	STATUS_CML
40	VOUT_OV_FAULT_LIMIT	88	READ_VIN
41	VOUT_OV_FAULT_RESPONSE	8B	READ_VOUT
42	VOUT_OV_WARN_LIMIT	8D	READ_TEMPERATURE
43	VOUT_UV_WARN_LIMIT	98	PMBUS_REVISION
44	VOUT_UV_FAULT_LIMIT	99	MFR_ID
45	VOUT_UV_FAULT_RESPONSE	9A	MFR_MODEL
46	IOUT_OC_FAULT_LIMIT	9B	MFR_REVISION
47	IOUT_OC_FAULT_RESPONSE	AD	IC_DEVICE_ID
4F	OT_FAULT_LIMIT	AE	IC_DEVICE_REV

Package description

The FS1412 is designed for use with standard surface-mount technology (SMT) population techniques. It has a positive (raised) footprint, with the pads being higher than the surrounding substrate. The finish on the pads is ENEPIG (Electroless Nickel Electroless Palladium Immersion Gold).

As a result of these properties, the FS1412 works extremely well in lead-free environments. The surface wets easily and the positive footprint accommodates processing variations.

Note: Refer to the Design Guidelines for more information about TDK's µPOL™ package series.

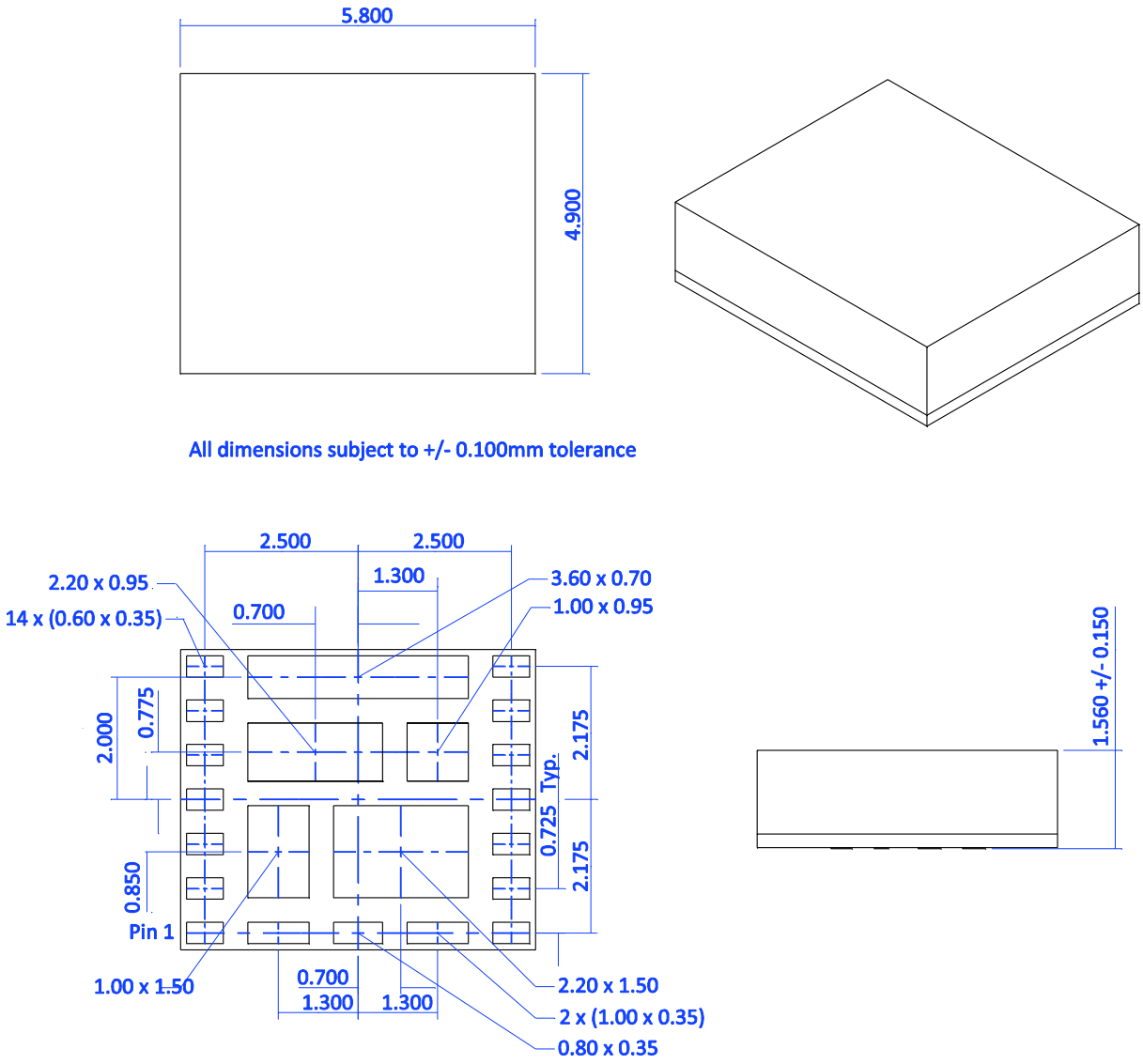


Figure 30 ***Dimensioned drawings***

REMINDERS FOR USING THESE PRODUCTS

Before using these products, be sure to request the delivery specifications.

SAFETY REMINDERS

Please pay sufficient attention to the warnings for safe designing when using these products.

REMINDER

The products listed on this specification sheet are intended for use in general electric equipment (AV equipment, telecommunication equipment, home appliances, amusement equipment, computer equipment, personal equipment, office equipment, measurement equipment, industrial robots) under a normal condition and use condition.

The products are not designed or warranted to meet the requirements of the applications listed below, whose performance and/or quality require a more stringent level of safety or reliability, or whose failure, malfunction or trouble could cause serious damage to sociality, person or property. Please understand that we are not responsible for any damage or liability caused by use of the products in any of the applications below or for any other use exceeding the range or conditions set forth in this specification sheet.

1. Aerospace/Aviation equipment
2. Transportation equipment (cars, electric trains, ships, etc.)
3. Medical equipment
4. Power-generation control equipment
5. Atomic energy related equipment
6. Seabed equipment
7. Transportation control equipment
8. Public Information-processing equipment
9. Military equipment
10. Electric heating apparatus, burning equipment
11. Disaster prevention/crime prevention equipment
12. Safety equipment
13. Other applications that are not considered general-purpose applications

When using this product in general-purpose application, you are kindly requested to take into consideration securing protection circuit/ equipment or providing backup circuits, etc., to ensure higher safety. To allow flexibility in the applications of the FS1412 device family, some parameters are accessible to the users through an I^2C/PMBus™ interface. These parameters can only be changed within limits that are acceptable to the device. However, it is the responsibility of the user to ensure that any parameter change, whether it be deliberate or inadvertent, does not violate the specifications of the end user system.

This product is subject to a license from Power One, Inc. related to digital power technology patents owned by Power One, Inc. Power One, Inc. technology is protected by patents including:

AU 3287379M 3287437AA 3290643AA 3291357AA

CN 10371856C 10452610C 10458656C 10459360C 10465848C 1069332A 11124619A 11346682A 1685299A 1685459A 1685582A 1685583A 1698023A 1802619A

EP 1561156A1 1561268A2 1576710A1 1576711A1 1604254A4 1604264A4 1714369A2 1745536A4 1769382A4 1899789A2 1984801A2

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