

# TK35N65W

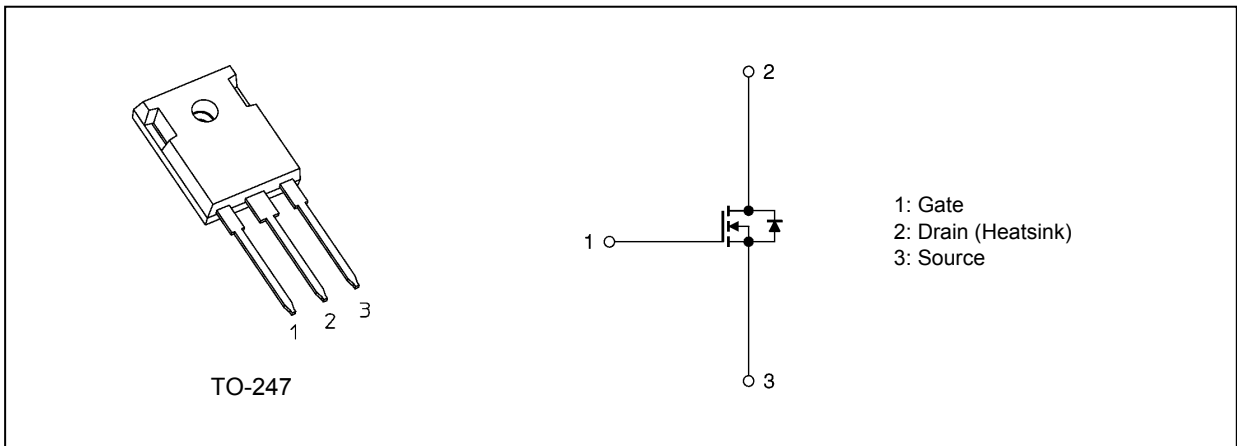
## 1. Applications

- Switching Voltage Regulators

## 2. Features

- (1) Low drain-source on-resistance:  $R_{DS(ON)} = 0.068 \Omega$  (typ.)  
by used to Super Junction Structure : DTMOS
- (2) Easy to control Gate switching
- (3) Enhancement mode:  $V_{th} = 2.5$  to  $3.5$  V ( $V_{DS} = 10$  V,  $I_D = 2.1$  mA)

## 3. Packaging and Internal Circuit



## 4. Absolute Maximum Ratings (Note) ( $T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	650	V
Gate-source voltage	$V_{GSS}$	$\pm 30$	
Drain current (DC)	$I_D$ (Note 1)	35	A
Drain current (pulsed)	$I_{DP}$ (Note 1)	140	
Power dissipation	$P_D$ ( $T_c = 25^\circ\text{C}$ )	270	W
Single-pulse avalanche energy	$E_{AS}$ (Note 2)	614	mJ
Avalanche current	$I_{AR}$	8.8	A
Reverse drain current (DC)	$I_{DR}$ (Note 1)	35	
Reverse drain current (pulsed)	$I_{DRP}$ (Note 1)	140	
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to 150	
Mounting torque	TOR	0.8	N · m

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production  
2013-08

**5. Thermal Characteristics**

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	$R_{th(ch-c)}$	0.463	°C/W
Channel-to-ambient thermal resistance	$R_{th(ch-a)}$	50	

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2:  $V_{DD} = 90\text{ V}$ ,  $T_{ch} = 25^\circ\text{C}$  (initial),  $L = 14\text{ mH}$ ,  $R_G = 25\ \Omega$ ,  $I_{AR} = 8.8\text{ A}$

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

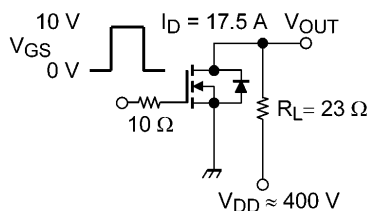
**6. Electrical Characteristics**

**6.1. Static Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	—	—	$\pm 1$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	650	—	—	V
Gate threshold voltage	$V_{th}$	$V_{DS} = 10\text{ V}, I_D = 2.1\text{ mA}$	2.5	—	3.5	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 17.5\text{ A}$	—	0.068	0.08	$\Omega$

**6.2. Dynamic Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = 300\text{ V}, V_{GS} = 0\text{ V}, f = 100\text{ kHz}$	—	4100	—	$\text{pF}$
Reverse transfer capacitance	$C_{rss}$		—	9	—	
Output capacitance	$C_{oss}$		—	90	—	
Effective output capacitance	$C_{o(er)}$	$V_{DS} = 0\text{ to }400\text{ V}, V_{GS} = 0\text{ V}$	—	130	—	
Gate resistance	$r_g$	$V_{DS} = \text{OPEN}, f = 1\text{ MHz}$	—	2	—	$\Omega$
Switching time (rise time)	$t_r$	See Figure 6.2.1	—	30	—	$\text{ns}$
Switching time (turn-on time)	$t_{on}$		—	70	—	
Switching time (fall time)	$t_f$		—	8	—	
Switching time (turn-off time)	$t_{off}$		—	150	—	
MOSFET dv/dt ruggedness	dv/dt	$V_{DD} = 0\text{ to }400\text{ V}, I_D = 17.5\text{ A}$	50	—	—	V/ns



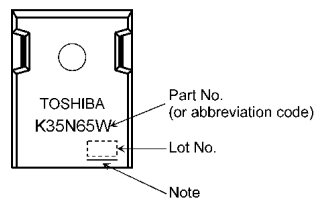
Duty  $\leq 1\%$ ,  $t_w = 10\ \mu\text{s}$   
**Fig. 6.2.1 Switching Time Test Circuit**

**6.3. Gate Charge Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DD} \approx 400\text{ V}, V_{GS} = 10\text{ V}, I_D = 35\text{ A}$	—	100	—	$\text{nC}$
Gate-source charge 1	$Q_{gs1}$		—	25	—	
Gate-drain charge	$Q_{gd}$		—	35	—	

**6.4. Source-Drain Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage	$V_{DSF}$	$I_{DR} = 35\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.7	V
Reverse recovery time	$t_{rr}$	$I_{DR} = 17.5\text{ A}, V_{GS} = 0\text{ V}$ $-dI_{DR}/dt = 50\text{ A}/\mu\text{s}$	—	430	—	$\text{ns}$
Reverse recovery charge	$Q_{rr}$		—	4.2	—	$\mu\text{C}$
Peak reverse recovery current	$I_{rr}$		—	21	—	A
Diode dv/dt ruggedness	dv/dt	$I_{DR} = 17.5\text{ A}, V_{GS} = 0\text{ V}, V_{DD} = 400\text{ V}$	15	—	—	V/ns

**7. Marking (Note)****Fig. 7.1 Marking**

Note: A line under a Lot No. identifies the indication of product Labels.

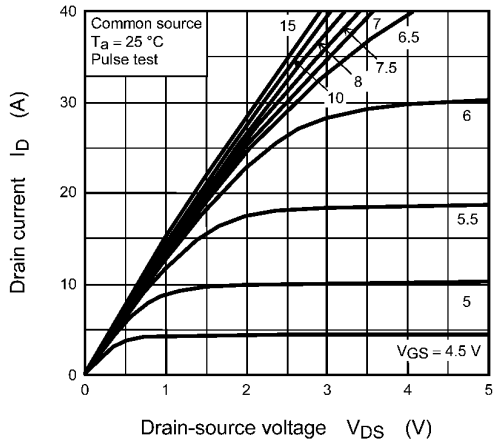
Not underlined: [[Pb]]/INCLUDES > MCV

Underlined: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

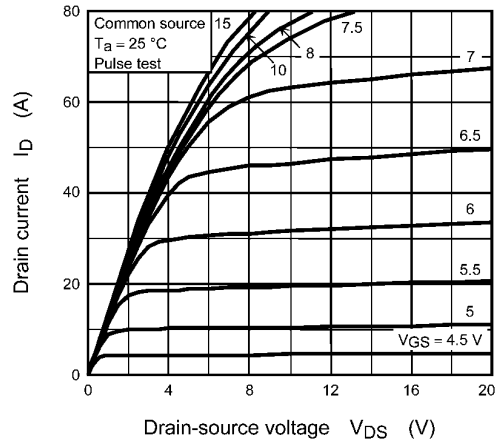
Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product.

The RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

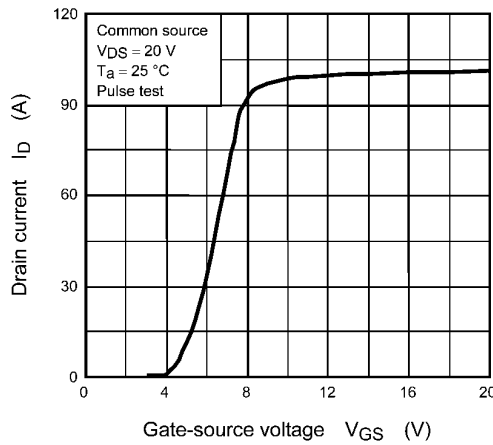
**8. Characteristics Curves (Note)**



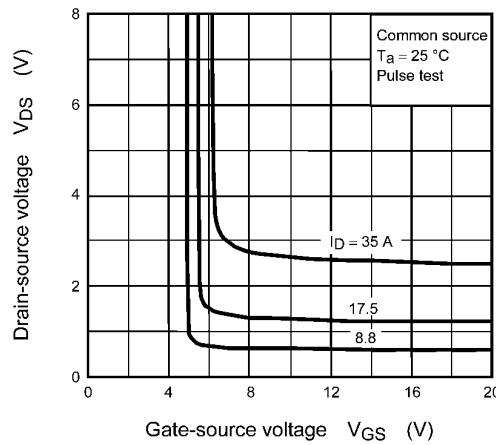
**Fig. 8.1  $I_D - V_{DS}$**



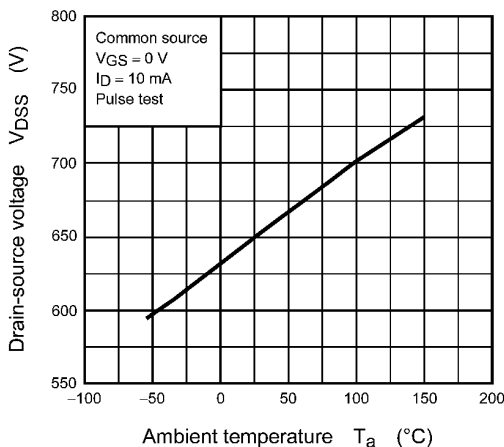
**Fig. 8.2  $I_D - V_{DS}$**



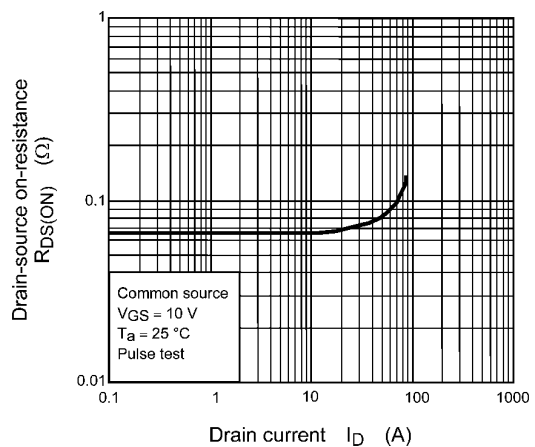
**Fig. 8.3  $I_D - V_{GS}$**



**Fig. 8.4  $V_{DS} - V_{GS}$**



**Fig. 8.5  $V_{DSS} - T_a$**



**Fig. 8.6  $R_{DS(ON)} - I_D$**

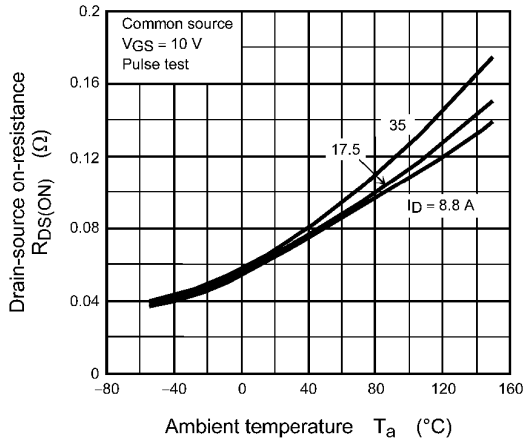


Fig. 8.7  $R_{DS(ON)} - T_a$

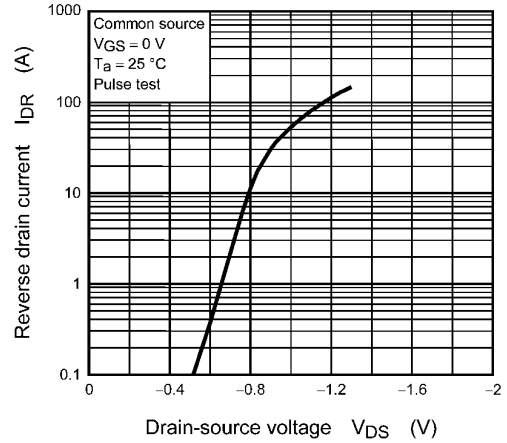


Fig. 8.8  $I_{DR} - V_{DS}$

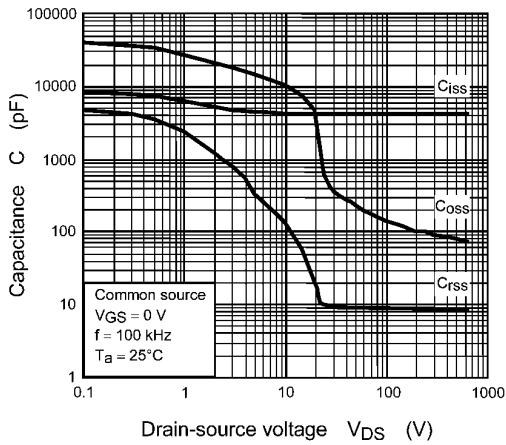


Fig. 8.9  $C - V_{DS}$

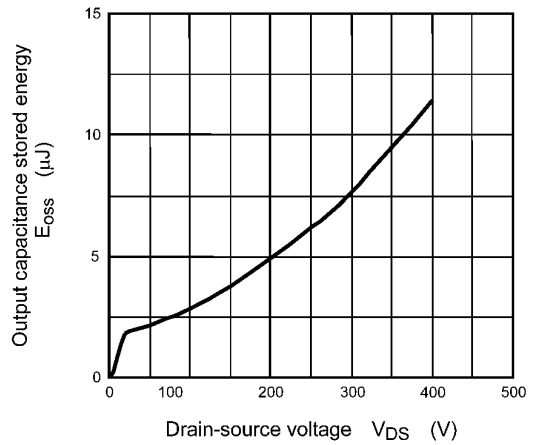


Fig. 8.10  $E_{oss} - V_{DS}$

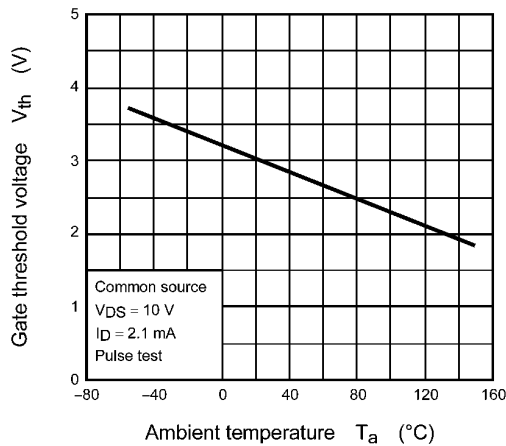


Fig. 8.11  $V_{th} - T_a$

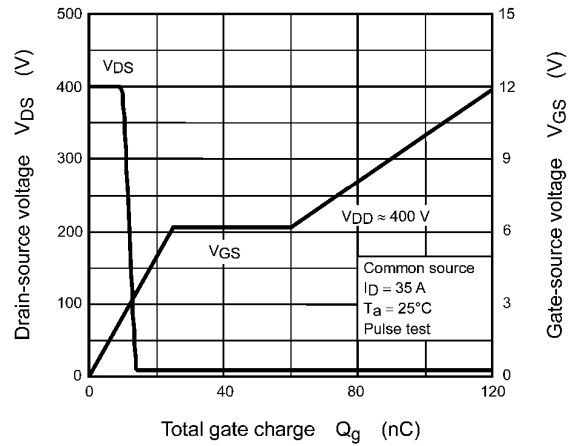
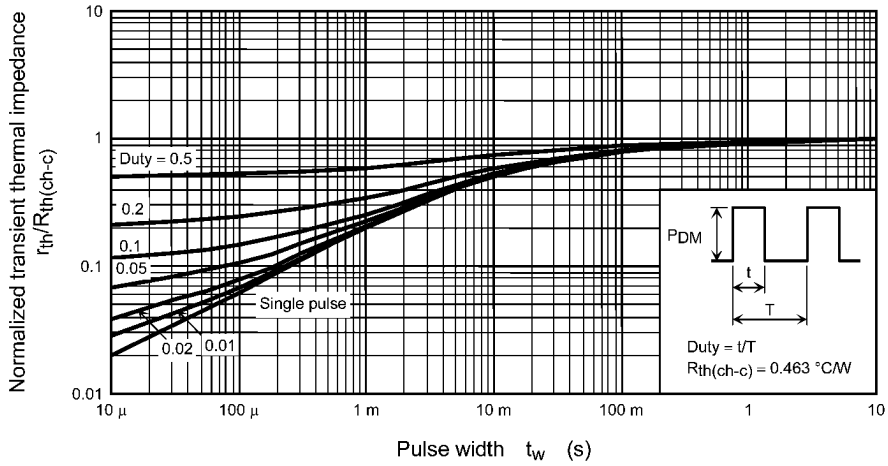
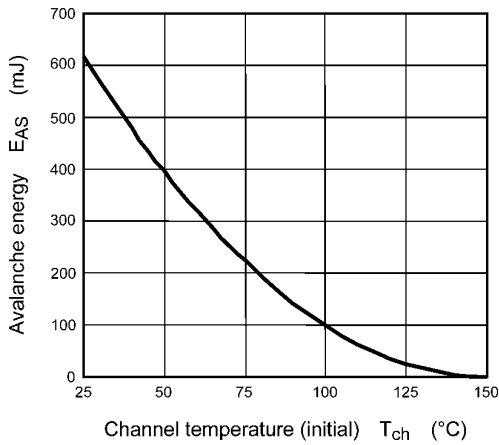


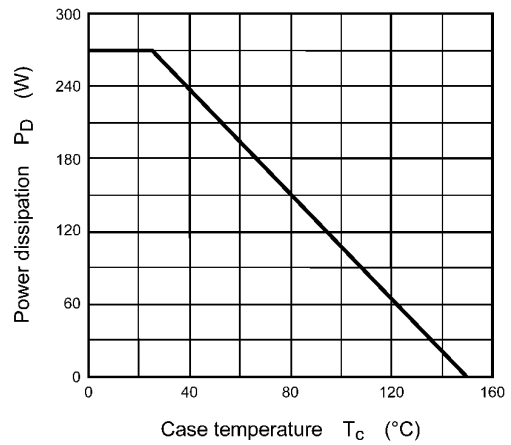
Fig. 8.12 Dynamic Input/Output Characteristics



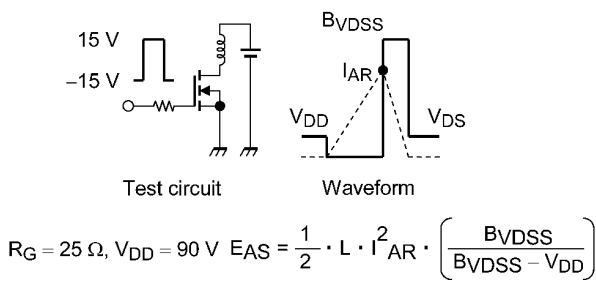
**Fig. 8.13**  $r_{th} - t_w$   
(Guaranteed Maximum)



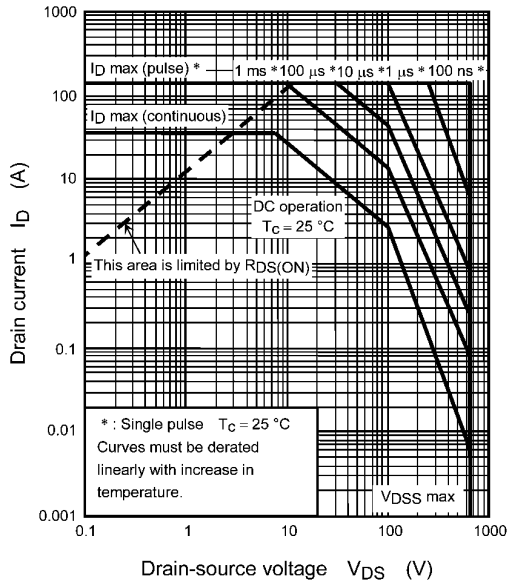
**Fig. 8.14**  $E_{AS} - T_{ch}$   
(Guaranteed Maximum)



**Fig. 8.15**  $P_D - T_c$   
(Guaranteed Maximum)



**Fig. 8.16** Test Circuit/Waveform



**Fig. 8.17 Safe Operating Area (Guaranteed Maximum)**

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.





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