TEXAS INSTRUMENTS

SN65LVDS122EVM

User's Guide

March 2003 *High-Performance Linear/Interface Products*

SLLU056A

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 3 V to 3.6 V specified in this User's Guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 70°C. The EVM is designed to operate properly with certain components above 70°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Chapter 1

Introduction

This chapter gives a brief overview of the SN65LVDS122EVM and highlights the high-speed performance and functionality of the SN65LVDS122, 2x2 cross-point switch.

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1.1 Overview

The SN65LVDS122 is a 1.5-Gbps 2x2 cross-point switch. The four different functions that the SN65LVDS122 provides are shown in Figure 1–1. The function of the SN65LVDS122 is selected via pins S0 and S1. Control pins 1DE and 2DE enable or disable the outputs. The output levels of this device are LVDS, while the receiver has a wide input common-mode voltage range with an ability to accept LVPECL and CML signaling levels in addition to LVDS.

Figure 1–1. Functional Configurations of the SN65LVDS122

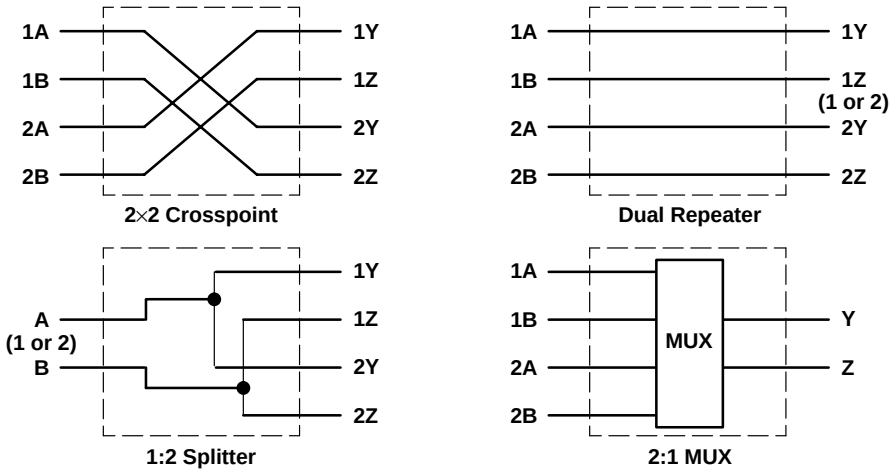
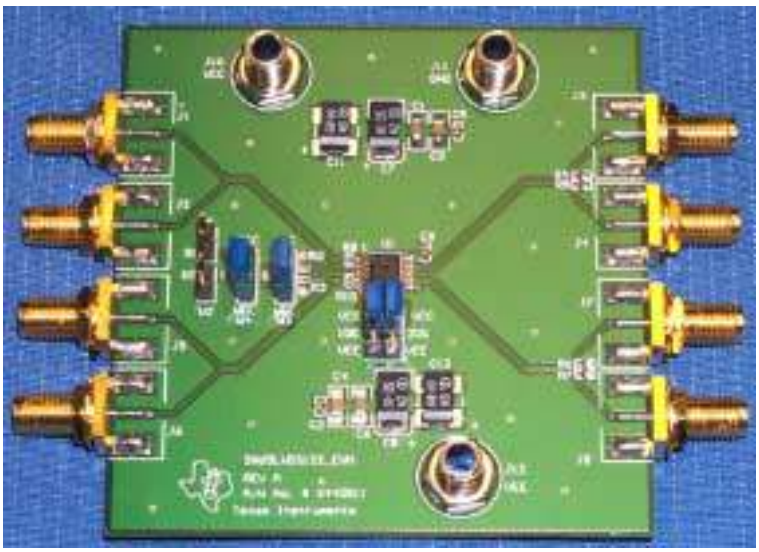


Figure 1–2 is a picture of the SN65LVDS122PW and EVM. The EVM part number is SN65LVDS122EVM. The EVM comes with the SN65LVDS122PW (TSSOP) installed. A copy of the data sheet is shipped with the EVM. The lastest version of the data sheet is available from www.ti.com.

Figure 1–2. SN65LVDS122 EVM



1.2 Signal Paths

The signal paths on this EVM include eight edge-launch SMA connectors (J1–J8) for high-speed data transmission, two jumpers (W1, W2) for active switch logic control, two jumpers (W3, W4) for static switch logic control, one jumper (J9) for enabling and disabling the outputs, and three banana jacks (J10, J11, J12) for power and ground connections.

Chapter 2

Setup and Equipment Required

This chapter describes the equipment, setup, and operation of the SN65LVDS122EVM.

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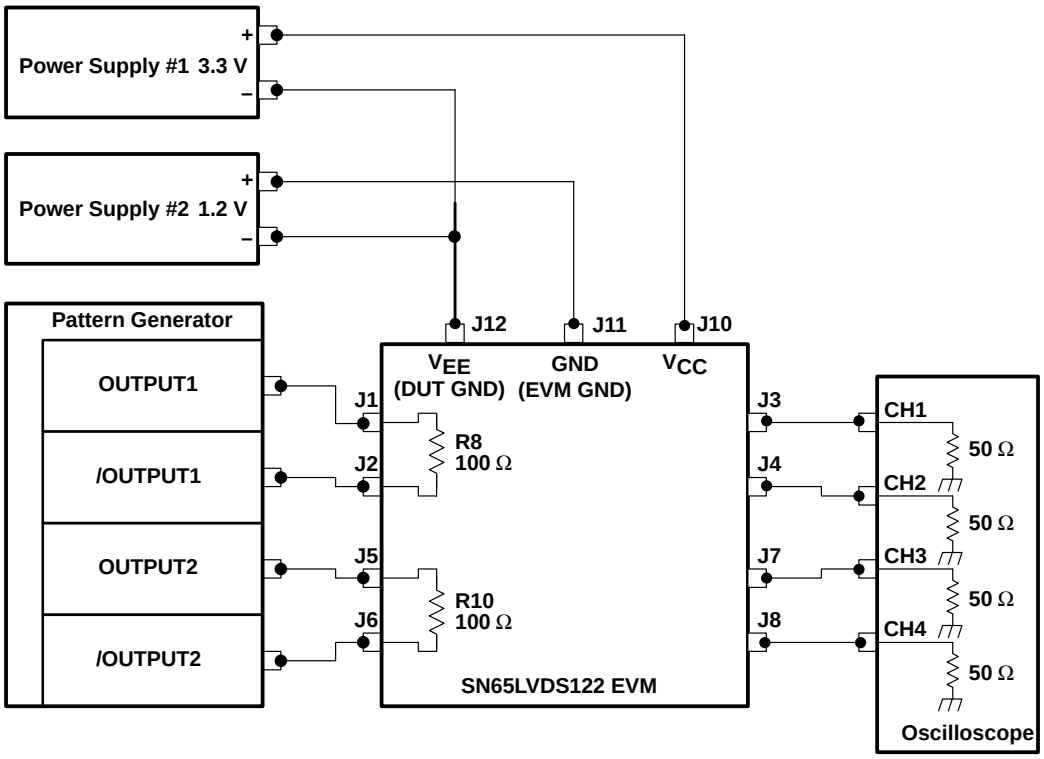
2.1 Overview

TIA/EIA–644 specifies the LVDS driver output characteristics such that it maintains at least 247 mV across a 100-Ω differential load. This requirement includes the effects of up to 32 standard receivers with their ground reference up to 1 V different from that of the driver. This common-mode loading limitation of LVDS drivers affects how they are observed and much of the test set up that follows. By using three power jacks (J10, J11, and J12), different methods of termination or probing the output characteristics can be observed without exceeding the common-mode drive capability. Figure 2–1 shows the typical setup for the SN65LVDS122EVM.

Figure 2–1. EVM Power Connections for SN65LVDS122 Evaluation

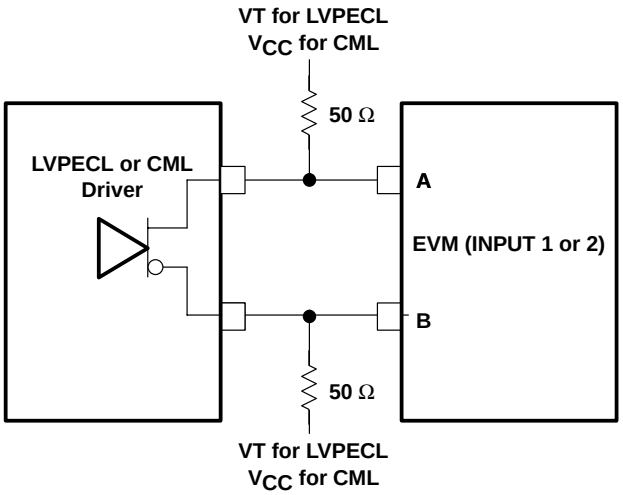


2.2 Applying an Input

When using a general-purpose signal generator with 50-Ω output impedance, make sure that the signal levels are between 0 V and 4 V with respect to J12, device under test ground (DUT GND), designated as VEE.

Inputs should be applied to the SMA connectors J1, J2, J5, and J6. Matched cable lengths must be used when connecting the signal generator to the EVM to avoid inducing skew between the noninverting and inverting inputs. The EVM comes with 100-Ω resistors installed across the differential inputs for LVDS termination. The simple 100-Ω terminations do not provide the necessary termination for LVPECL or CML[1] output structures. In order to interface the SN65LVDS122 EVM with CML or LVPECL drivers, external terminations are required. Figure 2–2 shows an example termination for LVPECL and CML output structures. Remove resistors R8 and R10 when using the external terminations.

Figure 2–2. External Termination for Interfaceing CML or LVPECL Drivers



The use of external resistors creates a significant stub between the termination and the actual device receivers. The user needs to verify that the transition time of the input signal, coupled with the stub length, does not lead to reflection problems. In normal applications, the termination would be placed as close as possible to the device inputs to minimize reflections.

The control lines S0 and S1 can be stimulated by an external 50-Ω source, via jumpers W1 and W2. These control signals are LVTTL compatible inputs and therefore the external source should provide LVTTL inputs relative to J12. If S0 and S1 are controlled by an external source, then remove the jumpers from W3 and W4 and install 50-Ω resistors R2 and R3.

[1]CML is not a standardized physical layer and therefore the output structures and required termination differ from vendor to vendor.

2.3 Observing an Output

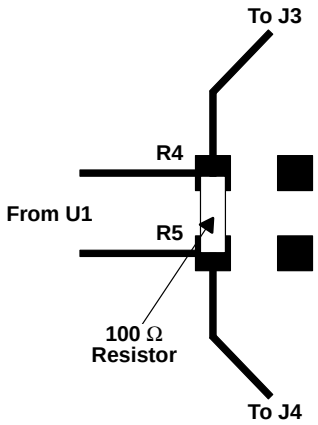
When the SN65LVDS122 EVM is connected directly to an oscilloscope with 50–Ω internal terminations to ground; resistors R4, R5, R6, and R7 are not needed (the EVM is shipped without R4–R7 installed). All external cabling needs to be matched in length to prevent skew between inverting and noninverting signals and between channels.

The three power jacks (J10, J11, and J12) are used to provide power and a ground reference for the EVM. The power connections to the EVM determine the common-mode load the device outputs must drive. LVDS devices have limited common-mode driver capability and when using 50-Ω termination on each line of the signal pair, they should be connected to a 1.2-V termination voltage with respect to the driver ground. When connecting the EVM outputs directly to oscilloscope inputs, the oscilloscope ground becomes termination voltage and the objective of the three power jacks (split power plane) is to offset the SN65LVDS122, so that the termination appears as 50 Ω to 1.2 V.

Returning to Figure 2–1, power supply #1 provides 3.3 V to the EVM and power supply #2 provides the offset voltage. This offset is used to set the DUT ground potential with respect to EVM GND. The ground returns in the SMA connectors connects EVM GND to the oscilloscope ground. Optimum device setup can be confirmed by adjusting the voltage on the offset power supply until its current is minimized. It is important to note that use of the dual supplies and offsetting the EVM relative to the DUT ground are steps needed for the test and evaluation of devices. Actual designs would include high-impedance receivers, which would not require offsetting the load.

If the EVM outputs are to be evaluated with a high-impedance probe, direct probing on the EVM is supported via installation of a 100-Ω resistor across the solder pads for R4 and R5 (see Figure 2–3) and another 100-Ω resistor across the solder pads for R6 and R7. The advantage of using a high-impedance probe is that the power supply #2 of Figure 2–1 can be omitted with J12 and J11 connected together. In order to successfully offset the EVM, power supply #2 must be able to sink current. The disadvantage is the possible bandwidth limitations of the probe and measurement quality.

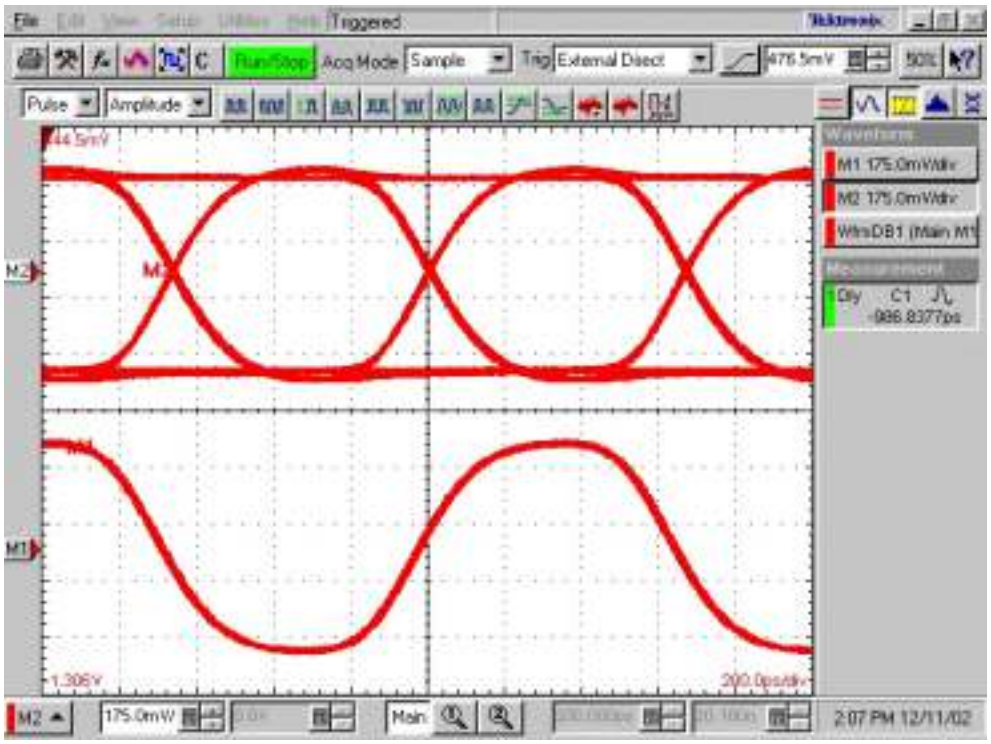
Figure 2–3. 100- Parallel Termination Using Solder Pads From R4 and R5



2.4 Typical Test Results

Figure 2–4 is a typical result obtained with the EVM setup shown in Figure 2–1. The upper waveform is the difference voltage between channels 1 and 2 of the oscilloscope and the lower trace is the difference voltage between channels 3 and 4. The DUT was configured to send the 1B/1A inputs to the outputs 2Z/2Y and inputs 2A/2B to outputs 1Y/1Z by setting 1DE and 2DE to a high level and by setting W3 and W4 to V_{CC}. The stimuli were a 2^{23}–1 PRBS to J1 and J2 at 1.5 Gbps, and a 750 MHz clock to J5 and J6. The input levels for both clock and data were a differential voltage of 400 mV with a common-mode voltage of 0 V (referenced to the ground of the pattern generator).

Figure 2–4. Typical Test Results With the SN65LVDS122EVM



Chapter 3

EVM Construction

This chapter provides the SN65LVDS122EVM schematic, board layers, and bill of materials.

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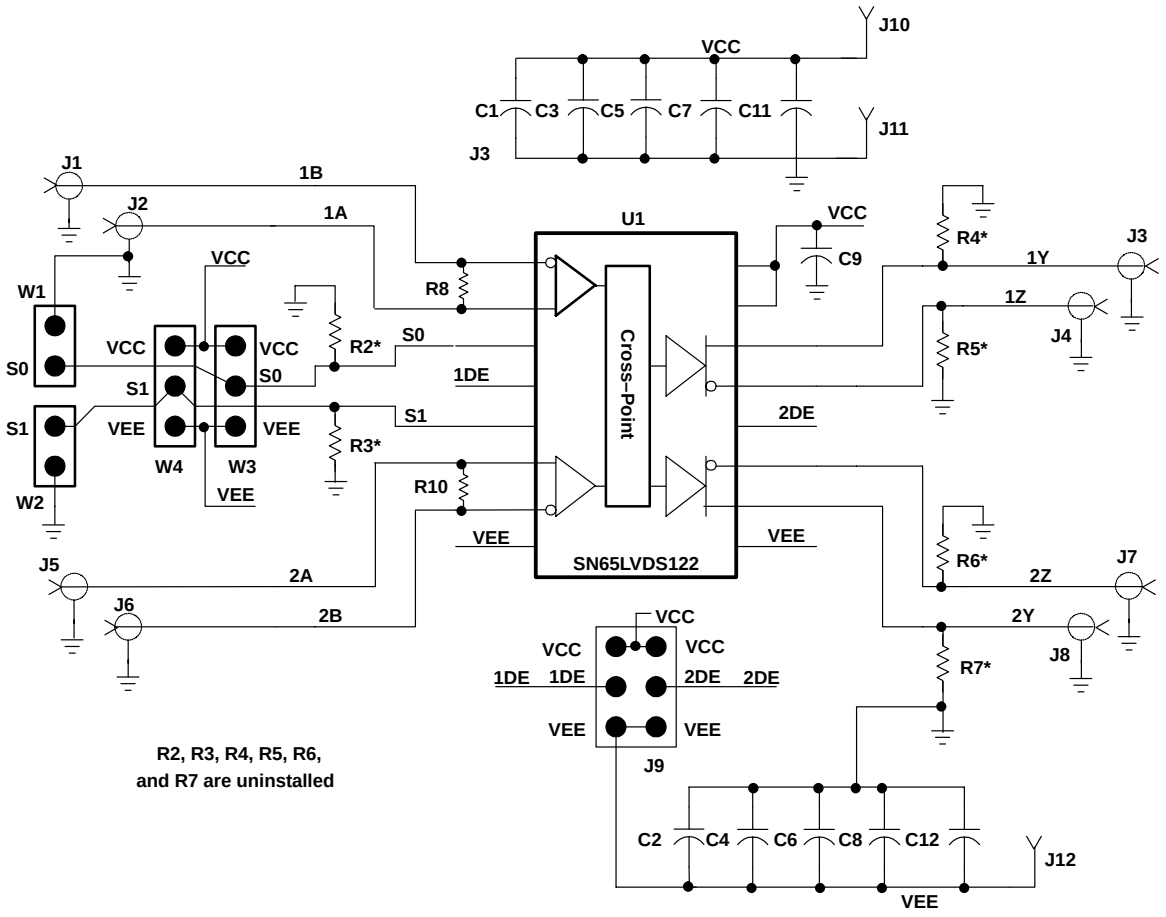
3.1 Schematic

Figure 3–1. SN65LVDS122EVM Schematic



3.2 Board Layout Patterns

Figure 3–2. SN65LVDS122EVM Silk Screen

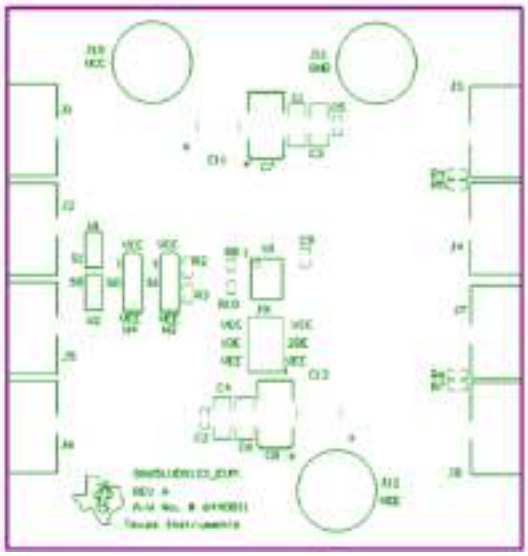


Figure 3–3. Signal Layer and GND Fill

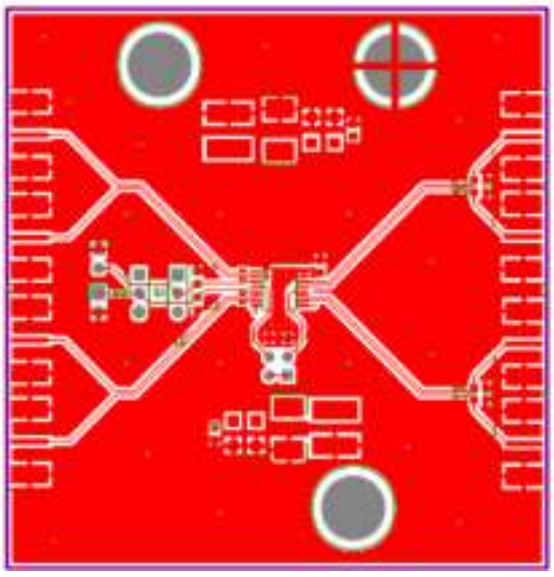


Figure 3–4. Layer 2 GND Plane

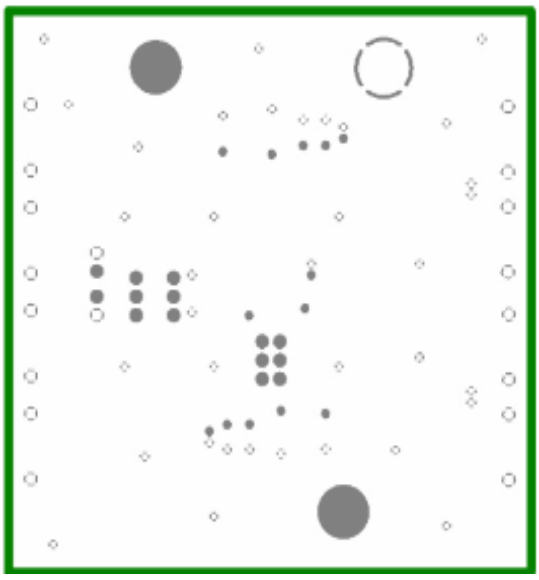


Figure 3–5. Layer 3 Split V_{CC} amd V_{EE}

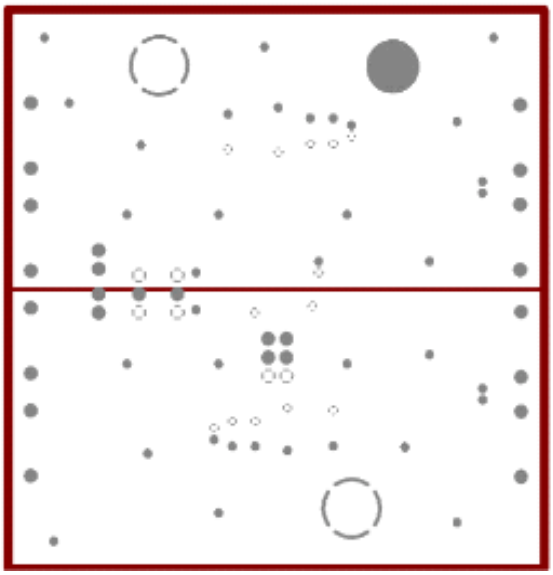


Figure 3–6. Layer 4 GND Plane

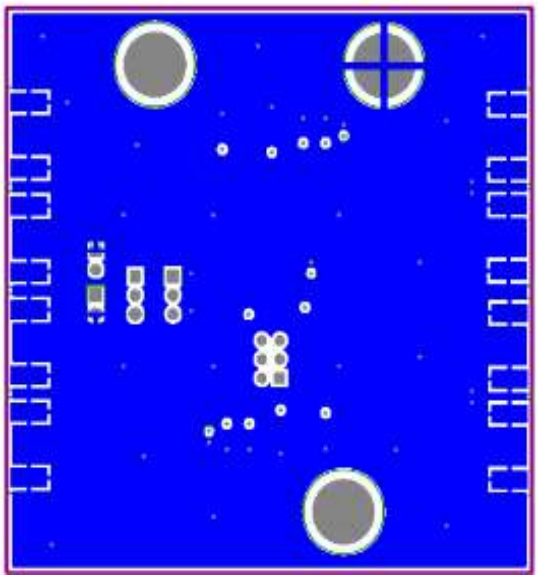
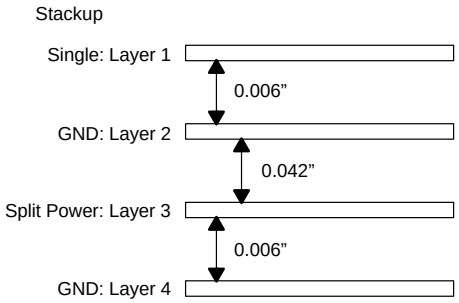


Figure 3–7. PCB Fabrication Notes and Stackup

Notes:

1) PWB to be fabricated to meet or exceed IPC-6012, Class 3 standards and workmanship conform to IPC-A-600, Class 3 current revisions
2) Board material and construction to be UL approved and marked on the finished board.
3) Laminate materal: Copper-clad NELCO N4000-13 (DO NOT USE—13SI)
4) Copper weight: 1 oz finished
5) Finished thickness: 0.62” ±0.10”
6) Minimum plating thickness in through holes: 0.001”
7) SMOBC/HASL
8) LPI soldermask both sides using appropriate layer artwork: color = green
9) LPI silkscreen as required: color = white
10) LPI soldermask both sides using appropriate layer artwork: color = green
11) Minimum copper conductor width is: 0.010”
Minimum conductor spacing is: 0.009”
12) Number of finished layers: 4
13) Top layer 10 mil traces to be 50-Ω impedance
14) Spacing between layers 3 and 4 should be 0.006”



3.3 Bill of Materials

Table 3–1. Bill of Materials for SN65LVDS122EVM—Rev A.PCB

Comment	Pattern	Qty.	Components
0.001 μF, 25 V, 5%	603	1	C9
0.01 μF, 50 V, ±10%	603	1	C2, C5
0.1 μF, 50 V, 5%	1206	2	C3, C4
100 Ω, 1/4 Watt, 1%	402	2	R8, R10
10 μF, 35 V, 10%	7343	2	C7, C8
1 μF, 25 V +80 –20%	1206	1	C6, C1
2-position jumper	2pos_jump	2	W1, W2
3-position jumper	3pos_jump	2	W3, W4
3×2×0.1	2×3×0.1	1	J9
49.9 Ω, 1/4 Watt, 1% (not installed)	603	6	R2, R3, R4, R5, R6, R7
68 μF, 10 V, 20%, Low ESR	CAP_592D_R	2	C11, C12
Banana jack	Banana jack	3	J10, J11, J12
SMA_PCB_MT_MOD	SMA_END_50–Ω	8	J1, J2, J3, J4, J5, J6, J7, J8
SN65LVDS122	16-TSSOP(PW)	1	U1