



# GAN190-650EBE

650 V, 190 mOhm Gallium Nitride (GaN) FET in a DFN  
8 mm x 8 mm package

19 April 2023

Product data sheet

## 1. General description

The GAN190-650EBE is a general purpose 650 V, 190 mΩ Gallium Nitride (GaN) FET in a DFN 8 mm x 8 mm surface mount package. It is a normally-off e-mode device offering superior performance.

## 2. Features and benefits

- Enhancement mode - normally-off power switch
- Ultra high frequency switching capability
- No body diode
- Low gate charge, low output charge
- Qualified for standard applications
- ESD protection
- RoHS, Pb-free, REACH-compliant
- High efficiency and high power density
- Low package inductance and low package resistance

## 3. Applications

- High power density and high efficiency power conversion
- AC-to-DC converters, totem pole PFC
- DC-to-DC converters
- Fast battery charging, mobile phone, laptop, tablet and USB type-C chargers
- Datacom and telecom (AC-to-DC and DC-to-DC) converters
- Motor drives
- Solar (PV) inverters
- Class D audio amplifiers, TV PSU and LED drivers

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$-55\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-	650	V
$V_{TDS}$	transient drain to source voltage	pulsed; $t_p = 1\text{ }\mu\text{s}$ ; $\delta_{factor} = 0.01$	-	-	800	V
$I_D$	drain current	$V_{GS} = 6\text{ V}$ ; $T_{mb} = 25\text{ °C}$	[1]	-	11.5	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	125	W
$T_j$	junction temperature		-55	-	150	°C
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 6\text{ V}$ ; $I_D = 3.9\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 11</a> ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	138	190	mΩ
		$V_{GS} = 6\text{ V}$ ; $I_D = 3.9\text{ A}$ ; $T_j = 150\text{ °C}$ ; <a href="#">Fig. 11</a> ; <a href="#">Fig. 14</a>	-	300	-	mΩ

650 V, 190 mOhm Gallium Nitride (GaN) FET in a DFN 8 mm x 8 mm package

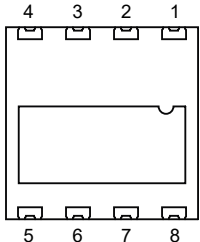
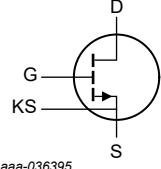
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>G</sub>	gate resistance	f = 5 MHz; T <sub>j</sub> = 25 °C; open drain	-	5	-	Ω
<b>Dynamic characteristics</b>						
Q <sub>GD</sub>	gate-drain charge	I <sub>D</sub> = 3.9 A; V <sub>DS</sub> = 400 V; V <sub>GS</sub> = 6 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 15</a> ; <a href="#">Fig. 16</a>	-	1.1	-	nC
Q <sub>G(tot)</sub>	total gate charge		-	2.8	-	nC
Q <sub>OSS</sub>	output charge	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 400 V; T <sub>j</sub> = 25 °C	[2]	24.5	-	nC

[1] Limited by device saturation

[2] Q<sub>r</sub> is not specified separately from Q<sub>OSS</sub> for e-mode GaN FETs, since Q<sub>r</sub> = Q<sub>OSS</sub> + Q<sub>D</sub>, and Q<sub>D</sub> = 0. (Q<sub>D</sub> is charge associated with diffusion of minority carriers. Since there is no body diode, no minority carriers in excess of Q<sub>OSS</sub> have to be transferred for e-mode GaN FETs.)

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 <p>Transparent top view</p> <p><b>DFN8080-8 (SOT8074-1)</b></p>	 <p>aaa-036395</p>
2	D	drain		
3	D	drain		
4	D	drain		
5	S	source		
6	S	source		
7	KS	kelvin source		
8	G	gate		
mb	S	mounting base; connected to source		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
GAN190-650EBE	DFN8080-8	plastic thermal enhanced small outline package; no leads; 8 terminals; body: 8 x 8 x 0.9 mm	SOT8074-1

## 7. Marking

Table 4. Marking codes

Type number	Marking code
GAN190-650EBE	190IEBE

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). T<sub>j</sub> = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	-55 °C ≤ T <sub>j</sub> ≤ 150 °C	-	650	V

650 V, 190 mOhm Gallium Nitride (GaN) FET in a DFN 8 mm x 8 mm package

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>TDS</sub>	transient drain to source voltage	pulsed; t <sub>p</sub> = 1 μs; δ <sub>factor</sub> = 0.01	-	800	V
V <sub>GS</sub>	gate-source voltage		-1.4	7	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; Fig. 1	-	125	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 6 V; T <sub>mb</sub> = 25 °C	[1]	11.5	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; Fig. 2	[1]	20.5	A
T <sub>stg</sub>	storage temperature		-55	150	°C
T <sub>j</sub>	junction temperature		-55	150	°C
T <sub>slid(M)</sub>	peak soldering temperature		-	260	°C

[1] Limited by device saturation

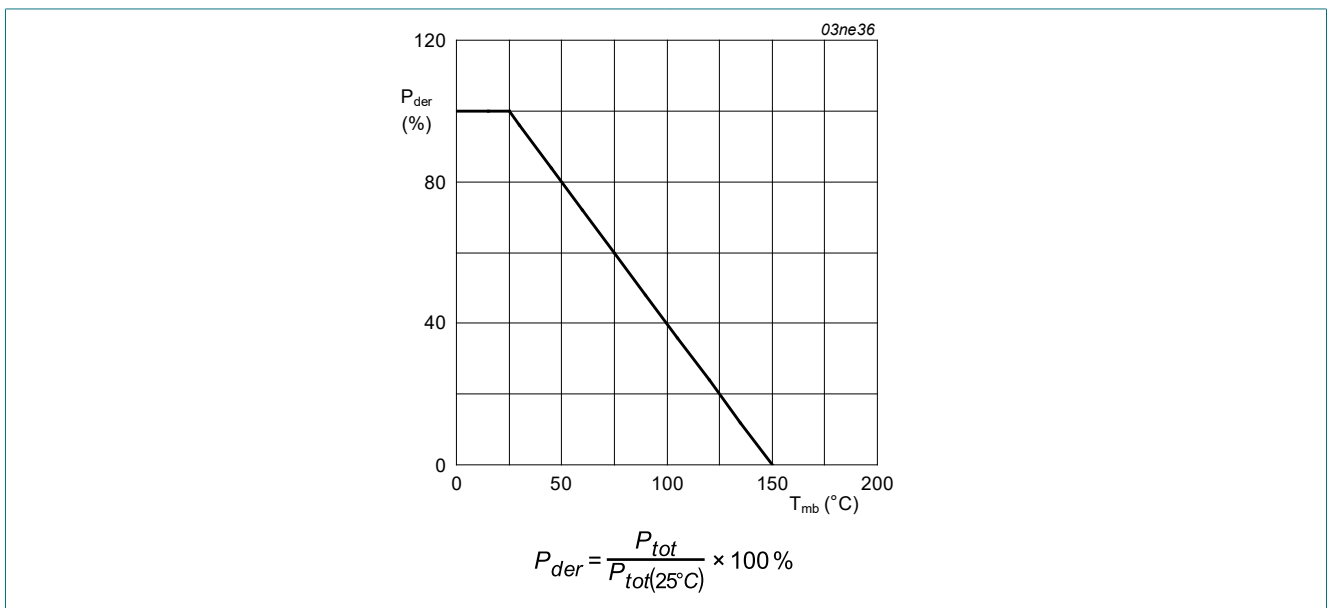


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

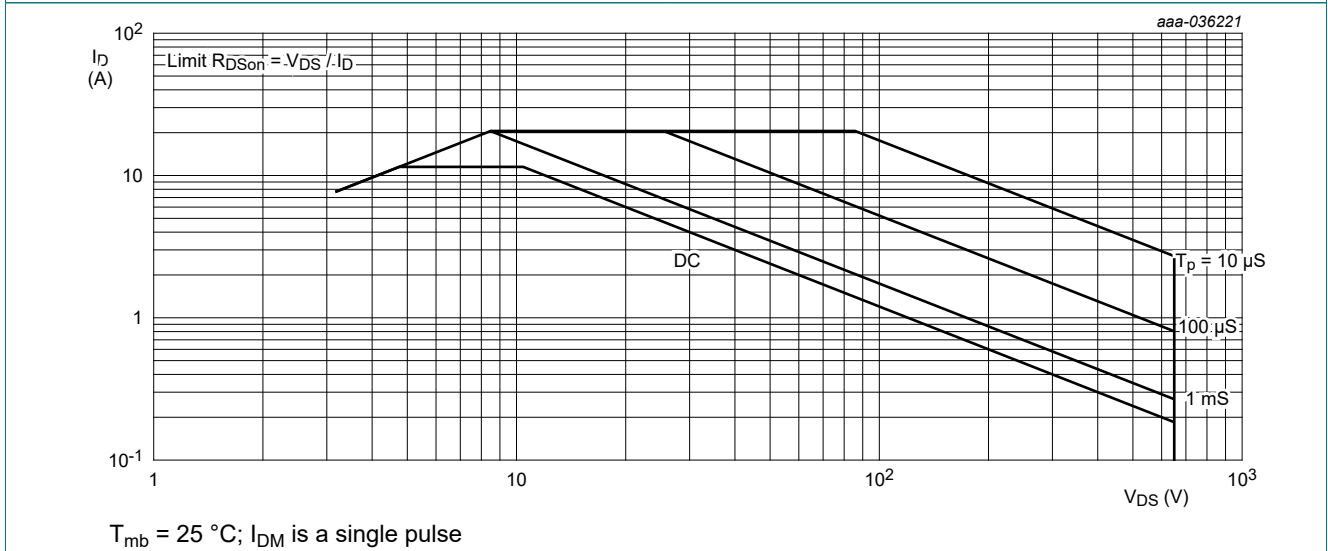


Fig. 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	<a href="#">Fig. 3</a>	-	-	1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	-	35.9	K/W

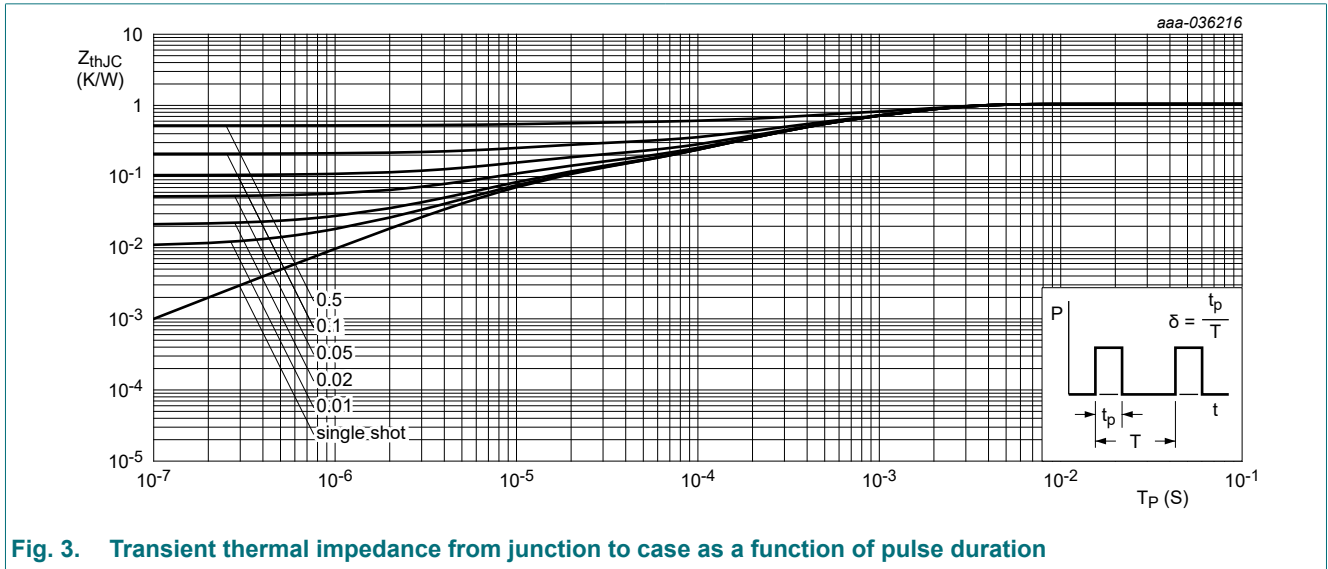


Fig. 3. Transient thermal impedance from junction to case as a function of pulse duration

## 10. Characteristics

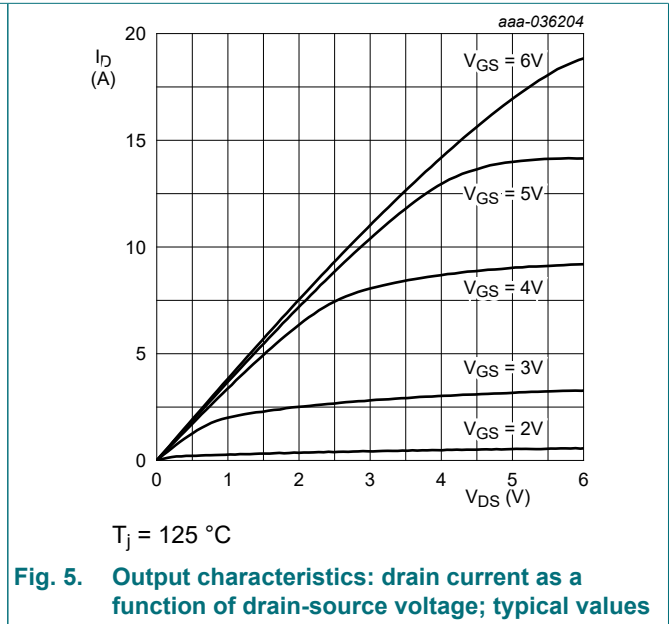
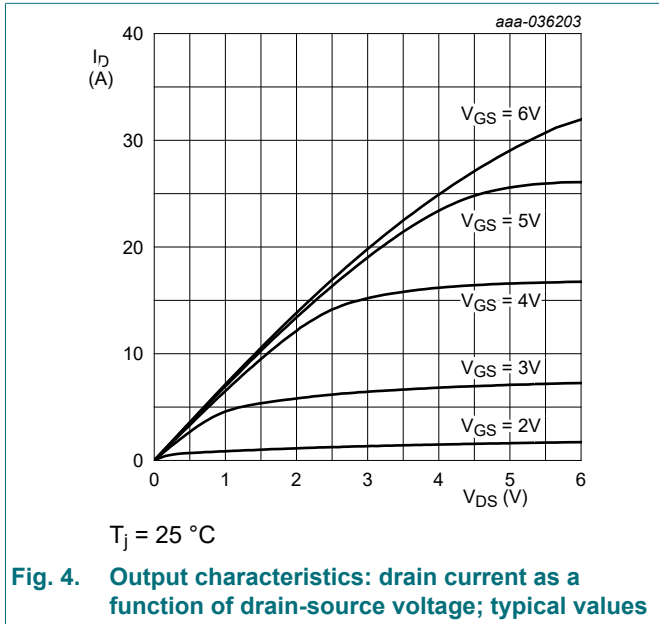
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 12.2 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 8</a>	1.2	1.7	2.5	V
		$I_D = 12.2 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ <a href="#">Fig. 8</a>	-	1.7	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 650 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 9</a>	-	0.45	20	$\mu\text{A}$
		$V_{DS} = 650 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C};$ <a href="#">Fig. 9</a>	-	6	-	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 6 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 10</a>	-	60	-	$\mu\text{A}$
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 6 \text{ V}; I_D = 3.9 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 11; Fig. 12; Fig. 13</a>	-	138	190	m $\Omega$
		$V_{GS} = 6 \text{ V}; I_D = 3.9 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ <a href="#">Fig. 11; Fig. 14</a>	-	300	-	m $\Omega$
$R_G$	gate resistance	$f = 5 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C};$ open drain	-	5	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 3.9 \text{ A}; V_{DS} = 400 \text{ V}; V_{GS} = 6 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 15; Fig. 16</a>	-	2.8	-	nC
$Q_{GS}$	gate-source charge		-	0.25	-	nC
$Q_{GD}$	gate-drain charge		-	1.1	-	nC

650 V, 190 mOhm Gallium Nitride (GaN) FET in a DFN 8 mm x 8 mm package

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 3.9\text{ A}$ ; $V_{DS} = 400\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 15</a>	-	2.2	-	V
$C_{iss}$	input capacitance	$V_{DS} = 400\text{ V}$ ; $V_{GS} = 0\text{ V}$ ; $f = 100\text{ kHz}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 17</a>	-	96	-	pF
$C_{oss}$	output capacitance		-	30	-	pF
$C_{rss}$	reverse transfer capacitance		-	0.5	-	pF
$C_{o(er)}$	effective output capacitance, energy related	$0\text{ V} \leq V_{DS} \leq 400\text{ V}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 18</a>	[1]	43	-	pF
$C_{o(tr)}$	effective output capacitance, time related	$0\text{ V} \leq V_{DS} \leq 400\text{ V}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$	[2]	60	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 400\text{ V}$ ; $V_{GS} = 6\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; $I_D = 8\text{ A}$ ; $L = 318\text{ }\mu\text{H}$ ; $R_{on} = 10\text{ }\Omega$ ; $R_{off} = 2\text{ }\Omega$ ; <a href="#">Fig. 19</a> ; <a href="#">Fig. 20</a>	-	1.4	-	ns
$t_r$	rise time		-	4	-	ns
$t_{d(off)}$	turn-off delay time		-	1.7	-	ns
$t_f$	fall time		-	4	-	ns
$Q_{oss}$	output charge	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 400\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$	[3]	24.5	-	nC
<b>Source-drain characteristics</b>						
$V_{SD}$	source-drain voltage	$I_S = 3.9\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 21</a> ; <a href="#">Fig. 22</a> ; <a href="#">Fig. 23</a> ; <a href="#">Fig. 24</a>	-	2.6	-	V

- [1]  $C_{O(er)}$  is the fixed capacitance that gives the same stored energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 400 V
- [2]  $C_{O(tr)}$  is the fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 400 V
- [3]  $Q_r$  is not specified separately from  $Q_{oss}$  for e-mode GaN FETs, since  $Q_r = Q_{oss} + Q_D$ , and  $Q_D = 0$ . ( $Q_D$  is charge associated with diffusion of minority carriers. Since there is no body diode, no minority carriers in excess of  $Q_{oss}$  have to be transferred for e-mode GaN FETs.)



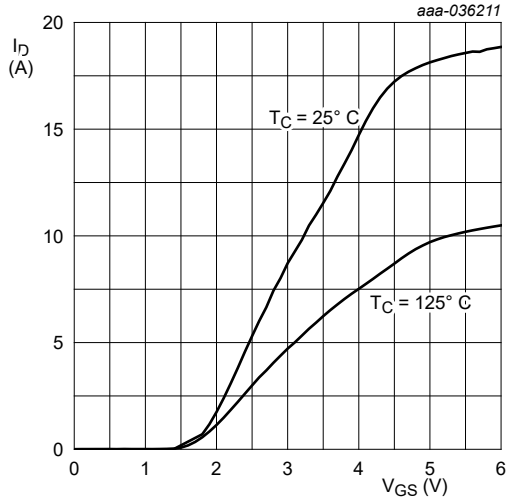
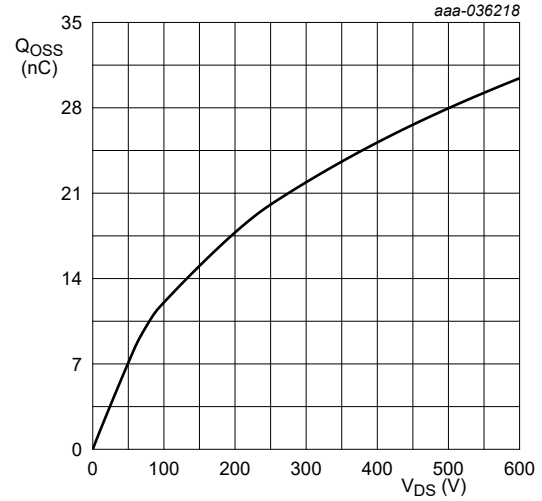
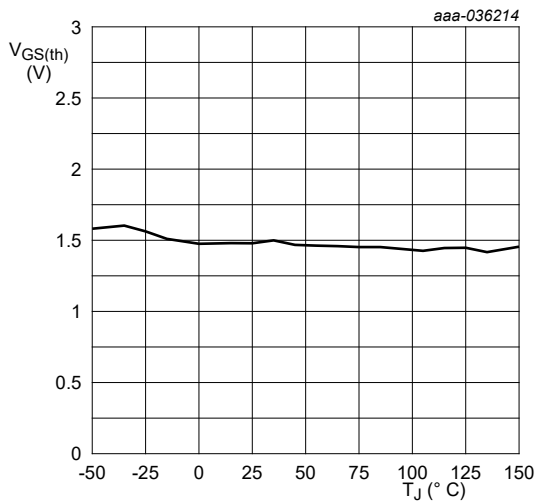


Fig. 6. Transfer characteristics; drain current as a function of gate-source voltage; typical values



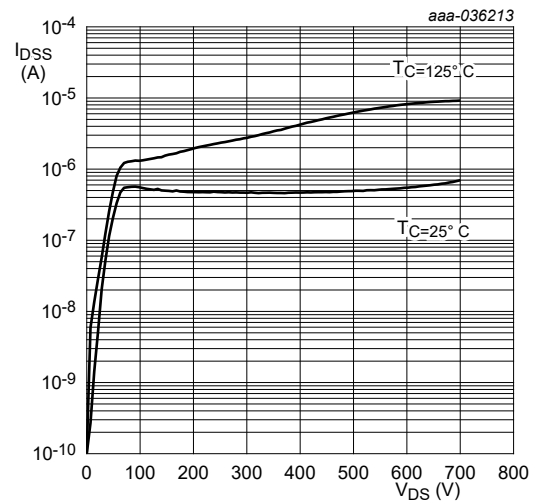
Freq. = 100 kHz

Fig. 7. Output charge as a function of drain-source voltage; typical values



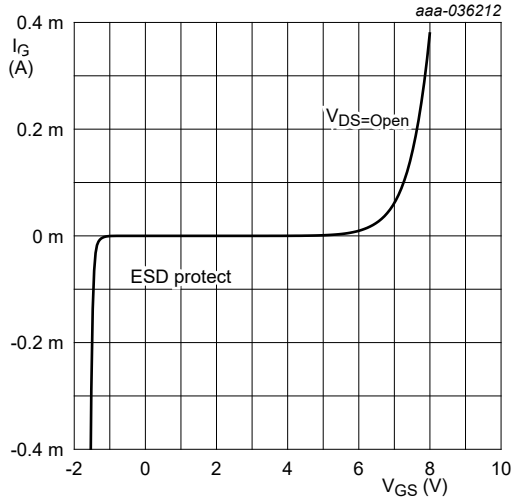
$I_D = 12.2\text{ mA}$  ;  $V_{DS} = V_{GS}$

Fig. 8. Gate-source threshold voltage as a function of junction temperature



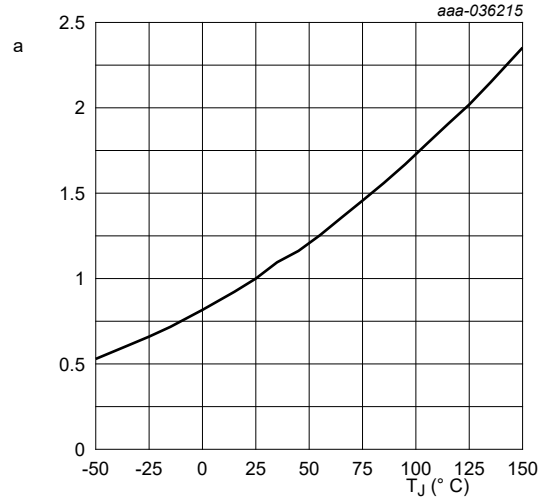
$V_{GS} = 0\text{ V}$

Fig. 9. Drain-source current as a function of drain-source voltage; typical values



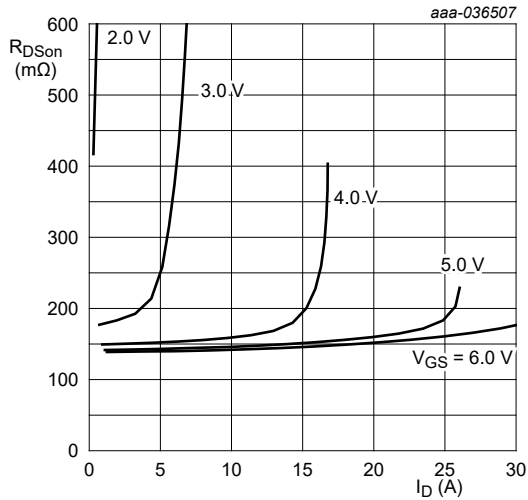
$I_g$  reverse turn on by ESD unit

Fig. 10. Gate-source current as a function of gate-source voltage; typical values



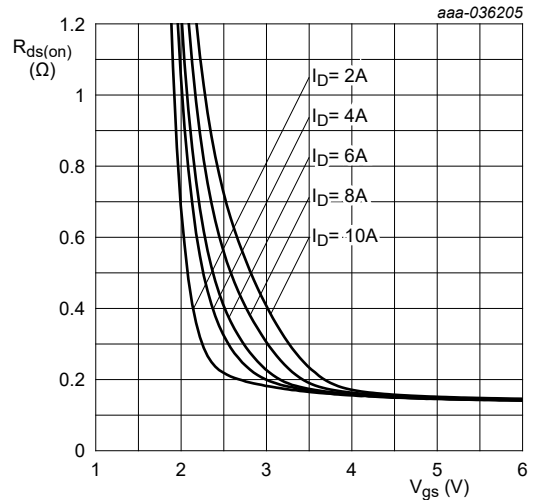
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ C)}$$

Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^\circ C$

Fig. 12. Drain-source on-state resistance as a function of drain current ; typical values



$T_j = 25^\circ C$

Fig. 13. Drain-source on-state resistance as a function of gate-source voltage; typical values

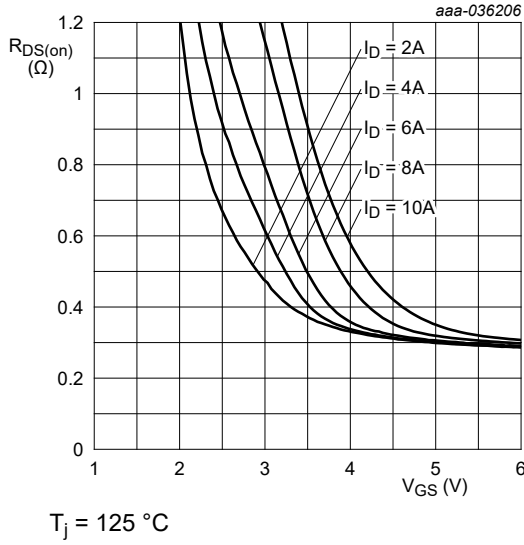


Fig. 14. Drain-source on-state resistance as a function of gate-source voltage; typical values

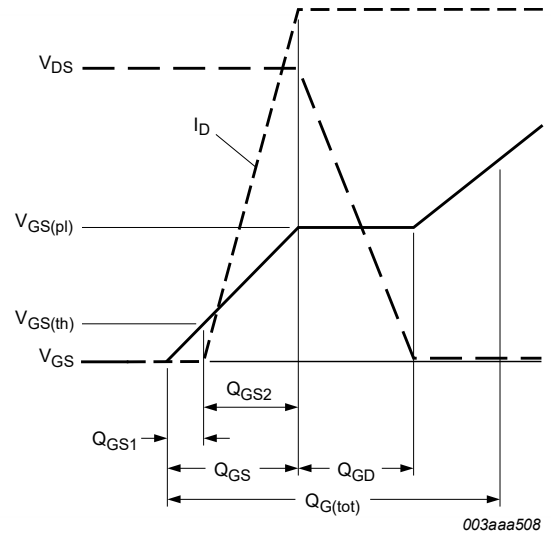


Fig. 15. Gate charge waveform definitions

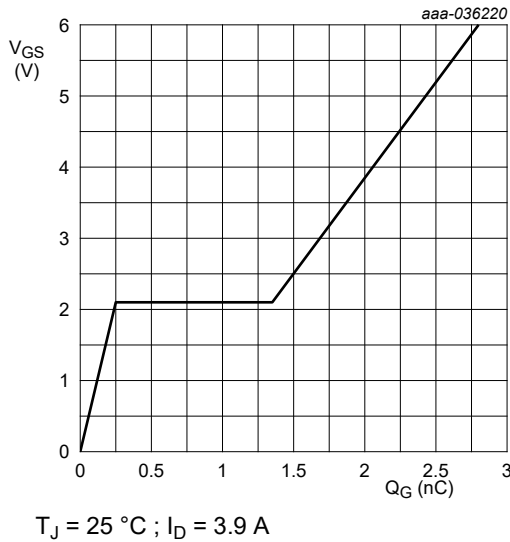


Fig. 16. Gate-source voltage as a function of gate charge; typical values

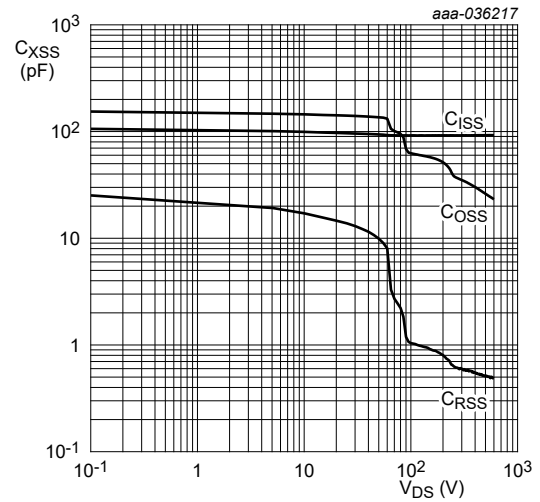
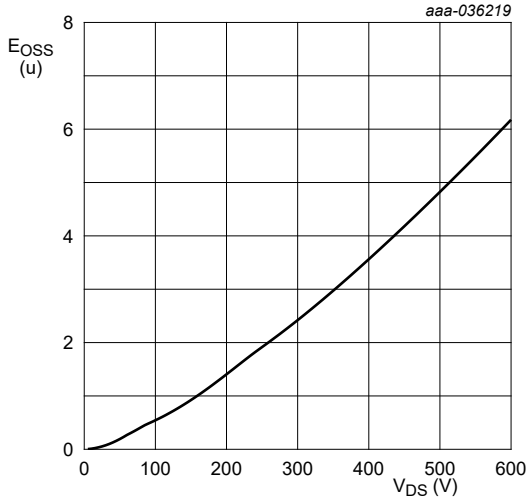


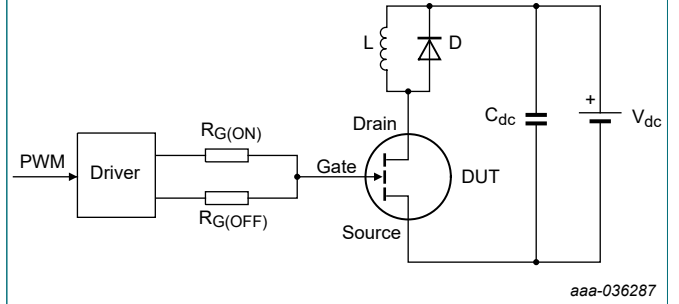
Fig. 17. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values





Freq. = 100 kHz

Fig. 18. COSS stored energy as a function of drain-source voltage; typical values



V<sub>DS</sub> = 400 V; I<sub>D</sub> = 10 A; L = 318 μH; V<sub>GS</sub> = 6 V;  
R<sub>on</sub> = 10 Ω; R<sub>off</sub> = 2 Ω

Fig. 19. Typical switching times with inductive load

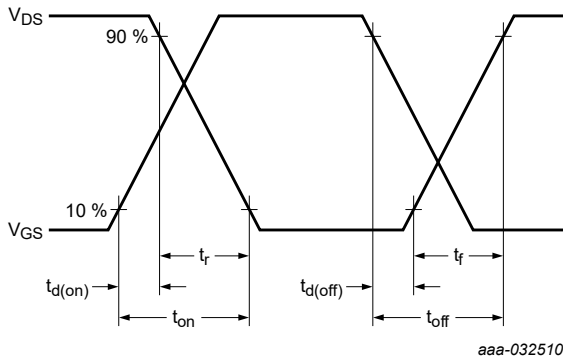
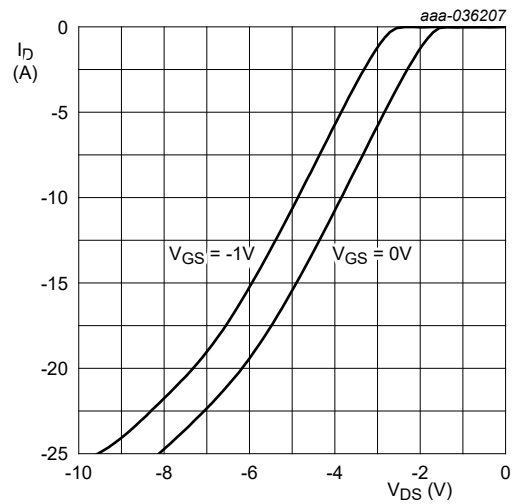


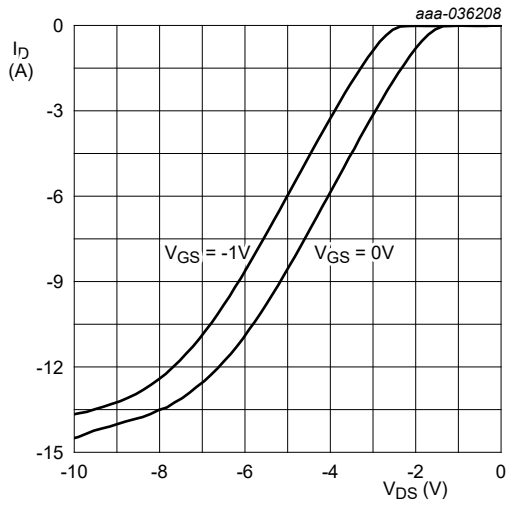
Fig. 20. Switching time waveform



T<sub>j</sub> = 25 °C

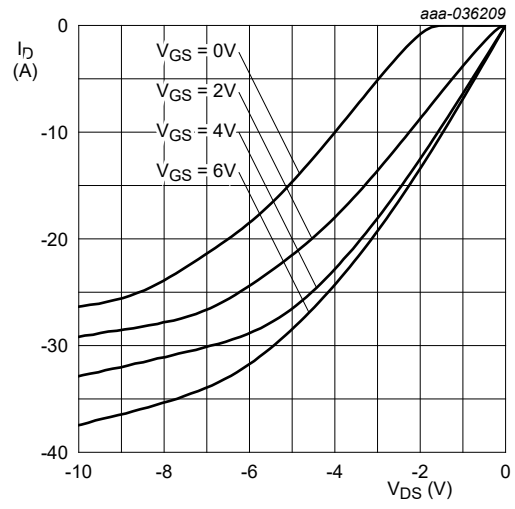
Fig. 21. Source current as a function of source-drain voltage; typical values

650 V, 190 mOhm Gallium Nitride (GaN) FET in a DFN 8 mm x 8 mm package



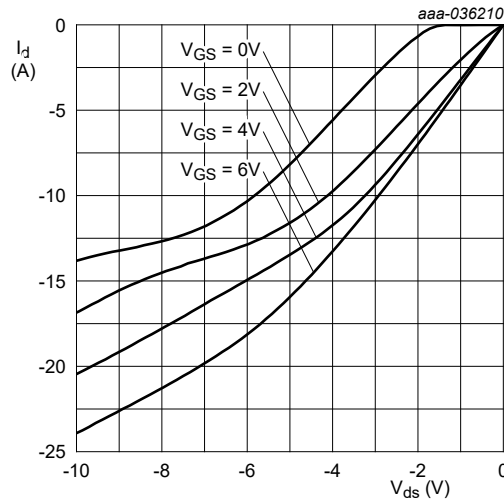
$T_j = 125\text{ °C}$

Fig. 22. Source current as a function of source-drain voltage; typical values



$T_j = 25\text{ °C}$

Fig. 23. Source current as a function of source-drain voltage; typical values



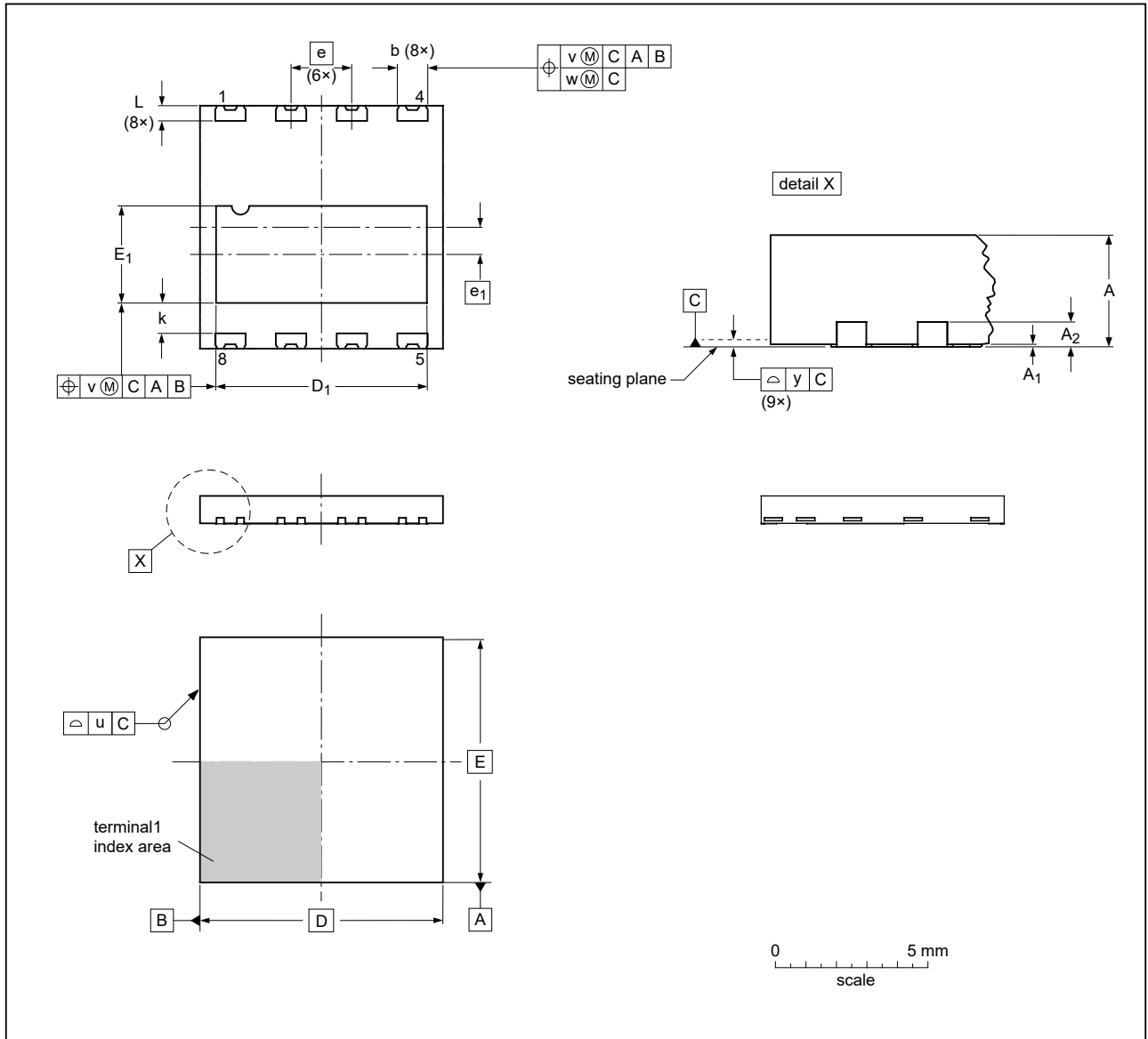
$T_j = 125\text{ °C}$

Fig. 24. Source current as a function of source-drain voltage; typical values

### 11. Package outline

DFN8080-8: plastic thermal enhanced small outline package; no leads; 8 terminals; body: 8 × 8 × 0.9 mm

SOT8074-1



Dimensions (mm are the original dimensions)

Unit	A	A <sub>1</sub>	A <sub>2</sub>	b	D	D <sub>1</sub>	E	E <sub>1</sub>	e	e <sub>1</sub>	k	L	y	u	v	w
max	1.0	0.05	0.203	1.05	8	7.04	8	3.3	2	0.9	1	0.6	0.1	0.1	0.1	0.05
nom	0.9	0.02	REF	1.00	BSC	6.94	BSC	3.2	BSC	BSC	REF	0.4				
min	0.8	0.00		0.92		6.84		3.1								

sot8074-1\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT8074-1		MO-229 compatible			23-03-03

Fig. 25. Package outline DFN8080-8 (SOT8074-1)

## 12. Soldering

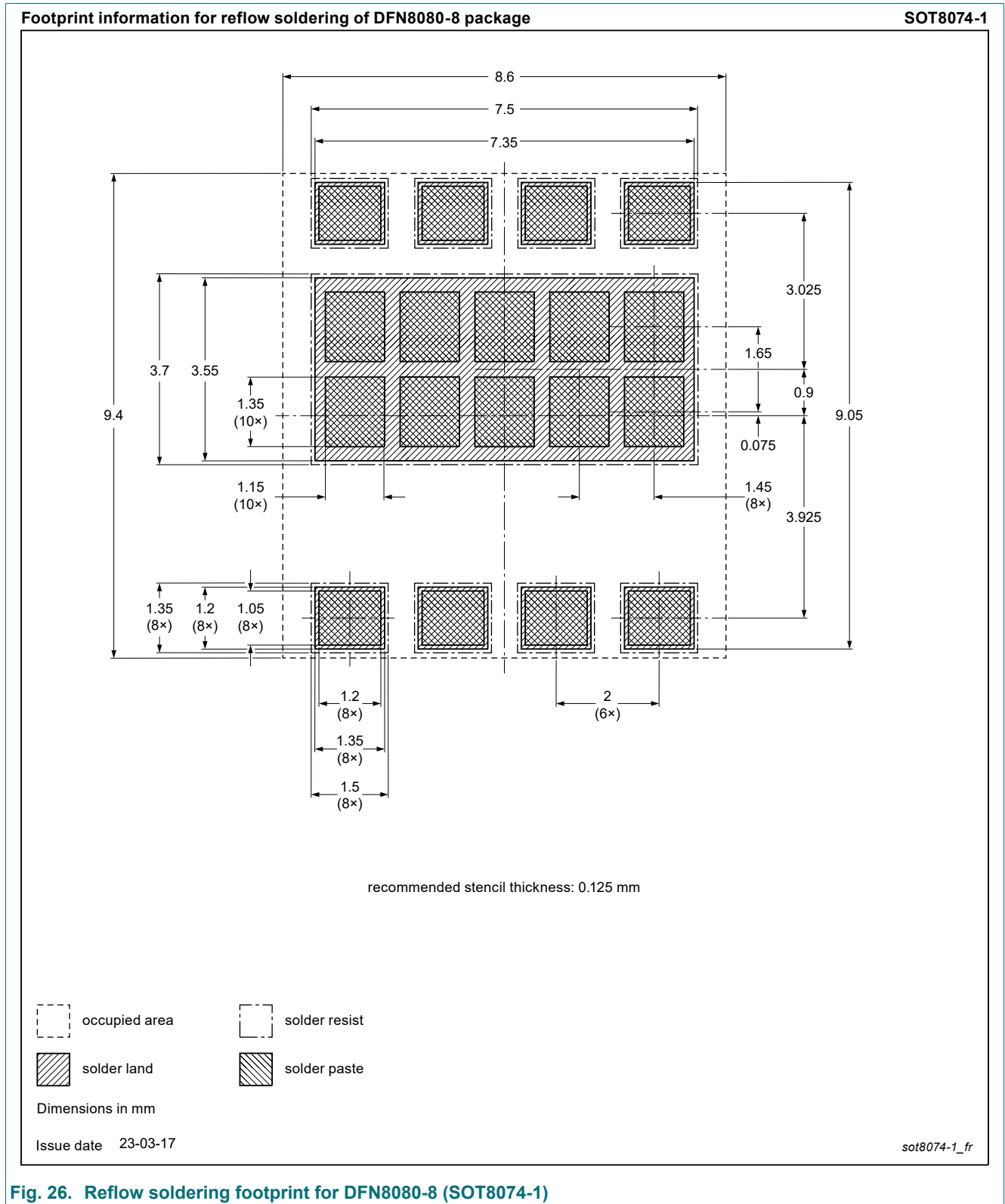


Fig. 26. Reflow soldering footprint for DFN8080-8 (SOT8074-1)

## 13. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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