

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

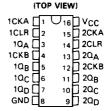
- '390, 'LS390 . . . Individual Clocks for A and B Flip-Flops Provide Dual ÷ 2 and ÷ 5 Counters
- '393, 'LS393 . . . Dual 4-Bit Binary Counter with Individual Clocks
- All Have Direct Clear for Each 4-Bit Counter
- **Dual 4-Bit Versions Can Significantly Improve** System Densities by Reducing Counter Package Count by 50%
- Typical Maximum Count Frequency . . . 35 MHz
- **Buffered Outputs Reduce Possibility of Collector** Commutation

description

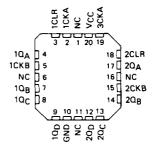
Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The '390 and 'LS390 incorporate dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The '393 and 'LS393 each comprise two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The '390, 'LS390, '393, and 'LS393 have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

Series 54 and Series 54LS circuits are characterized for operation over the full military temperature range of -55°C to 125°C: Series 74 and Series 74LS circuits are characterized for operation from 0°C to 70°C.

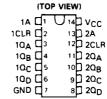
SN54390, SN54LS390 . . . J OR W PACKAGE SN74390 . . . N PACKAGE SN74LS390 . . . D OR N PACKAGE



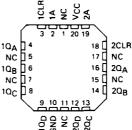
SN54LS390 . . . FK PACKAGE (TOP VIEW)



SN54393, SN54LS393 . . . J OR W PACKAGE **SN74393...N PACKAGE** SN74LS393 . . . D OR N PACKAGE



SN54LS393 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

INSTRUMENTS

PRODUCTION DATA documents contain information PHUDUCTUM ALL ADCUMENTS CONTAIN INFORMATION COURSELS OF PUBLICATION date. Products conform to appecifications per the terms of Texas Instruments standard warranty. Production processing does not nacessarily include testing of all parameters.

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

'390, 'LS390 **BCD COUNT SEQUENCE** (EACH COUNTER) (See Note A)

			-	
COUNT		OUT	PUT	
COUNT	a_{D}	σc	σB	QA
0	L	L	L	L
1	L	L	L	Н
2	L	L	н	L
3	L	L	Н	Н
4	L	Н	L	L
5	L	н	L	Н
6	L	н	н	L
7	L	н	Н	н
8	н	L	L	L
9	н	L	L	Н

FUNCTION TABLES '390, 'LS390 BI-QUINARY (5-2) (EACH COUNTER) (See Note B)

COUNT		OUT	PUT	
COUNT	۵A	σ_{D}	α_{C}	αB
0	L	L	L	L
1	Ł	L	L	Н
2	L	L	Н	L
3	Ļ	L	Н	Н
4	L	Н	L	L
5	н	L	L	L
6	н	L	L	Н
7	Н	L	Н	L
8	н	L	н	н
9	н	н	Ļ	Ļ

'393, 'LS393 COUNT SEQUENCE (EACH COUNTER)

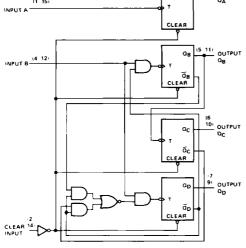
COUNT		OUT	PUT	
COOM	αD	αc	αB	QA
0	L	F	L	L
1	L	L	L,	н
2	L	L	н	L
3	L	L	н	н
4	L	н	L	L
5	L	н	L	н
6	L	н	н	L
7	L	н	Н	н
8	н	L	L	L
9	н	L,	L	н
10	н	L	н	L
11	н	L	н	Н
12	н	H	L	L
13	н	Н	L	н
14	н	н	н	L
15	Ι	Н	н	н

- NOTES A. Output QA is connected to input B for BCD count.
 - B. Output QD is connected to input A for bi-quinary
 - count.

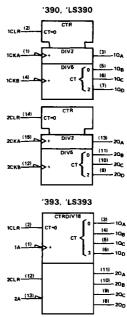
 C. H = high level, L = low level.

logic diagrams (positive logic)

1390, LS390 13 13) OUTPUT OΑ



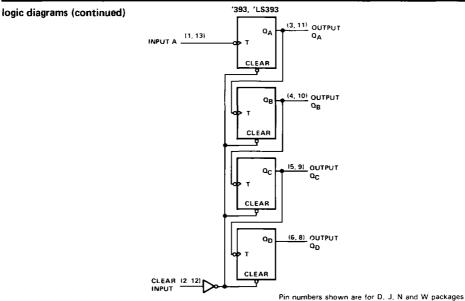
logic symbols†



 $^\dagger \text{These symbols are in accordance with ANSI/IEEE Std. 91-1984}$ and IEC Publication 617-12.

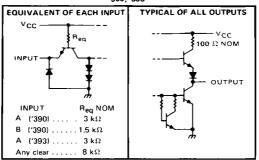
Pin numbers shown are for D, J, N, and W packages.

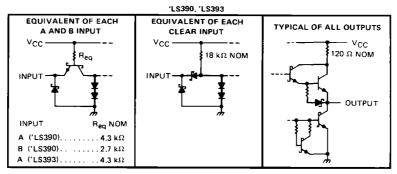




schematics of inputs and outputs

'390, '393







SN54390, SN54393, SN74390, SN74393 DUAL 4-BIT DECADE AND BINARY COUNTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)								7 V	
Input voltage								5.5 V	
Operating free-air temperature range:	SN54390, SN54393							-55°C to 125°C	
	SN74390, SN74393							. 0°C to 70°C	
Storage temperature range								65°C to 150°C	

NOTE 1: Voltage values are with respect to network ground terminal

recommended operating conditions

			SN5439 SN5439	-		SN7439 SN7439		UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	1
Supply voltage, V _{CC}		4.5	5	5.5	4.75	5	5.25	٧
High-level output current, IOH				-800			-800	μА
Low-level output current, IOL				16			16	mA
Count for guess &	A input	0		25	0		25	MHz
Count frequency, f _{count}	B input	0		20	0		20	WIHZ
	A input high or low	20			20			
Pulse width, t _W	B input high or low	25			25			ns
	Clear high	20			20			1
Clear inactive-state setup time, t _{su}	·	25:			25↓			ns
Operating free-air temperature, TA		-55		125	0		70	,C

¹ The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	240445750		7707.001			'390			′393		
	PARAMETER		TEST CON	IDITIONS†	MIN	TYP‡	MAX	MIN	TYP [‡]	MAX	UNIT
V _{1H}	High-level input voltage				2			2			ν
VIL	Low-level input voltage						8.0			0.8	V
Vik	Input clamp voltage		V _{CC} = MIN,	I ₁ = -12 mA			-1.5			-1.5	V
νон	High-level output voltage		V _{CC} = MIN, V _{IL} = 0.8 V,	V _{IH} = 2 V, I _{OH} = -800 μA	2.4	3.4		2.4	3.4		٧
VOL	Low-level output voltage		V _{CC} = MIN, V _{IL} = 0.8 V,	V _{IH} = 2 V,		0.2	0.4		0.2	0.4	V
t _j	Input current at maximum input voltage		V _{CC} = MAX,	V _I = 5.6 V			1			1	mA
		Clear		·			40			40	
ΉН	High-level input current	Input A	V _{CC} = MAX,	V! = 2.4 V			80			80	μА
		Input B					120				1
		Clear					-1			-1	
I _{IL}	Low-level input current	Input A	VCC = MAX,	V _I = 0.4 V			-3.2			-3.2	mA
		Input B					-4.8				Ī
1	Chart area to a series area &		V 144 V	SN54'	-20		-57	-20		-57	
los	Short-circuit output current §		V _{CC} = MAX	SN74'	-18		-57	18		-57	mA
Icc	Supply current		VCC = MAX,	See Note 2		42	69		38	64	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2. ICC is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \text{ °C}$

[§] Not more than one output should be shorted at a time.

The Q_A outputs of the '390 are tested at I_{OL} = 16 mA plus the limit value for I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability

SN54390, SN54393, SN74390, SN74393 DUAL 4-BIT DECADE AND BINARY COUNTERS

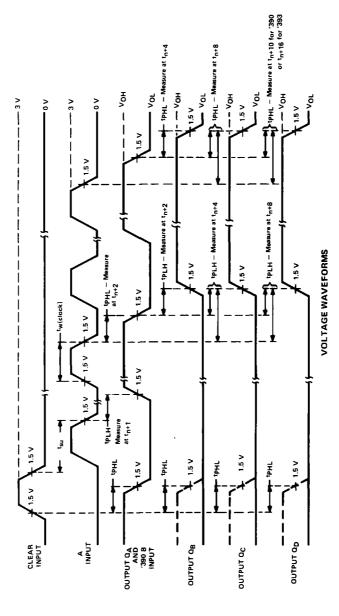
switching characteristics, VCC = 5 V, TA = 25°C

PARAMETER	FROM	TO	TEST CONDITIONS		'390			'393		UNIT
PARAMETER	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
	_A	Q _A		25	35		25	35		MHz
fmax	В	QΒ		20	30					WITZ
tPLH	А	0.			12	20		12	_ 20	ns
tPHLtPHL	l ^	Q _A			13	20		13	20	
tPLH	Α	OC of ,380	C _L = 15 pF,		37	60		40	60	ns
t _{PHL}] ^	Q _D of '393	$R_L = 400 \Omega$,		39	60		40	60	115
^t PLH	В	0-	See Note 3		13	21				
tPHL	В	σB	and		14	21				ns
tPLH .	В	- 0-	Figure 1		24	39				
tpHL	}	Ωc			26	39				ns
^t PLH	В	Q _D			13	21				ns
tpHL_	<u> </u>	⁴ b			14	21				.,,
tPHL.	Clear	Any			24	39		24	39	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



PARAMETER MEASUREMENT INFORMATION



NOTE A' Input pulses are supplied by a generator having the following characteristics t, < 5 ns, t₁ < 5 ns, PRB = 1 MHz, duty cycle = 50%, Z_{out} > 50 ohms.

FIGURE 1

Texas 🏰 Instruments

SN54LS390, SN54LS393, SN74LS390, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS

absolute maximum ratings over operating free-air temp	erature range (unless otherwise noted)
Supply voltage, VCC (see Note 1)	
Clear input voltage	
Any A or B clock input voltage	
Operating free-air temperature range: SN54LS390, SN54L	LS393
SN74LS390, SN74L	-\$393 0°C to 70°C
Storage temperature range	
NOTE 1 Voltage values are with respect to network ground terminal.	

recommended operating conditions

			N54LS:				5 5.25 -400 8 25 12.5	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}		4.5	5	5.5	4.75	5	5.25	٧
High-level output current, IOH				-400			-400	μΑ
Low-level output current, IOL				4			8	mA
Count fragues	A input	0		25	0		25	
Count frequency, fcount	B input	0		12.5	0		12.5	MHz
	A input high or low	20			20			
Pulse width, t _W	B input high or low	40			40			ns
	Clear high	20			20			
Clear inactive-state setup time, t _{SU}		251			25↓			ns
Operating free-air temperature, TA		-55		125	0		70	,C

The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

							SN54L	s'		SN74L	S'	ในพา
	PARAMETER		1 1 1 2	T CONDITIONS		MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage					2			2			V
VIL	Low-level input voltage							07			0.8	٧
Vik	Input clamp voltage		VCC = MIN,	I _I = -18 mA				-15			-1.5	V
νон	High-level output voltage		V _{CC} = MIN, V _{IL} = V _{IL} max,	V _{IH} = 2 V, I _{OH} = -400 μA	-	2.5	3.4		2.7	34		V
			V _{CC} = MIN,	V _{IH} = 2 V,	IOL = 4 mA		0 25	0 4		0 25	0.4	V
VOL	Low-level output voltage		V _{IL} ≈ 0.8 V,		IOL = 8 mA					0 35	0.5	1 °
	Input current at	Clear			V ₁ = 7 V			0.1			0.1	
t ₁	·	Input A	VCC = MAX		V _I = 55 V	L		02			0.2	mA.
	maximum input voltage	Input B			V[-55V			0 4			0 4	۱ <u>^</u>
		Clear	_					0 02			0.02	
ίн	High-level input current	Input A	V _{CC} = MAX,	V+ = 2.7 V				0.1			0 1	mΑ
		Input B	•					0.2			0.2	
		Clear						-04			-0 4	
I _I L	Low-level input current	Input A	V _{CC} = MAX,	V1 = 0.4 V		L		1.6			-1.6	mA
		Input B						2.4			-2 4	}
los	Short-circuit output curi	rent ^S	V _{CC} = MAX			-20		-100	-20		100	mA
	Complex oursess	_	VCC = MAX,		'LS390		15	26		15	26	mA
ICC	Supply current		See Note 2		'LS393		15	26		15	26] '''^

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

NOTE 2: ICC is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second

¹ The QA outputs of the 'LS390 are tested at IQL = MAX plus the limit value for I_{IL} for the clock B input. This permits driving the clock B input while maintaining full fan-out capability.

SN54LS390, SN54LS393, SN74LS390, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS

switching characteristics, VCC = 5 V, TA = 25°C

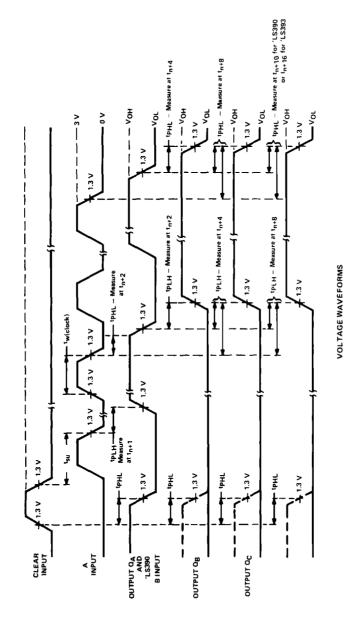
	FROM	то			'LS390	i		'LS393		l <u>.</u>
PARAMETER	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
	Α	QΑ		25	35		25	35		MHz
f _{max}	В	ΩB		12.5	20					MHZ
^t PLH	Α .	0.			12	20		12	20	
^t PHL	1 ~	QΑ			13	20		13	20	ns
tPLH	A	Q _C of 'LS390	CL = 15 pF,		37	60	[40	60	
tPHL .	1_^	Q _D of 'L\$393	R _L = 2 kΩ,		39	60		40	60	ns
^t PLH	В	ΩB	See Note 4 and Figure 2		13	21				ns
[†] PHL	1	_ _ B			14	21] ''`
tPLH	В	QC			24	39				
tPHL	1 °	^{QC}			26	39				ns
tPLH	В	0-			13	21				ns
tPHL.	1	α _D			14	21				
[†] PHL	Clear	Any			24	39		24	39	ns

NOTE 4: Load circuits and voltage waveforms are shown in Section 1



FIGURE 2

PARAMETER MEASUREMENT INFORMATION



NOTE A: Input pulses are supplied by a generator having the following characteristics ty:: 15 ns, ty" 6 ns, PRR = 1 MHz, duty cycle = 50 %,

Texas VI