AK5365

24-Bit 96kHz ΔΣ ADC with Selector/PGA/ALC

GENERAL DESCRIPTION

AK5365 is a high-performance 24-bit, 96kHz sampling ADC for consumer audio and digital recording applications. Thanks to AKM's Enhanced Dual-Bit modulator architecture, this analog-to-digital converter has an impressive dynamic range of 103dB with a high level of integration. The AK5365 has a 5-channel stereo input selector, an input Programmable Gain Amplifier with an ALC function. All this integration with high-performance makes the AK5365 well suited for CD and DVD recording systems.

FEATURES

1. 24bit Stereo ADC
- **5ch Stereo Inputs Selector**
- **Input PGA from +12dB to 0dB, 0.5dB Step**
- **Auto Level Control (ALC) Circuit**
- **Digital HPF for offset cancellation (fc=1.0Hz@fs=48kHz)**
- **Digital Attenuator**
- **Soft Mute**
- **Single-end Inputs**
- **S/(N+D) : 94dB**
- **DR, S/N : 103dB**
- **Audio I/F Format : 24bit MSB justified, I^2S**

2. 3-wire Serial μP Interface / I^2C-Bus

3. Master / Slave Mode

4. Master Clock : 256fs/384fs/512fs

5. Sampling Rate : 32kHz to 96kHz

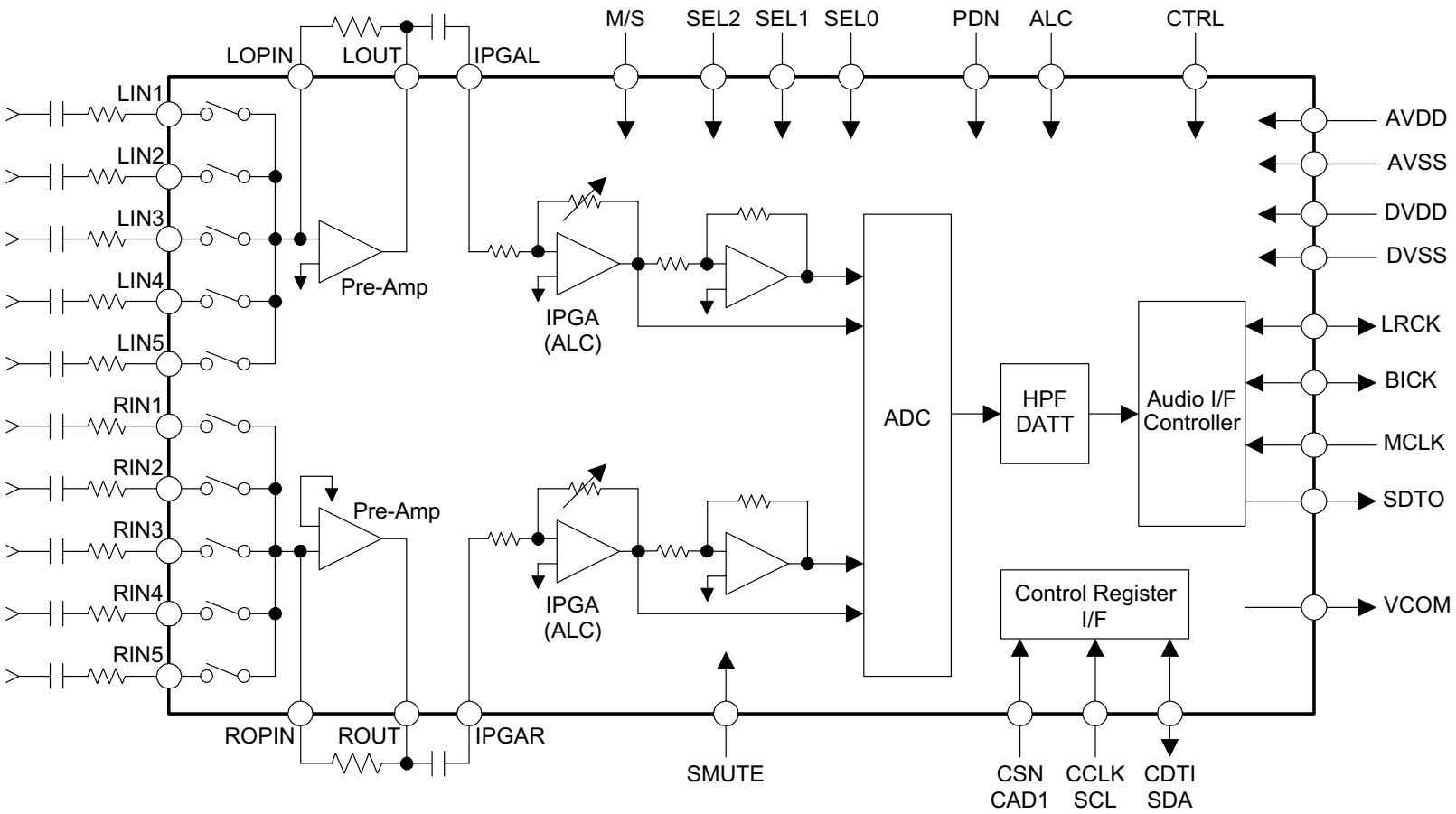
6. Power Supply
- **AVDD: 4.75 ~ 5.25V (typ. 5.0V)**
- **DVDD: 3.0 ~ 5.25V (typ. 3.3V)**

7. Power Supply Current : 27mA

8. Ta = -40 ~ 85°C

9. Package : 44pin LQFP

■ Block Diagram

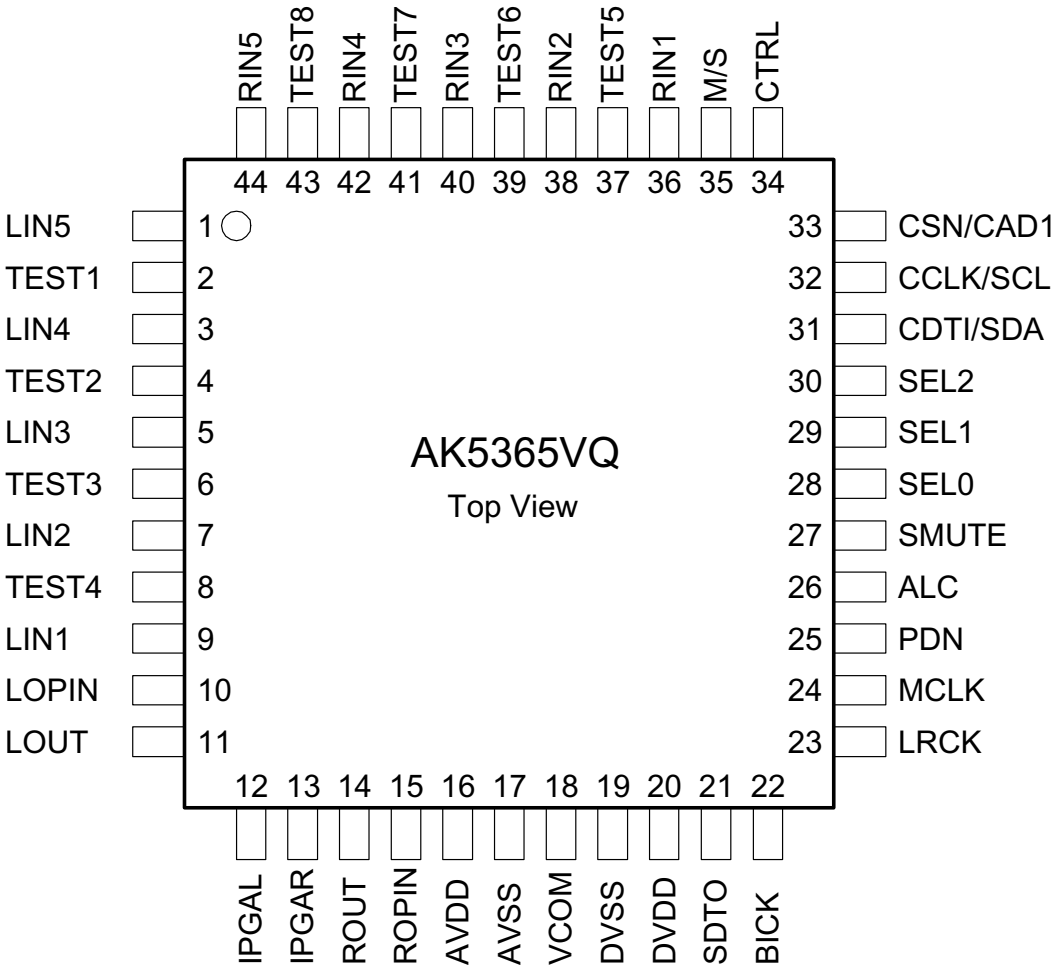


Block diagram

■ Ordering Guide

AK5365VQ	–40 ~ +85°C	44pin LQFP (0.8mm pitch)
AKD5365	Evaluation Board for AK5365	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	LIN5	I	Lch Analog Input 5 Pin
2	TEST1	I	Test 1 Pin (Connected to AVSS)
3	LIN4	I	Lch Analog Input 4 Pin
4	TEST2	I	Test 2 Pin (Connected to AVSS)
5	LIN3	I	Lch Analog Input 3 Pin
6	TEST3	I	Test 3 Pin (Connected to AVSS)
7	LIN2	I	Lch Analog Input 2 Pin
8	TEST4	I	Test 4 Pin (Connected to AVSS)
9	LIN1	I	Lch Analog Input 1 Pin
10	LOPIN	I	Lch Feed Back Resistor Input Pin
11	LOUT	O	Lch Feed Back Resistor Output Pin
12	IPGAL	I	Lch IPGA Input Pin
13	IPGAR	I	Rch IPGA Input Pin
14	ROUT	O	Rch Feed Back Resistor Output Pin
15	ROPIN	I	Rch Feed Back Resistor Input Pin
16	AVDD	-	Analog Power Supply Pin, 4.75 ~ 5.25V
17	AVSS	-	Analog Ground Pin
18	VCOM	O	Common Voltage Output Pin, AVDD/2 Bias voltage of ADC input.
19	DVSS	-	Digital Ground Pin
20	DVDD	-	Digital Power Supply Pin, 3.0 ~ 5.25V
21	SDTO	O	Audio Serial Data Output Pin
22	BICK	I/O	Audio Serial Data Clock Pin

Note: All digital input pins except pull-down pins should not be left floating.
Note: TEST1, TEST2, TEST3 and TEST4 pins should be connected to AVSS.

No.	Pin Name	I/O	Function
23	LRCK	I/O	Output Channel Clock Pin
24	MCLK	I	Master Clock Input Pin
25	PDN	I	Power-Down Mode Pin "H": Power up, "L": Power down reset and initializes the control register.
26	ALC	I	ALC Enable Pin (Internal Pull-down Pin, typ. 100kΩ) "H" : ALC Enable, "L" : ALC Disable
27	SMUTE	I	Soft Mute Pin (Internal Pull-down Pin, typ. 100kΩ) "H" : Soft Mute, "L" : Normal Operation
28	SEL0	I	Input Selector 0 Pin
29	SEL1	I	Input Selector 1 Pin
30	SEL2	I	Input Selector 2 Pin
31	CDTI	I	Control Data Input Pin in 3-wire Control (CTRL pin = "L")
	SDA	I/O	Control Data Input / Output Pin in I^2C Control (CTRL pin = "H")
32	CCLK	I	Control Data Clock Pin in 3-wire Control (CTRL pin = "L")
	SCL	I	Control Data Clock Pin in I^2C Control (CTRL pin = "H")
33	CSN	I	Chip Select Pin in 3-wire Control (CTRL pin = "L")
	CAD1	I	Chip Address 1 Select Pin in I^2C Control (CTRL pin = "H")
34	CTRL	I	Control Mode Pin "H" : I^2C Control & I^2S Compatible, "L" : 3-wire Control
35	M/S	I	Master / Slave Mode Pin "H" : Master Mode, "L" : Slave Mode
36	RIN1	I	Rch Analog Input 1 Pin
37	TEST5	I	Test 5 Pin (Connected to AVSS)
38	RIN2	I	Rch Analog Input 2 Pin
39	TEST6	I	Test 6 Pin (Connected to AVSS)
40	RIN3	I	Rch Analog Input 3 Pin
41	TEST7	I	Test 7 Pin (Connected to AVSS)
42	RIN4	I	Rch Analog Input 4 Pin
43	TEST8	I	Test 8 Pin (Connected to AVSS)
44	RIN5	I	Rch Analog Input 5 Pin

Note: All digital input pins except pull-down pins should not be left floating.
Note: TEST5, TEST6, TEST7 and TEST8 pins should be connected to AVSS.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	−0.3	6.0	V
	Digital	DVDD	−0.3	6.0	V
	|AVSS – DVSS| (Note 2)	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (VREF, LIN1-5, RIN1-5, LOPIN, ROPIN, IPGAL, IPGAR pins)		VINA	−0.3	AVDD+0.3	V
Digital Input Voltage (All digital input pins)		VIND	−0.3	DVDD+0.3	V
Ambient Temperature (powered applied)		Ta	−40	85	°C
Storage Temperature		Tstg	−65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AVSS and DVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 3)	Analog	AVDD	4.75	5.0	5.25	V
	Digital	DVDD	3.0	3.3	AVDD	V

Note 1. All voltages with respect to ground.
Note 3. The power up sequence between AVDD and DVDD is not critical.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=5.0V, DVDD=3.3V; AVSS=DVSS=0V; fs=48kHz, 96kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz at fs=48kHz, 40Hz ~ 40kHz at fs=96kHz; unless otherwise specified)

Parameter			min	typ	max	Units
Pre-Amp Characteristics:						
Feedback Resistance			10		50	kΩ
S/(N+D)		(Note 4)	-	100		dB
S/N (A-weighted)			-	108		dB
Load Resistance		(Note 5)	6.3			kΩ
Load Capacitance					20	pF
Input PGA Characteristics:						
Input Voltage		(Note 6)	0.9	1	1.1	Vrms
Input Resistance		(Note 7)	6.3	10	15	kΩ
Step Size			0.2	0.5	0.8	dB
Gain Control Range	ALC = OFF		0		+12	dB
	ALC = ON		−9.5		+12	dB
ADC Analog Input Characteristics: IPGA=0dB, ALC = OFF		(Note 8)				
Resolution					24	Bits
S/(N+D) (−0.5dBFS)	fs=48kHz		84	94		dB
	fs=96kHz		82	92		dB
DR (−60dBFS)	fs=48kHz, A-weighted		96	103		dB
	fs=96kHz		89	99		dB
S/N	fs=48kHz, A-weighted		96	103		dB
	fs=96kHz		89	99		dB
Interchannel Isolation		(Note 9)	90	110		dB
Interchannel Gain Mismatch				0.2	0.5	dB
Gain Drift				100	-	ppm/°C
Power Supply Rejection		(Note 10)		50	-	dB
Power Supplies						
Power Supply Current						
Normal Operation (PDN pin = "H")						
AVDD				23	35	mA
DVDD	(fs=48kHz)			4	8	mA
	(fs=96kHz)			8	16	mA
Power-down mode (PDN pin = "L")		(Note 11)				
AVDD				10	100	μA
DVDD				10	100	μA

Note 4. This value is measured at LOUT and ROUT pins using the circuit as shown in Figure 24. The input signal voltage is 2Vrms.

Note 5. This value is the input impedance of an external device that the LOUT and ROUT pins can drive, when a device is connected with LOUT and ROUT pin externally. The feedback resistor (min. 10kΩ) that it is usually connected with the LOUT/ROUT pins, and the value of input impedance (min. 6.3kΩ) of the IPGAL/R pins are not included.

Note 6. Full scale (0dB) of the input voltage at ALC=OFF and IPGA=0dB. Input voltage to IPGAL and IPGAR pins is proportional to AVDD voltage. Vin = 0.2 x AVDD (Vrms).

Note 7. This value is input impedance of the IPGAL and IPGAR pins.

Note 8. This value is measured via the following path. Pre-Amp → IPGA (Gain : 0dB) → ADC. The measurement circuit is Figure 24.

Note 9. This value is the interchannel isolation between all the channels of the LIN1-5 and RIN1-5 when the applied input signal causes the Pre-Amp output to equal IPGA input.

Note 10. PSR is applied to AVDD and DVDD with 1kHz, 50mVpp.

Note 11. All digital input pins are held DVDD or DVSS.

FILTER CHARACTERISTICS (fs=48kHz)

(Ta=−40 ~ 85°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 5.25V; fs=48kHz)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 12)	−0.005dB	PB	0		21.5	kHz
	−0.02dB		-	21.768	-	kHz
	−0.06dB		-	22.0	-	kHz
	−6.0dB		-	24.0	-	kHz
Stopband		SB	26.5			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	80			dB
Group Delay (Note 13)		GD		29.6		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 12)	−3dB	FR		1.0		Hz
	−0.5dB			2.9		Hz
	−0.1dB			6.5		Hz

Note 12. The passband and stopband frequencies scale with fs. For example, 21.768kHz at −0.02dB is 0.454 x fs.
Note 13. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 24bit data both channels to the ADC output register for ADC.

FILTER CHARACTERISTICS (fs=96kHz)

(Ta=−40 ~ 85°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 5.25V; fs=96kHz)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 14)	−0.005dB	PB	0		43.0	kHz
	−0.02dB		-	43.536	-	kHz
	−0.06dB		-	44.0	-	kHz
	−6.0dB		-	48.0	-	kHz
Stopband		SB	53.0			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	80			dB
Group Delay (Note 15)		GD		29.6		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 14)	−3dB	FR		2		Hz
	−0.5dB			5.8		Hz
	−0.1dB			13		Hz

Note 14. The passband and stopband frequencies scale with fs. For example, 43.536kHz at −0.02dB is 0.454 x fs.
Note 15. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 24bit data both channels to the ADC output register for ADC.

DC CHARACTERISTICS

(Ta=−40 ~ 85°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 5.25V)

Parameter	Symbol	min	typ	Max	Units
High-Level Input Voltage	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%DVDD	V
High-Level Output Voltage (Iout=−400μA)	VOH	DVDD-0.5	-	-	V
Low-Level Output Voltage					
(Except SDA pin : Iout=400μA)	VOL	-	-	0.5	V
(SDA pin : Iout=3mA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=−40 ~ 85°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 5.25V; C_L=20pF)

Parameter		Symbol	min	typ	max	Units
Master Clock Timing						
Frequency		fCLK	8.192		24.576	MHz
Pulse Width Low		tCLKL	0.4/fCLK			ns
Pulse Width High		tCLKH	0.4/fCLK			ns
LRCK Frequency						
Normal Speed Mode		fsn	32		48	kHz
Double Speed Mode		fsd	48		96	kHz
Duty Cycle	Slave mode		45		55	%
	Master mode			50		%
Audio Interface Timing						
Slave mode						
BICK Period		tBCK	160			ns
BICK Pulse Width Low		tBCKL	65			ns
Pulse Width High		tBCKH	65			ns
LRCK Edge to BICK "↑" (Note 16)		tLRB	30			ns
BICK "↑" to LRCK Edge (Note 16)		tBLR	30			ns
LRCK to SDTO (MSB) (Except I^2S mode)		tLRS			35	ns
BICK "↓" to SDTO		tBSD			35	ns
Master mode						
BICK Frequency		fBCK		64fs		Hz
BICK Duty		dBCK		50		%
BICK "↓" to LRCK		tMBLR	−20		20	ns
BICK "↓" to SDTO		tBSD	−20		35	ns

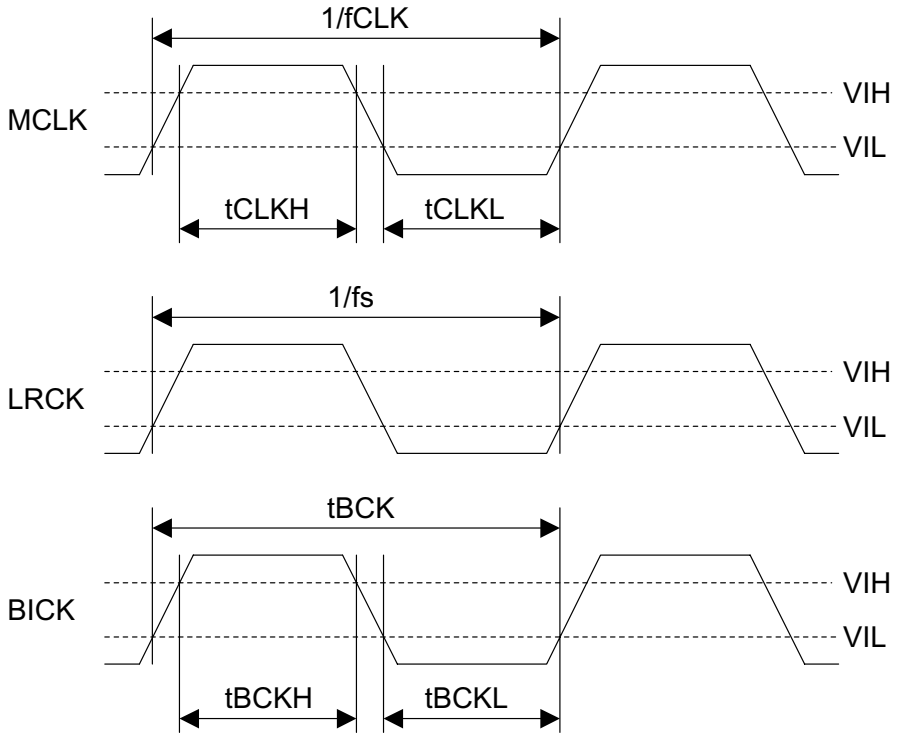
Note 17. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	min	typ	max	Units
Control Interface Timing (3-wire Serial mode):					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	40			ns
CDTI Hold Time	tCDH	40			ns
CSN "H" Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		100	kHz
Bus Free Time Between Transmissions	tBUF	4.7		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	4.0		-	µs
Clock Low Time	tLOW	4.7		-	µs
Clock High Time	tHIGH	4.0		-	µs
Setup Time for Repeated Start Condition	tSU:STA	4.7		-	µs
SDA Hold Time from SCL Falling (Note 17)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.25		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		1.0	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	4.0		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Reset Timing					
PDN Pulse Width (Note 18)	tPD	150			ns
PDN "↑" to SDTO valid (Note 19)	tPDV		516		1/fs
PWN "↑" to SDTO valid (Note 20)	tPDV		516		1/fs

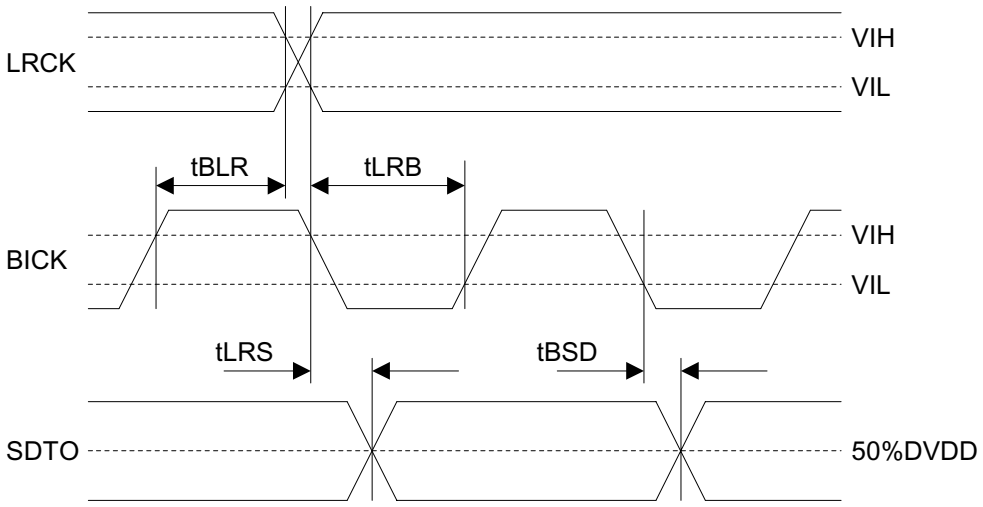
Note 17. Data must be held long enough to bridge the 300ns-transition time of SCL.
Note 18. The AK5365 can be reset by bringing the PDN pin = "L".
Note 19. This cycle is the number of LRCK rising edges from the PDN pin = "H".
Note 20. This cycle is the number of LRCK rising edges from the PWN bit = "1".

Purchase of Asahi Kasei Microsystems Co., Ltd I^2C components conveys a license under the Philips I^2C patent to use the components in the I^2C system, provided the system conform to the I^2C specifications defined by Philips.

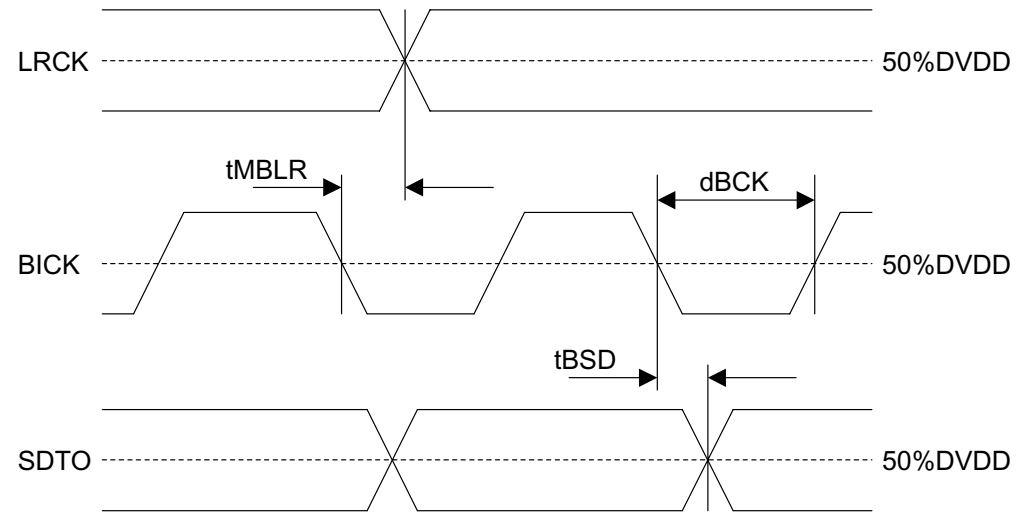
■ **Timing Diagram**



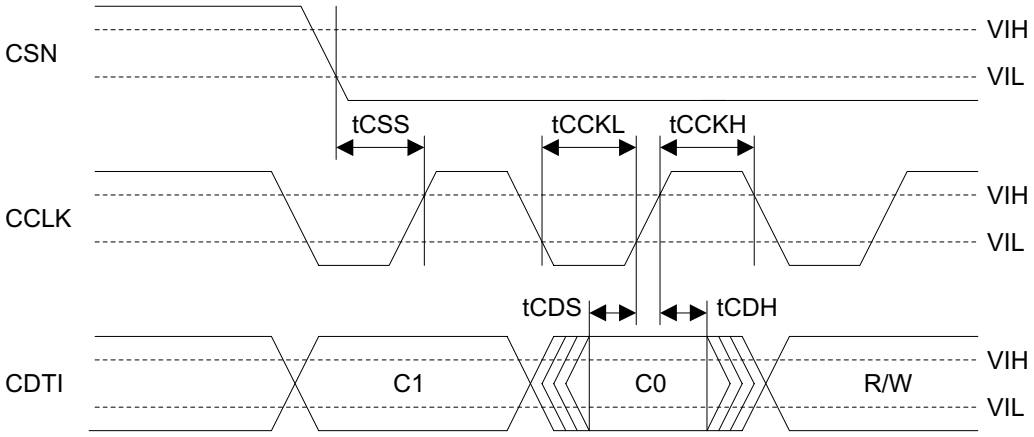
Clock Timing



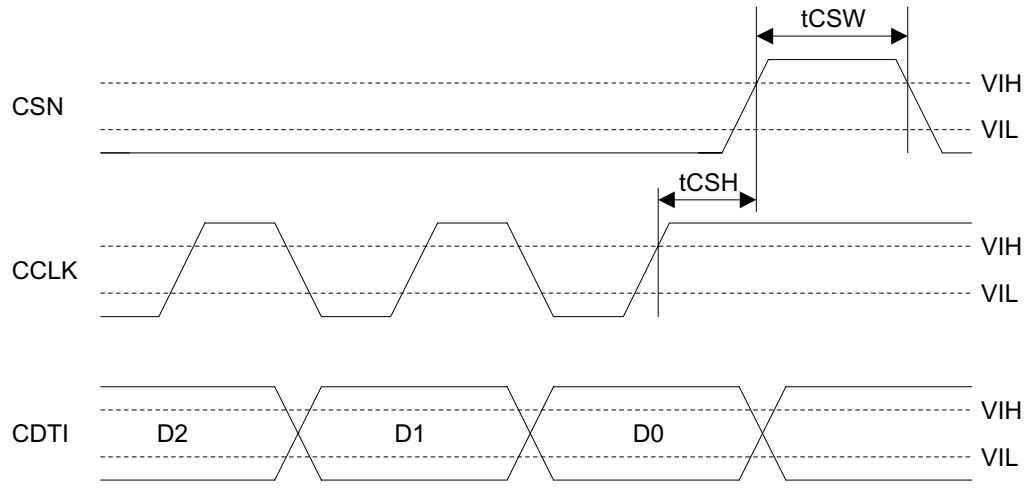
Audio Interface Timing (Slave mode)



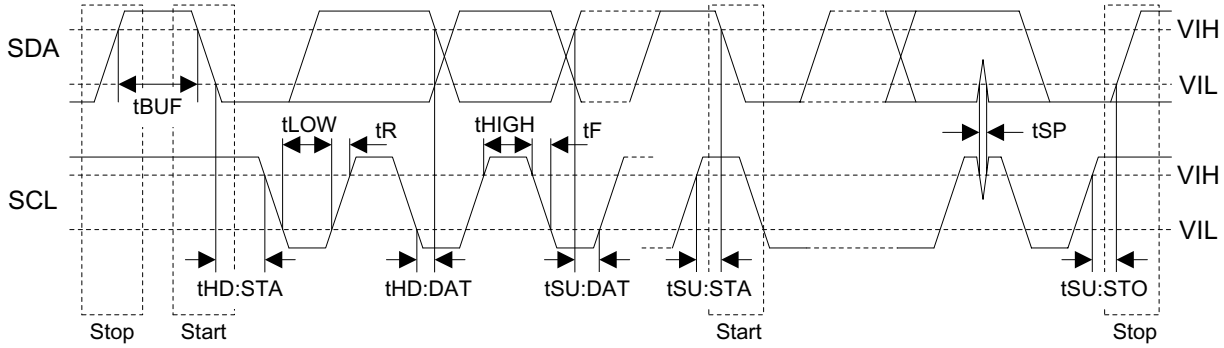
Audio Interface Timing (Master mode)



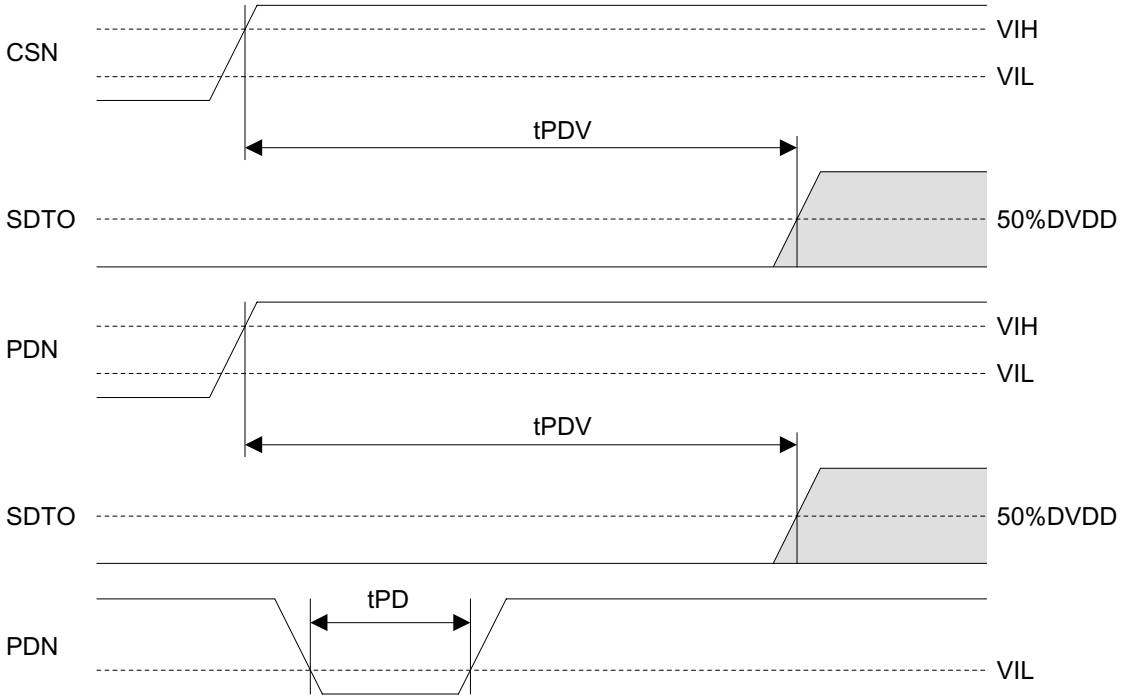
WRITE Command Input Timing



WRITE Data Input Timing



I^{2}C Bus Mode Timing



Power Down & Reset Timing

OPERATION OVERVIEW

■ System Clock

MCLK (256fs/384fs/512fs), BICK (48fs~) and LRCK (fs) clocks are required in slave mode. The LRCK clock input must be synchronized with MCLK, however the phase is not critical. MCLK frequency is automatically detected in slave mode. Table 1 shows the relationship of typical sampling frequency and the system clock frequency.

MCLK (256fs/384fs/512fs) is required in master mode. MCLK frequency is selected by CKS1-0 bits as shown in Table 2. In master mode, after setting CKS1-0 bits, there is a possibility the frequency and duty of LRCK and BICK outputs become an abnormal state.

All external clocks (MCLK, BICK and LRCK) must be present unless PDN pin = "L" and PWN bit = "1". If these clocks are not provided, the AK5365 may draw excess current due to its use of internal dynamically refreshed logic. If the external clocks are not present, place the AK5365 in power-down mode (PDN pin = "L" or PWN bit = "0"). In master mode, the master clock (MCLK) must be provided unless PDN pin = "L".

fs	MCLK		
	256fs	384fs	512fs
32kHz	8.192MHz	12.288MHz	16.384MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz
48kHz	12.288MHz	18.432MHz	24.576MHz
96kHz	24.576MHz	N/A	N/A

Table 1. System clock example (Slave mode)

CKS1	CKS0	MCLK		
		32kHz ≤ fs ≤ 48kHz	48kHz < fs ≤ 96kHz	
0	0	256fs	256fs	Default
0	1	512fs	N/A	
1	0	384fs	N/A	
1	1	N/A	N/A	

Table 2. Master clock frequency select (Master mode)

■ Audio Interface Format

Two kinds of data formats can be chosen with the DIF bit (Table 3) and the CTRL pin (Table 4). The DIF bit and CTRL pin are ORed between pin and register. In both modes, the serial data is in MSB first, 2's compliment format. The SDTO is clocked out on the falling edge of BICK. The audio interface supports both master and slave modes. In master mode, BICK and LRCK are output with the BICK frequency fixed to 64fs and the LRCK frequency fixed to 1fs.

Mode	DIF bit	SDTO	LRCK	BICK	Figure	
0	0	24bit, MSB justified	H/L	≥ 48fs	Figure 1	Default
1	1	24bit, I^2S Compatible	L/H	≥ 48fs	Figure 2	

Table 3. Audio Interface Format (CTRL pin = "L")

Mode	CTRL pin	SDTO	LRCK	BICK	Figure
0	L	24bit, MSB justified	H/L	≥ 48fs	Figure 1
1	H	24bit, I^2S Compatible	L/H	≥ 48fs	Figure 2

Table 4. Audio Interface Format (DIF bit = "0")

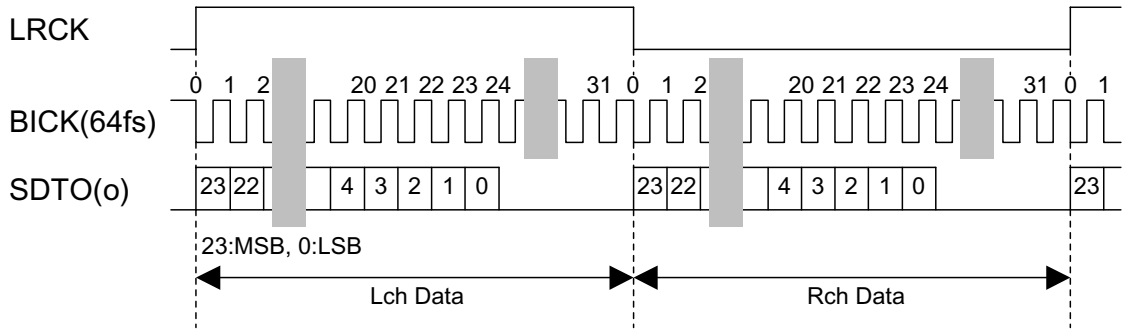


Figure 1. Mode 0 Timing

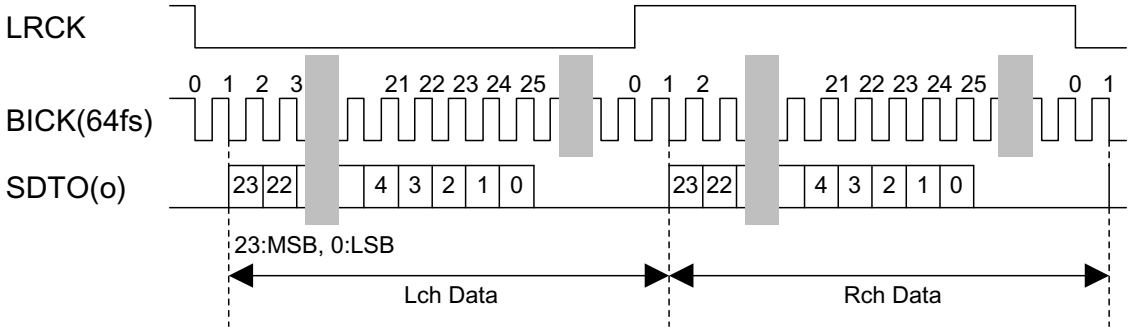


Figure 2. Mode 1 Timing

■ Master Mode and Slave Mode

The M/S pin selects either master or slave mode. M/S pin = "H" selects master mode and "L" selects slave mode. The AK5365 outputs BICK and LRCK in master mode. In slave mode, MCLK, BICK and LRCK are input externally.

	BICK, LRCK
Slave Mode	BICK = Input LRCK = Input
Master Mode	BICK = Output LRCK = Output

Table 5. Master mode/Slave mode

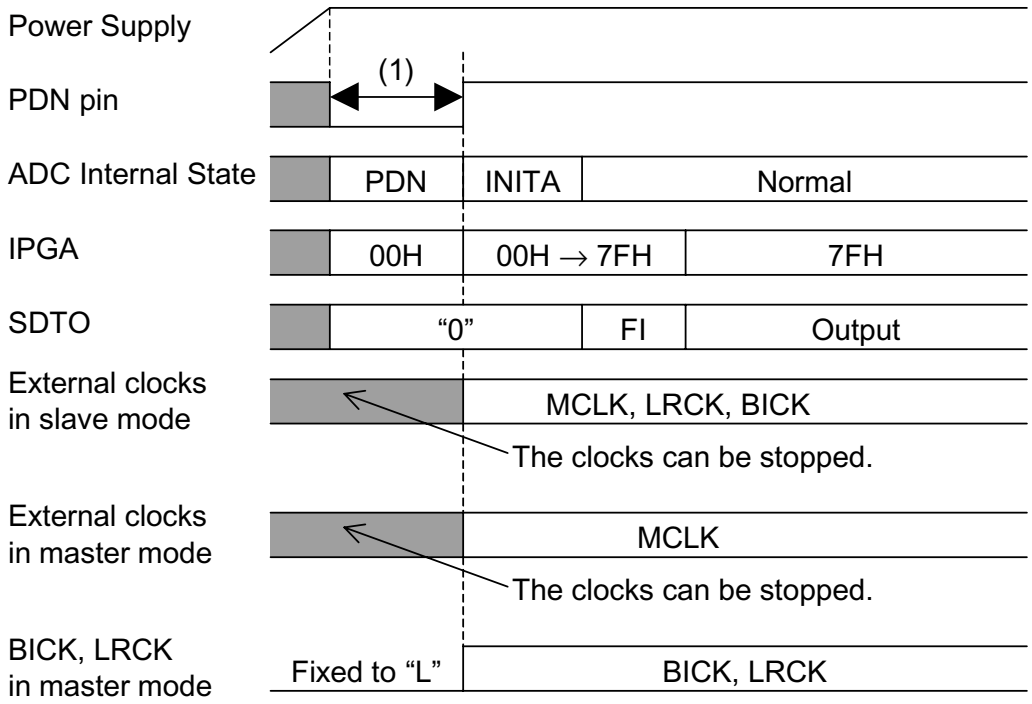
■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 1.0Hz (@fs=48kHz) and scales with sampling rate (fs).

■ Power-up/down

The AK5365 is placed in the power-down mode by bringing PDN pin = "L" and the digital filter is also reset at the same time. This reset should always be done after power-up. An analog initialization cycle starts after exiting the power-down mode. Therefore, the output data SDTO becomes available after 516 cycles of LRCK.

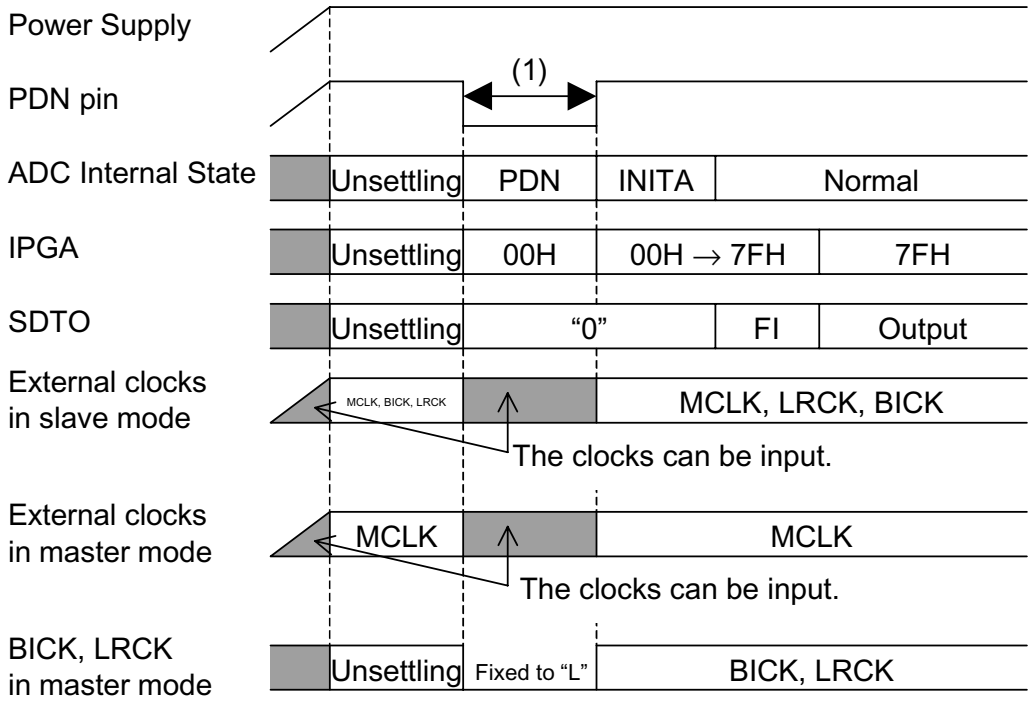
(1) Power-up Sequence 1



- INITA : Initializing period of ADC analog section (516/fs).
- FI : Fade in. After exiting power down, IPGA value fades in.
- PDN : Power down state.
- The period of (1) should be min. 150ns in Figure 3.

Figure 3. Power-up Sequence 1

(2) Power-up Sequence 2



- INITA : Initializing period of ADC analog section (516/fs).
- FI : Fade in. After exiting power down, IPGA value fades in.
- PDN : Power down state.
- The period of (1) should be min. 150ns in Figure 4.

Figure 4. Power-up Sequence 2

■ Input Selector

The AK5365 includes 5ch stereo input selectors (Figure 5). The input selector is 5 to 1 selector. The input channel is set by the SEL2-0 bits (Table 6) and the SEL2-0 pins (Table 7). The SEL2-0 pins should be fixed to "LLL" if the AK5365 is controlled by the SEL 2-0 bits, because the setting of the SEL2-0 pins are prior to the SEL2-0 bits setting.

SEL2 bit	SEL1 bit	SEL0 bit	Input Channel	
0	0	0	LIN1 / RIN1	Default
0	0	1	LIN2 / RIN2	
0	1	0	LIN3 / RIN3	
0	1	1	LIN4 / RIN4	
1	0	0	LIN5 / RIN5	

Table 6. Input Selector (SEL2-0 pin = "LLL")

SEL2 pin	SEL1 pin	SEL0 pin	Input Channel
L	L	L	LIN1 / RIN1
L	L	H	LIN2 / RIN2
L	H	L	LIN3 / RIN3
L	H	H	LIN4 / RIN4
H	L	L	LIN5 / RIN5

Table 7. Input Selector (SEL2-0 bit = "000")

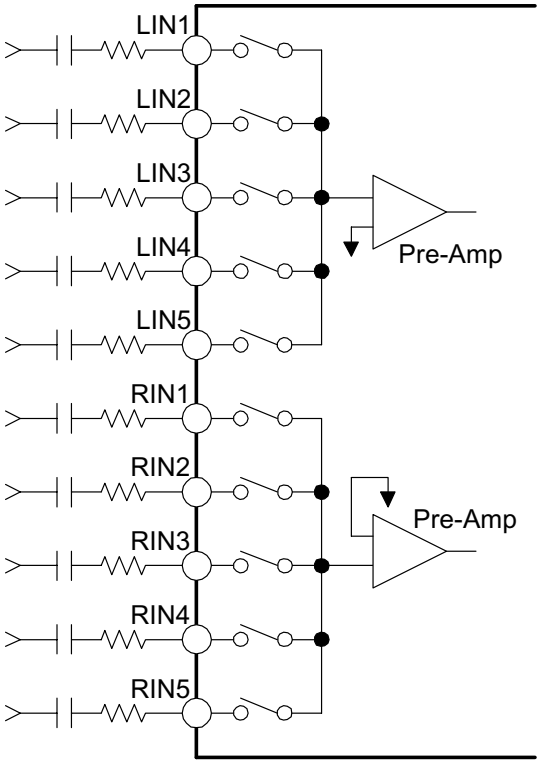


Figure 5. Input Selector

[Input selector switching sequence]

The input selector should be changed after soft mute to avoid the switching noise of the input selector (Figure 6).

1. Enable the soft mute before changing channel.
2. Change channel.
3. Disable the soft mute.

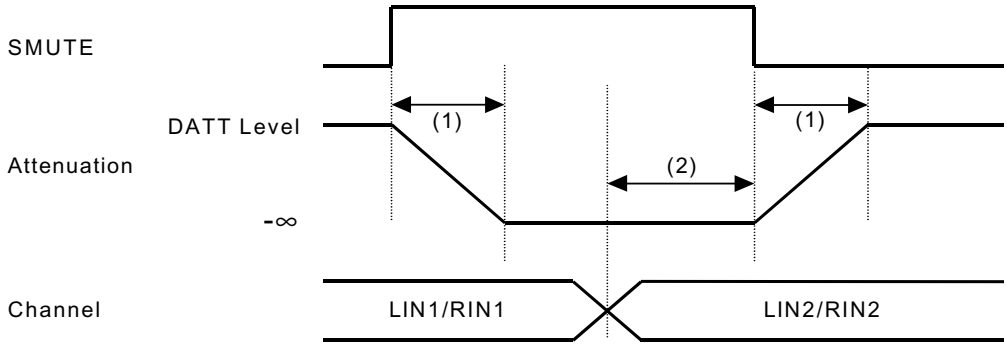


Figure 6. Input channel switching sequence example

The period of (1) varies in the setting value of DATT. It takes 1024/fs to mute when DATT value is 0dB.

When changing channels, the input channel should be changed during (2). The period of (2) should be around 200ms because there is some DC difference between the channels.

■ Function of CTRL Pin

The CTRL pin sets the audio interface format and the type of serial control interface. When the CTRL pin is "L", the audio interface format is selected by the DIF bit and the serial control interface is 3-wire control mode. When the CTRL pin is "H", the audio interface format is fixed to 24bit I^2S compatible and the serial control interface is I^2C-bus control mode.

CTRL pin	Audio Interface Format	Serial Control Interface
L	Note	3-wire Control
H	24bit, I^2S Compatible	I^2C-Bus Control

Table 8. CTRL pin Function

Note: The audio interface format is ORed between the CTRL pin and DIF bit. When the CTRL pin is "L", the audio interface format can be selected between 24bit MSB justified and 24bit I^2S compatible by DIF bit. When the CTRL pin is "H", the audio interface format is fixed to 24bit I^2S compatible.

■ Input Attenuator

The input ATTs are constructed by adding the input resistor (Ri) for LIN1-5/RIN1-5 pins and the feedback resistor (Rf) between LOPIN (ROPIN) pin and LOUT (ROUT) pin (Figure 7). The input voltage range of the IPGAL/IPGAR pin is typically 0.2 x AVDD (Vrms). If the input voltage of the input selector exceeds 0.2 x AVDD, the input voltage of the IPGAL/IPGAR pins must be attenuated to 0.2 x AVDD by the input ATTs. Table 9 shows the example of Ri and Rf.

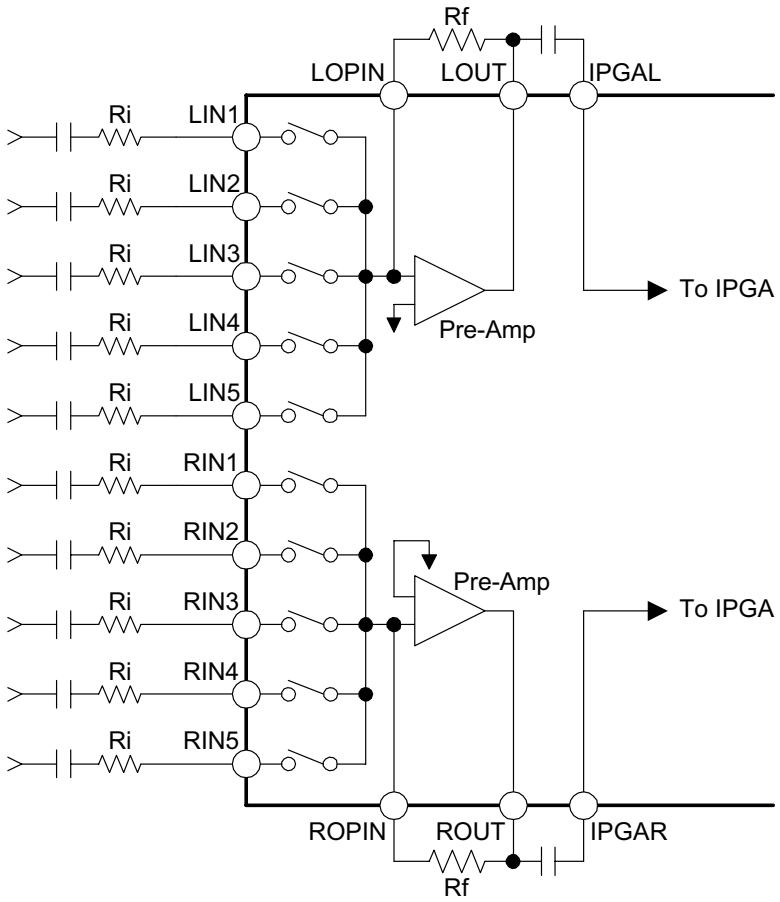


Figure 7. Input ATT

- Example for input range

Input Range	Ri [kΩ]	Rf [kΩ]	ATT Gain [dB]	IPGAL/R pin
4Vrms	47	12	−11.86	1.02Vrms
2Vrms	47	24	−5.84	1.02Vrms
1Vrms	47	47	0	1Vrms

Table 9. Input ATT example

■ Input Volume

The AK5365 includes two independent channel analog volumes (IPGA) with 25 levels at 0.5dB steps located in front of the ADC. The digital volume controls (DATT) have 128 levels (including MUTE) and is located after the ADC. Both the analog and digital volumes are controlled through the same register address. When the MSB of the register is "1", the IPGA changes and when the MSB = "0", the DATT changes.

The IPGA is a true analog volume control that improves the S/N ratio as seen in Table 10. Independent zero-crossing detection is used to ensure level changes only occur during zero-crossings. If there are no zero-crossings, the level will then change after a time-out period (Table 11); the time-out period scales with fs. If a new value is written to the IPGA register before the IPGA changes at the zero crossing or time-out, the previous value becomes invalid. The timer (channel independent) for time-out is reset and the timer restarts for new IPGA value.

The DATT is a pseudo-log volume that is linear-interpolated internally. When changing the level, the transition between ATT values has 8031 levels and is done by soft changes, eliminating any switching noise.

	Input Gain Setting		
	0dB	+6dB	+12dB
fs=48kHz, A-weight	103dB	100dB	96dB

Table 10. PGA+ADC S/N

ZTM1	ZTM0	Zero crossing timeout period	@fs=48kHz	
0	0	288/fs	6ms	
0	1	1152/fs	24ms	
1	0	2304/fs	48ms	Default
1	1	4608/fs	96ms	

Table 11. Zero crossing timeout period

[Writing operation at ALC Enable]

Writing to the area over 80H (Table 17) of IPGL/R registers is ignored during ALC operation. After ALC is disabled, the IPGA changes to the last written data by zero-crossing or time-out. In case of writing to the DATT area under 7FH (Table 17) of IPGL/R registers, the DATT changes even if ALC is enabled.

■ ALC Operation

[1] ALC Limiter Operation

When the ALC limiter is enabled, and either Lch or Rch exceed the ALC limiter detection level (LMTH bit), the IPGA value is attenuated by the amount defined in the ALC limiter ATT step (LMAT bit) automatically. Then the IPGA value is changed commonly for L/R channels.

When the ZELMN bit = "1", the timeout period is set by the LTM1-0 bits. The operation for attenuation is done continuously until the input signal level becomes the ALC limiter detection level (LMTH bit) or less. If the ALC bit does not change into "0" or the ALC pin does not change into "L" after completing the attenuation, the attenuation operation repeats until the input signal level equals or exceeds the ALC limiter detection level (LMTH bit).

When the ZELMN bit = "0", the timeout period is set by the ZTM1-0 bits. This enables the zero-crossing attenuation function so that the IPGA value is attenuated at the zero-detect points of the waveform.

When FR bit = "1", the ALC operation corresponds to the impulse noise in additional to the normal ALC operation. Then if the impulse noise is supplied at ZELMN bit = "0", the ALC operation becomes the faster period than a set of ZTM1-0 bits. In case of ZELMN bit = "1", it becomes the same period as LTM1-0 bits. When FR bit = "0", the ALC operation is the normal ALC operation.

[2] ALC Recovery Operation

The ALC recovery refers to the amount of time that the AK5365 will allow a signal to exceed a predetermined limiting value prior to enabling the limiting function. The ALC recovery operation uses the WTM1-0 bits to define the wait period used after completing an ALC limiter operation. If the input signal does not exceed the "ALC Recovery Waiting Counter Reset Level", the ALC recovery operation starts. The IPGA value increases automatically during this operation up to the reference level (REF7-0 bits). The ALC recovery operation is done at a period set by the WTM1-0 bits. Zero crossing is detected during WTM1-0, the ALC recovery operation waits WTM1-0 period and the next recovery operation starts.

During the ALC recovery operation, when input signal level exceeds the ALC limiter detection level (LMTH bit), the ALC recovery operation changes immediately into an ALC limiter operation.
In the case of "(Recovery waiting counter reset level) ≤ Input Signal < Limiter detection level" during the ALC recovery operation, the wait timer for the ALC recovery operation is reset. Therefore, in the case of "(Recovery waiting counter reset level) > Input Signal", the wait timer for the ALC recovery operation starts.

When the impulse noise is input at FR bit = "1", the ALC recovery operation becomes faster than a normal recovery operation. When the FR bit = "0", the ALC recovery operation is done by normal period.

[3] ALC Level Diagram

(1) ALC=OFF

Figure 8 and 9 show the level diagram example at ALC=OFF. In Figure 8, Input ATT is −12dB.

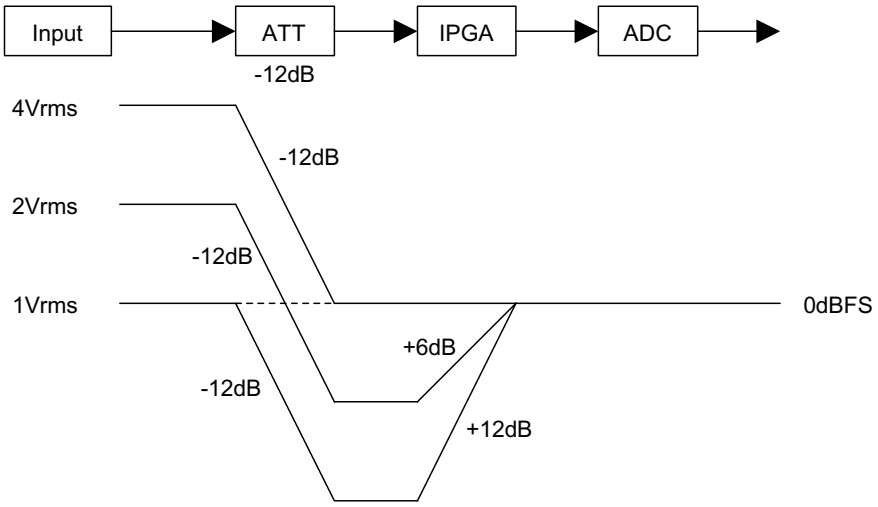


Figure 8. ALC Level diagram example (ALC=OFF)

In Figure 9, Input ATT is −6dB.

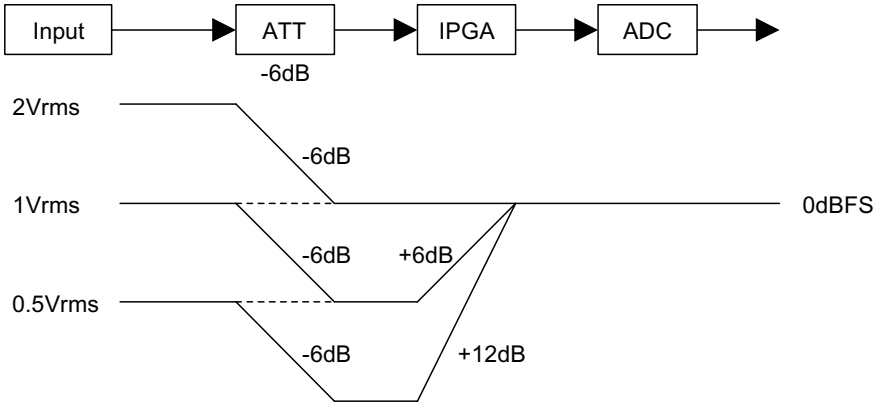


Figure 9. ALC Level diagram example (ALC=OFF)

(2) ALC=ON

Figure 10 and 11 show the level diagram example at ALC=ON. In Figure 10, Input ATT is −12dB and REF7-0 bits are "8CH".

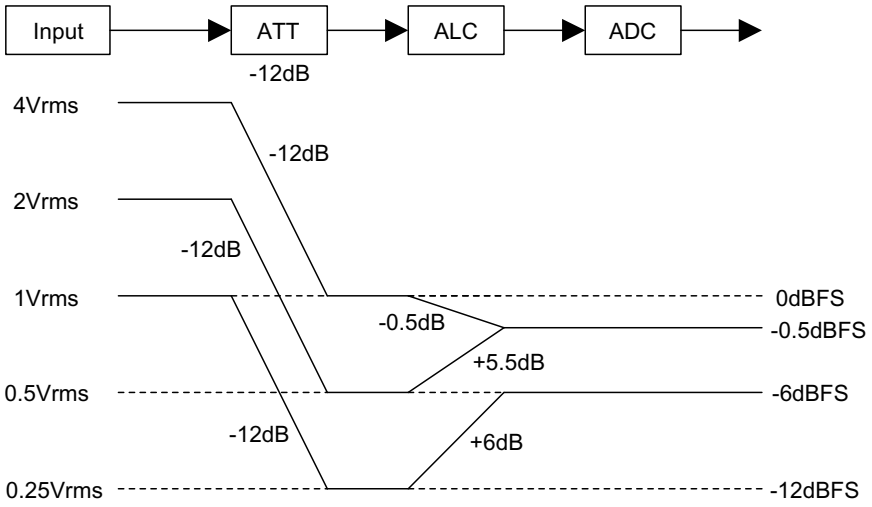


Figure 10. ALC Level diagram example (ALC=ON)

In Figure 11, Input ATT is −6dB and REF7-0 bits are "8CH".

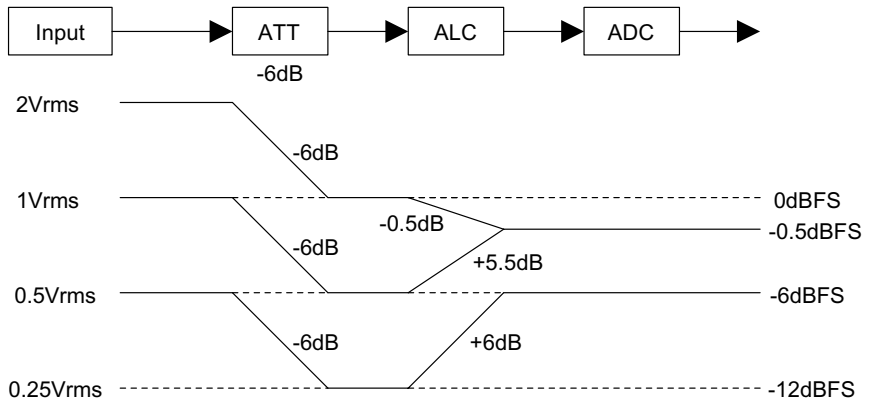
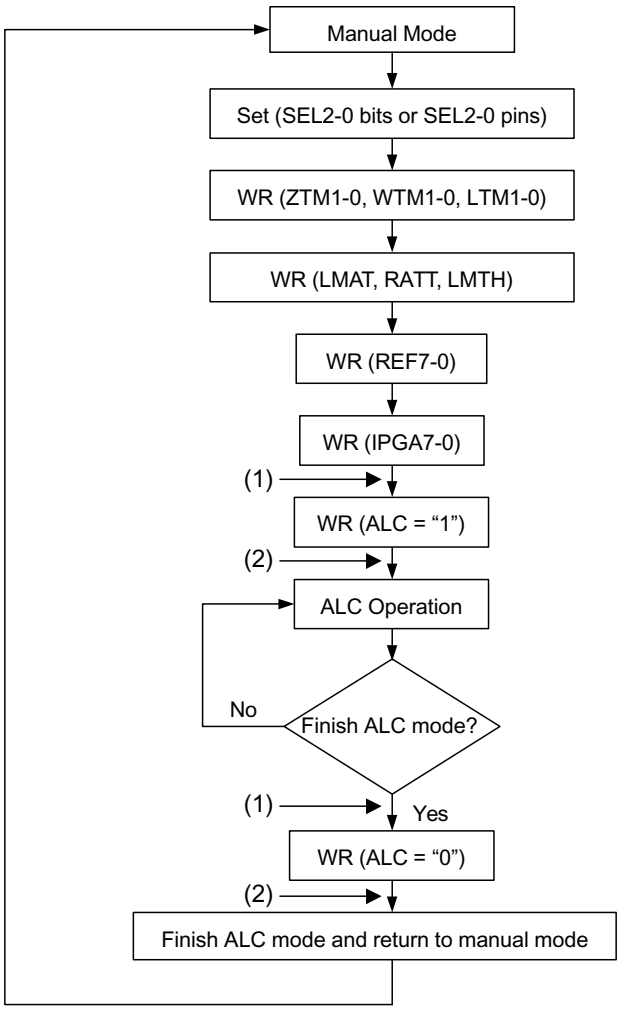


Figure 11. ALC Level diagram example (ALC=ON)

[4] Example of ALC Operation

The following registers should not be changed during the ALC operation.

- **LTM1-0, LMTH, LMAT, WTM1-0, ZTM1-0, RATT, REF7-0, ZELMN bits**
- The IPGA value of Lch becomes the start value if the IPGA value is different with Lch and Rch when the ALC starts.
- Writing to the area over 80H (Table 17) of IPGL/R registers is ignored during ALC operation. After ALC is disabled, the IPGA changes to the last written data by zero-crossing or time-out. In case of writing to the DATT area under 7FH (Table 17) of IPGL/R registers, the DATT changes even if ALC is enabled.



Note : WR : Write

Figure 12. Registers set-up sequence at ALC operation

(1): Enable soft mute (2): Disable soft mute

Note : ALC operation is enabled by the ALC pin.

Note : All the bits about ALC operation operate by the default value when an ALC operation is started with the ALC pin without setting up a bit about ALC operation with the register. A bit about ALC operation operate by the setting value when a bit about ALC operation is set up with the register and an ALC operation is started with the ALC pin.

Note : After ALC operation is disabled, the IPGA changes to the last written data during or before ALC operation.

[5] IPGA value before and after ALC operation

[Operation Example 1]

1. Set IPGA = +12dB at ALC=OFF. DATT portion is set to 0dB internally.
2. ALC=ON after soft mute is enabled.
3. Disable the soft mute.
4. During ALC operation. The IPGA changes from −9.5dB to the value set by REF7-0 bits.
5. ALC=OFF after soft mute is enabled.
6. Disable the soft mute. The IPGA return to +12dB automatically.

[Operation Example 2]

1. Set IPGA = +12dB at ALC=OFF. DATT portion is set to 0dB internally.
2. ALC=ON after soft mute is enabled.
3. Disable the soft mute.
4. During ALC operation. When the DATT portion is set to −10dB, the IPGA changes from −19.5dB to the value set by REF7-0 bits.
5. ALC=OFF after soft mute is enabled.
6. Disable the soft mute. The IPGA setting is −10dB.

■ Soft Mute Operation

Soft mute operation is performed in the digital domain of the ADC output.

Soft mute can be controlled by SMUTE bit or SMUTE pin. The SMUTE bit and SMUTE pin are ORed between pin and register. When SMUTE bit goes "1" or SMUTE pin goes "H", the ADC output data is attenuated by −∞ within 1024 LRCK cycles. When the SMUTE bit returned "0" or SMUTE pin goes "L" the mute is cancelled and the output attenuation gradually changes to IPGA value within 1024 LRCK cycles. If the soft mute is cancelled before mute state after starting of the operation, the attenuation is discontinued and returned to IPGA value.

Soft mute function and digital volume are common.

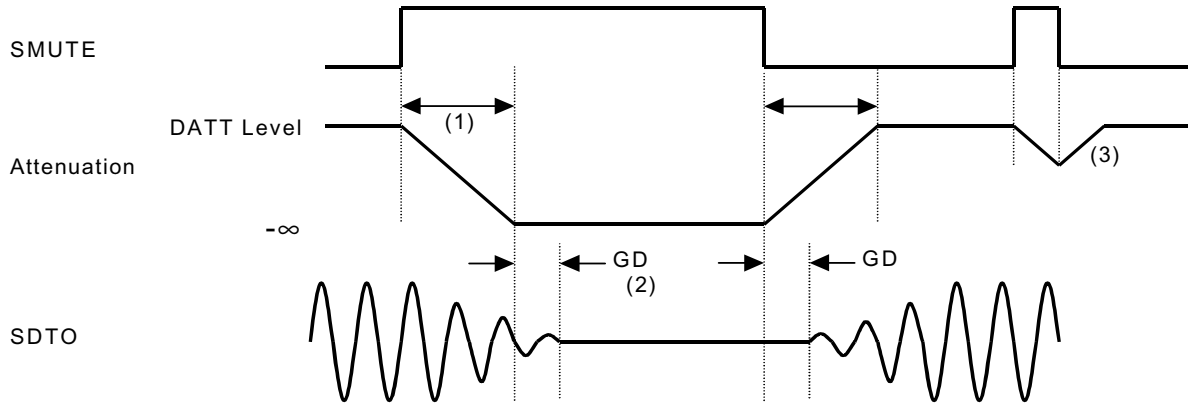


Figure 13. Soft Mute Function

(1) The output signal is attenuated by −∞ within 1024 LRCK cycles (1024/fs).
(2) Digital output delay from the analog input is called the group delay (GD).
(3) If the soft mute is cancelled before the mute, the attenuation is discontinued and returned to IPGA value.

■ Chip Address

In case of 3-wire control mode, the chip address is fixed to C1 bit = "1" and C0 bit = "0". Table 12 shows the relationship between chip address (C1-0 bits) and CAD1 pin in I^2C-bus control mode.

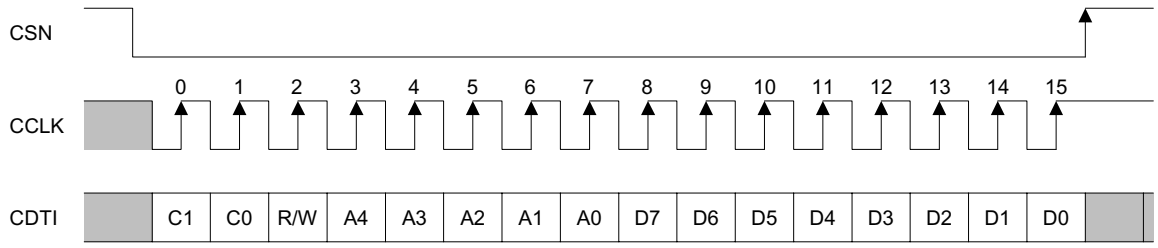
CAD1 pin	C1 bit	C0 bit
L	0	Fixed to "1"
H	1	Fixed to "1"

Table 12. Chip address in I^2C-bus control

Note : C1 bit should match with the input level of CAD1 pin.

■ Serial Control Interface

(1) 3-wire Serial Control Mode (CTRL pin = "L")
Internal registers may be written by using the 3-wire µP interface pins (CSN, CCLK and CDTI). The data on this interface consists of a Chip address (2bits, Fixed to "10"), Read/Write (1bit, Fixed to "1", Write only), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. After a low-to-high transition of CSN, data is latched for write operations. The clock speed of CCLK is 5MHz (max). The value of internal registers is initialized at PDN pin = "L".



C1 - C0 : Chip Address (C1="1", C0="0")
R/W : READ / WRITE (Fixed to "1" : WRITE only)
A4 - A0 : Register Address
D7 - D0 : Control Data

Figure 14. Serial Control I/F Timing

(2) I^2C-bus Control Mode (CTRL pin = "H")
The AK5365 supports the standard-mode I^2C-bus (max: 100kHz). The AK5365 does not support a fast-mode I^2C-bus system (max: 400kHz).

(2)-1. WRITE Operations
Figure 15 shows the data transfer sequence for the I^2C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 21). After the START condition, a slave address is sent. This address is 7 bits long followed by an eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as "00100". The next one bit are CAD1 (device address bits). This one bit identify the specific device on the bus. The hard-wired input pin (CAD1 pin) set these device address bits (Figure 16). If the slave address matches that of the AK5365, the AK5365 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 22). A R/W bit value of "1" indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK5365. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 17). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 18). The AK5365 generates an acknowledge after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 21).

The AK5365 can perform more than one byte write operation per sequence. After receipt of the third byte the AK5365 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 5-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 07H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 23) except for the START and STOP conditions.

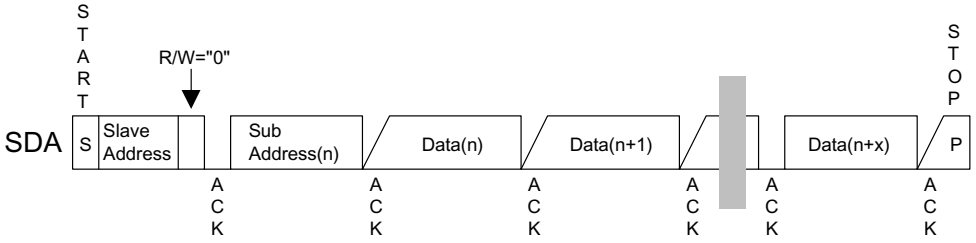


Figure 15. Data Transfer Sequence at the I^2C-Bus Mode

0	0	1	0	0	CAD1	1	R/W

(CAD1 should match with CAD1 pin.)
Figure 16. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 17. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 18. Byte Structure after the second byte

(2)-2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK5365. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 5-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 07H prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The AK5365 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(2)-2-1. CURRENT ADDRESS READ

The AK5365 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) were to address n, the next CURRENT READ operation would access data from the address n+1. After receipt of the slave address with R/W bit set to "1", the AK5365 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates a stop condition, the AK5365 ceases transmission.

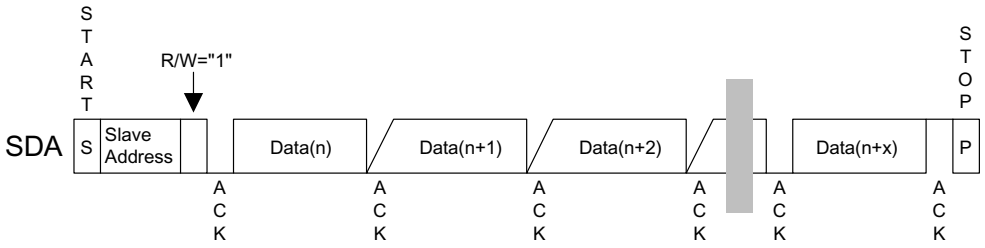


Figure 19. CURRENT ADDRESS READ

(2)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit set to "1". The AK5365 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates a stop condition, the AK5365 ceases transmission.

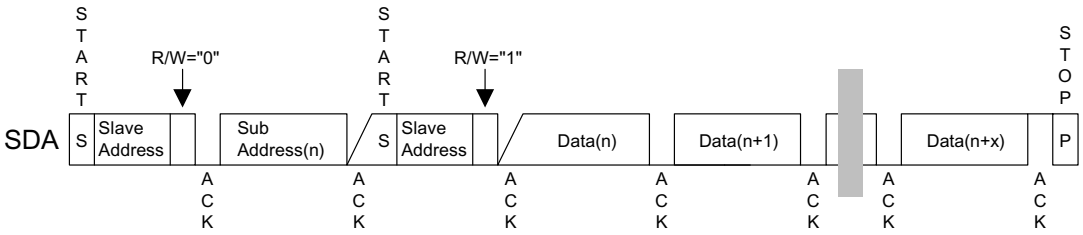


Figure 20. RANDOM ADDRESS READ

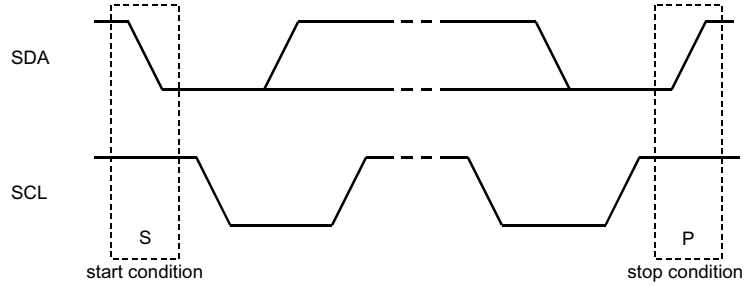


Figure 21. START and STOP Conditions

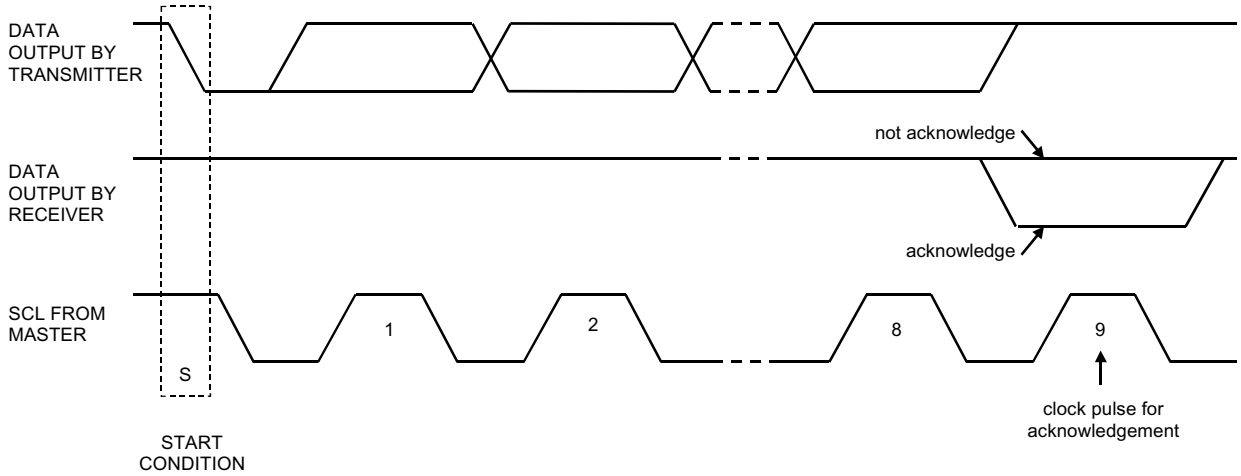


Figure 22. Acknowledge on the I^2C-Bus

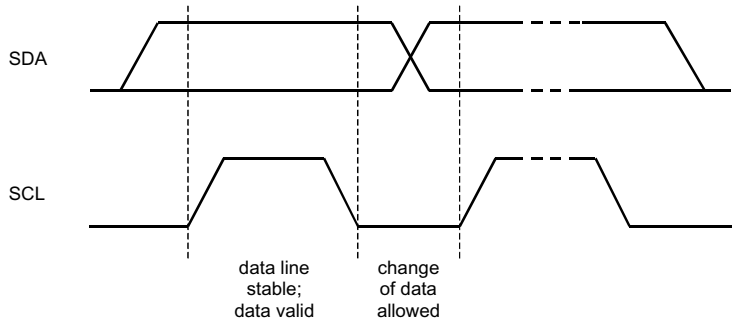


Figure 23. Bit Transfer on the I^2C-Bus

■ Control by Pin and Bit

Function	Pin	bit
ALC	ALC Enable Pin (Internal Pull-down) "L" : Disable "H" : Enable	ALC Enable bit "0" : Disable "1" : Enable
Input Selector	SEL2-0 Pin "LLL" : LIN1/RIN1 "LLH" : LIN2/RIN2 "LHL" : LIN3/RIN3 "LHH" : LIN4/RIN4 "HLL" : LIN5/RIN5	SEL2-0 bit "000" : LIN1/RIN1 "001" : LIN2/RIN2 "010" : LIN3/RIN3 "011" : LIN4/RIN4 "100" : LIN5/RIN5
Soft Mute	SMUTE Pin (Internal Pull-down) "L" : Normal operation "H" : Soft muted	SMUTE bit "0" : Normal operation "1" : Soft muted
Audio Interface Format	CTRL Pin "L" : 24bit MSB justified "H" : 24bit I^2S Compatible	DIF bit "0" : 24bit MSB justified "1" : 24bit I^2S Compatible

Table 13. Pin and Bit control

Note : The SEL2-0 pins should be fixed to "LLL" if the AK5365 is controlled by the SEL2-0 bits, because the setting of the SEL2-0 pins are prior to the SEL2-0 bits setting. Other Functions are ORed between pin and register.

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Down & Reset Control	0	0	0	0	0	0	0	PWN
01H	Input Selector Control	0	0	0	0	0	SEL2	SEL1	SEL0
02H	Clock & Format Control	0	0	0	0	DIF	CKS1	CKS0	SMUTE
03H	Timer Select	0	0	LTM1	LTM0	ZTM1	ZTM0	WTM1	WTM0
04H	Lch IPGA Control	IPGL7	IPGL6	IPGL5	IPGL4	IPGL3	IPGL2	IPGL1	IPGL0
05H	Rch IPGA Control	IPGR7	IPGR6	IPGR5	IPGR4	IPGR3	IPGR2	IPGR1	IPGR0
06H	ALC Mode Control 1	0	0	ZELMN	ALC	FR	LMTH	RATT	LMAT
07H	ALC Mode Control 2	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0

PDN pin = "L" resets the registers to their default values.

Note: Unused bits must contain a "0" value.
Note: Only write to address 00H to 07H.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Down & Reset Control	0	0	0	0	0	0	0	PWN
Default		0	0	0	0	0	0	0	1

PWN: Power down control
0 : Power down. All registers are not initialized.
1 : Normal Operation (Default)
"0" powers down all sections and then both IPGA and ADC do not operate. The contents of all register are not initialized and enabled to write to the registers.
When MCLK and LRCK are changed, it is not necessary to reset by the PDN pin or PWN bit because the AK5365 builds in reset-free circuit. However, it can be reduced the noise by reset.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Input Selector Control	0	0	0	0	0	SEL2	SEL1	SEL0
Default		0	0	0	0	0	0	0	0

SEL2-0: Input selector (see Table 6)
Initial values are "000".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Clock & Format Control	0	0	0	0	DIF	CKS1	CKS0	SMUTE
Default		0	0	0	0	0	0	0	0

SMUTE: Soft Mute control
0 : Normal Operation (Default)
1 : SDTO outputs soft-muted.

CKS1-0: Master clock frequency select (see Table 2)
Initial values are "00".

DIF: Audio interface format (see Table 3)
Initial values are "0".
When CTRL pin is "H", audio interface format is fixed to I^2S compatible.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Timer Select	0	0	LTM1	LTM0	ZTM1	ZTM0	WTM1	WTM0
Default		0	0	1	0	1	0	1	1

WTM1-0: ALC Recovery waiting time (see Table 14)

A period of recovery operation when any limiter operation does not occur during the ALC operation.

WTM1	WTM0	ALC recovery operation waiting period	@fs=48kHz	
0	0	288/fs	6ms	
0	1	1152/fs	24ms	
1	0	2304/fs	48ms	
1	1	4608/fs	96ms	Default

Table 14. ALC recovery waiting time

ZTM1-0: Zero crossing timeout (see Table 15)

When the IPGA of each L/R channels perform zero crossing or timeout independently, the IPGA value is changed by the μP WRITE operation, ALC recovery operation or ALC limiter operation (ZELMN bit = "0").

ZTM1	ZTM0	Zero crossing timeout period	@fs=48kHz	
0	0	288/fs	6ms	
0	1	1152/fs	24ms	
1	0	2304/fs	48ms	Default
1	1	4608/fs	96ms	

Table 15. Zero crossing timeout

LTM1-0: ALC Limiter period (see Table 16)

When ZELMN bit = "1", the IPGA value is changed immediately. When the IPGA value is changed continuously, the change is done by the period set by the LTM1-0 bits.

LTM1	LTM0	ALC limiter operation period	@fs=48kHz	
0	0	3/fs	63μs	
0	1	6/fs	125μs	
1	0	12/fs	250μs	Default
1	1	24/fs	500μs	

Table 16. ALC limiter period

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Lch IPGA Control	IPGL7	IPGL6	IPGL5	IPGL4	IPGL3	IPGL2	IPGL1	IPGL0
05H	Rch IPGA Control	IPGR7	IPGR6	IPGR5	IPGR4	IPGR3	IPGR2	IPGR1	IPGR0
Default		0	1	1	1	1	1	1	1

IPGL/R7-0: Input PGA & Digital volume control (see Table 17)
Initial values are “7FH”.

Digital ATT with 128 levels operates when writing data of less than 7FH. This ATT is a linear ATT with 8032 levels internally and these levels are assigned to pseudo-log data with 128 levels. The transition between ATT values has 8032 levels and is done by soft changes. For example, when ATT changes from 7FH to 7EH, the internal ATT value decreases from 8031 to 7775, one by one every fs cycle. It takes 8031 cycles (167ms@fs=48kHz) from 7FH to 00H (Mute).

The IPGAs are set to “00H” when PDN pin goes “L”. After returning to “H”, the IPGAs fade into the initial value, “7FH” in 8031 cycles.
The IPGAs are set to “00H” when PWN bit goes “0”. After returning to “1”, the IPGAs fade into the current value. The ADC output is “0” during the first 516LRCK cycles.

Writing to the area over 80H (Table 17) of IPGL/R registers is ignored during ALC operation. After ALC is disabled, the IPGA changes to the last written data by zero-crossing or time-out. In case of writing to the DATT area under 7FH (Table 17) of IPGL/R registers, the DATT changes even if ALC is enabled.

Data (hex)	Internal (DATT)	Gain (dB)	Step width (dB)	
98H	-	+12	-	**IPGA** Analog volume with 0.5dB step
97H	-	+11.5	0.5	
96H	-	+11	0.5	
:	-	:	0.5	
82H	-	+1.0	0.5	
81H	-	+0.5	0.5	
80H	-	0	-	
7FH	8031	0	-	**DATT** External 128 levels are converted to internal 8032 linear levels of DATT. Internal DATT soft-changes between data. DATT =2^m x (2 x l + 33) – 33 m: MSB 3-bits of data l: LSB 4-bits of data
7EH	7775	–0.28	0.28	
7DH	7519	–0.57	0.29	
:	:	:	:	
70H	4191	–5.65	0.51	
6FH	3999	–6.06	0.41	
6EH	3871	–6.34	0.28	
:	:	:	:	
60H	2079	–11.74	0.52	
5FH	1983	–12.15	0.41	
5EH	1919	–12.43	0.28	
:	:	:	:	
50H	1023	–17.90	0.53	
4FH	975	–18.32	0.42	
4EH	943	–18.61	0.29	
:	:	:	:	
40H	495	–24.20	0.54	
3FH	471	–24.64	0.43	
3EH	455	–24.94	0.30	
:	:	:	:	
30H	231	–30.82	0.58	
2FH	219	–31.29	0.46	
2EH	211	–31.61	0.32	
:	:	:	:	
20H	99	–38.18	0.67	
1FH	93	–38.73	0.54	
1EH	89	–39.11	0.38	
:	:	:	:	
10H	33	–47.73	0.99	
0FH	30	–48.55	0.83	
0EH	28	–49.15	0.60	
:	:	:	:	
05H	10	–58.10	1.58	
04H	8	–60.03	1.94	
03H	6	–62.53	2.50	
02H	4	–66.05	3.52	
01H	2	–72.07	6.02	
00H	0	MUTE		

Table 17. IPGA Code Table

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	ALC Mode Control 1	0	0	ZELMN	ALC	FR	LMTH	RATT	LMAT
Default		0	0	1	0	1	0	0	0

LMAT: ALC Limiter ATT step (see Table 18)

During the ALC limiter operation, when either Lch or Rch exceeds the ALC limiter detection level set by LMTH bit, the number of steps attenuated from the current IPGA value is set. For example, when the current IPGA value is 94H and the LMAT bit = "1", the IPGA transition to 92H when the ALC limiter operation starts, resulting in the input signal level being attenuated by 1dB (=0.5dB x 2).

LMAT	ATT Step	
0	1	Default
1	2	

Table 18. ALC limiter ATT step

RATT: ALC Recovery gain step (see Table 19)

During the ALC recovery operation, the number of steps changed from the current IPGA value is set. For example, when the current IPGA value is 82H and RATT bit = "1" is set, the IPGA changes to 84H by the ALC recovery operation and the output signal level is gained up by 1dB (=0.5dB x 2). When the IPGA value exceeds the reference level (REF7-0 bits), the IPGA value does not increase.

RATT	Gain Step	
0	1	Default
1	2	

Table 19. ALC recovery gain step

LMTH: ALC Limiter detection level / Recovery waiting counter reset level (see Table 20)

The ALC limiter detection level and the ALC recovery counter reset level may be offset by about ±2dB.

LMTH	ALC Limiter Detection Level	ALC Recovery Waiting Counter Reset Level	
0	ALC Output ≥ −0.5dBFS	−0.5dBFS > ALC Output ≥ −2.5dBFS	Default
1	ALC Output ≥ −2.0dBFS	−2.0dBFS > ALC Output ≥ −4.0dBFS	

Table 20. ALC Limiter detection level / Recovery waiting counter reset level

FR: ALC fast recovery

0 : Disable

1 : Enable (Default)

When the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation.

ALC: ALC enable flag

0 : ALC Disable (Default)

1 : ALC Enable

ZELMN: Zero crossing enable flag at ALC limiter operation

0 : Enable

1 : Disable (Default)

When the ZELMN bit = "0", the IPGA of each L/R channel perform a zero crossing or timeout independently. The zero crossing timeout is the same as the ALC recovery operation. When the ZELMN bit = "1", the IPGA value is changed immediately. The ALC Limiter period can be set up by a ZTM 1-0 bits when ZELMN bit = "0", it can be set up by a LTM1-0 bits when ZELMN bit = "1"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	ALC Mode Control 2	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
Default		1	0	0	0	1	0	0	1

REF7-0: Reference value at ALC recovery operation (see Table 21)

During the ALC recovery operation, if the IPGA value exceeds the setting reference value by gain operation, then the IPGA does not become larger than the reference value.

The REF7-0 bits should not be set up except for Table 21.

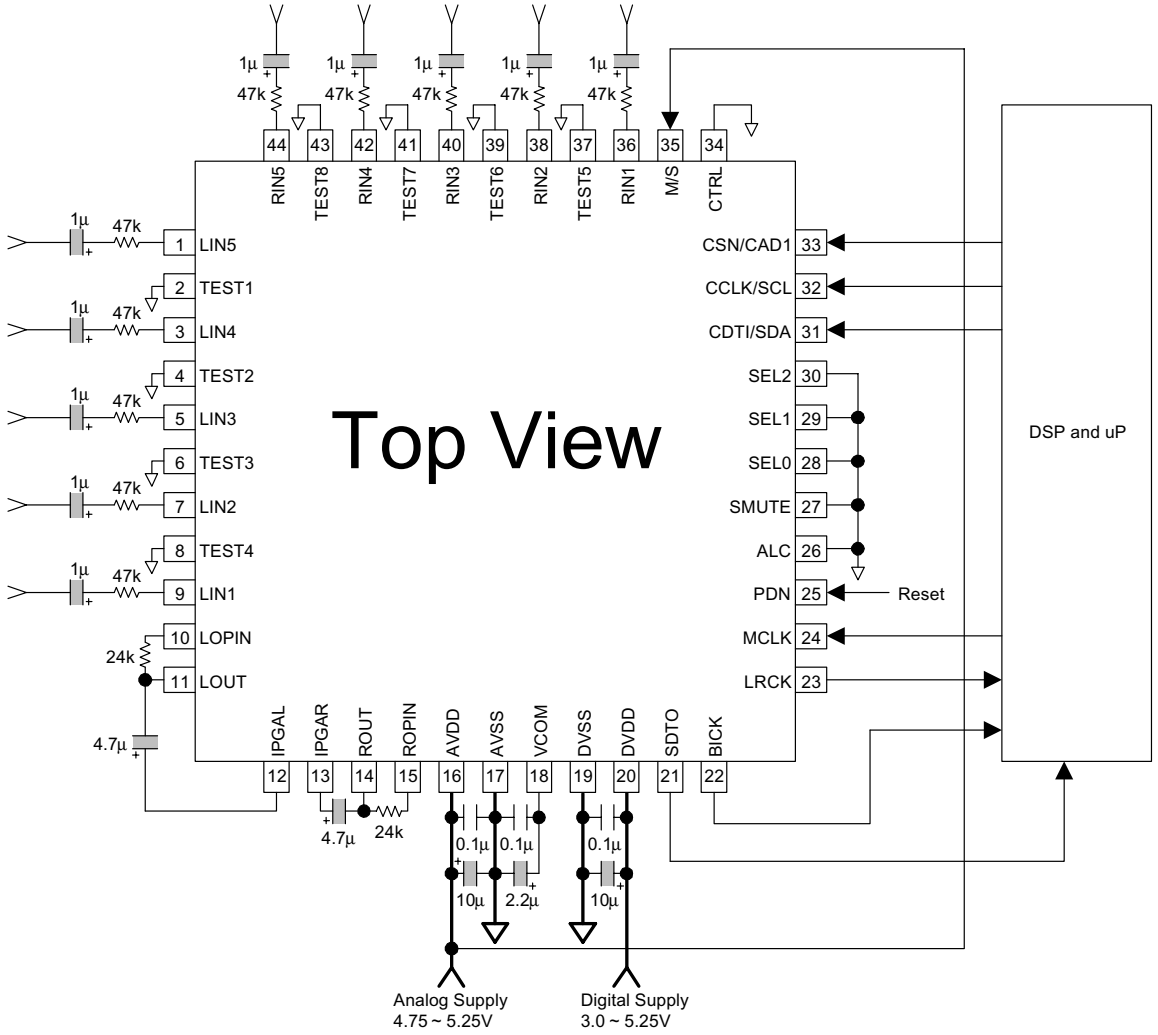
DATA (hex)	Gain (dB)	
98H	+12.0	
97H	+11.5	
96H	+11.0	
95H	+10.5	
:	:	
89H	+4.5	Default
:	:	
81H	+0.5	
80H	0	

Table 21. Reference value at ALC recovery operation

SYSTEM DESIGN

Figure 24 shows the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

- Master Mode, 3-wire control (CTRL pin = "L")



Note:
- AVSS and DVSS of the AK5365 should be distributed separately from the ground of external digital devices (MPU, DSP etc.).
- When LOUT/ROUT drives a capacitive load, resistors should be added in series between LOUT/ROUT and capacitive load.
- All input pins except pull-down pin (ALC, SMUTE pins) should not be left floating.

Figure 24. Typical Connection Diagram

1. Grounding and Power Supply Decoupling

The AK5365 requires careful attention to power supply and grounding arrangements. AVDD and DVDD are usually supplied from the analog supply in the system. Alternatively if AVDD and DVDD are supplied separately, the power up sequence is not critical. **AVSS and DVSS of the AK5365 must be connected to analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK5365 as possible, with the small value ceramic capacitor being the closest.

2. Voltage Reference Inputs

The differential voltage between AVDD and AVSS sets the analog input range. VCOM is a signal ground of this chip. An electrolytic capacitor 2.2μF parallel with a 0.1μF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VREF and VCOM pins in order to avoid unwanted coupling into the AK5365.

3. Analog Inputs

An analog input of AK5365 is single-ended input to Pre-Amp through the external resistor. For input signal range, adjust feedback resistor so that Pre-Amp output may become the input range (typ. 0.2 x AVDD Vrms) of IPGA (IPGAL, IPGAR pin). Between the Pre-Amp output (LOUT, ROUT pin) and the IPGA input (IPGAL, IPGAR pin) is AC coupled with capacitor. When the impedance of IPGAL/R pins is “R” and the capacitor of between the Pre-Amp output and the IPGA input is “C”, the cut-off frequency is $fc = 1/(2\pi RC)$.

The ADC output data format 2’s compliment. The internal HPF removes the DC offset.

The AK5365 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. The AK5365 includes an anti-aliasing filter (RC filter) to attenuate a noise around 64fs.

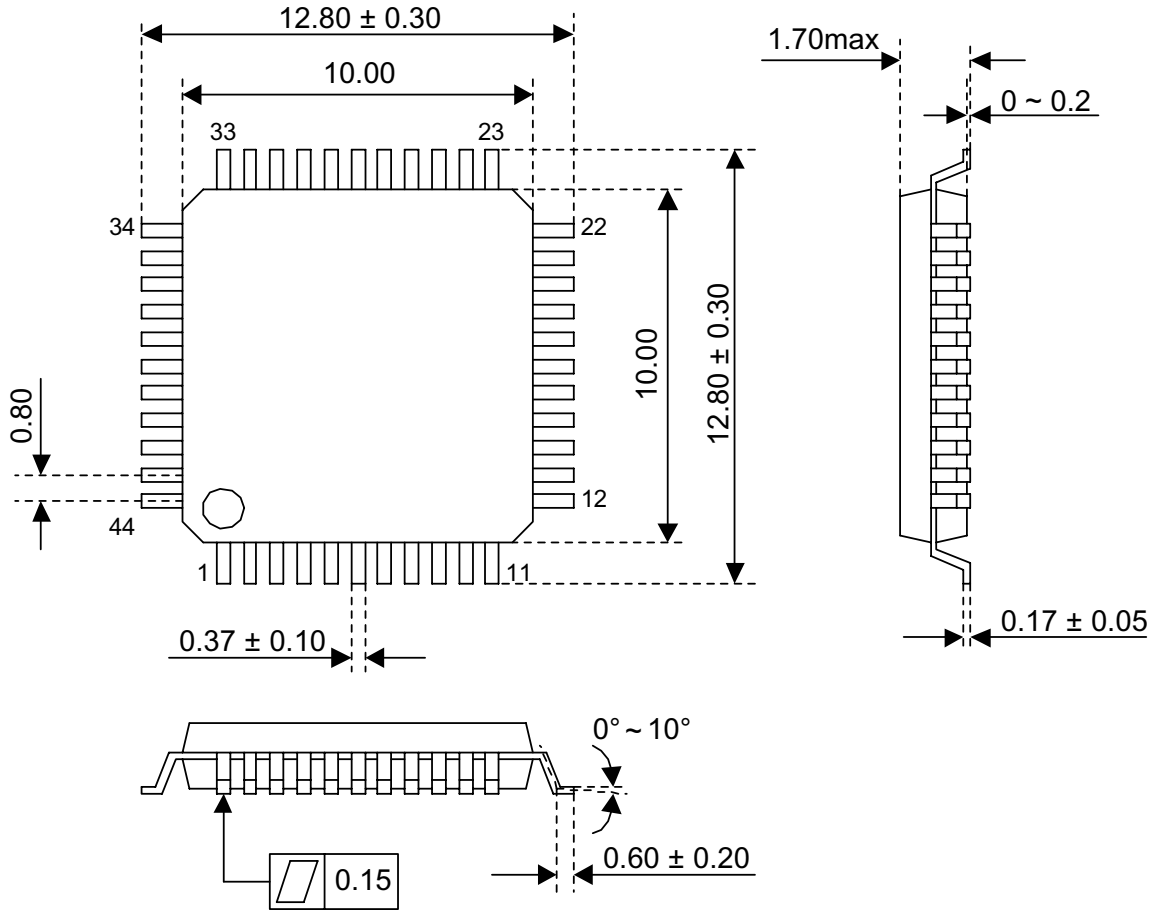
4. Attention to the PCB Wiring

LIN1-5 and RIN1-5 pins are the summing nodes of the Pre-Amp. Attention should be given to avoid coupling with other signals on those nodes. This can be accomplished by making the wire length of the input resistors as short as possible. The same theory also applies to the LOPIN/ROPIN pins and feedback resistors; keep the wire length to a minimum. Unused input pins among LIN1-5 and RIN1-5 pins should be left open.

When external devices are connected to LOUT and ROUT pin, the input impedance of an external device which the LOUT and ROUT pins can drive is min 6.3kΩ.

PACKAGE

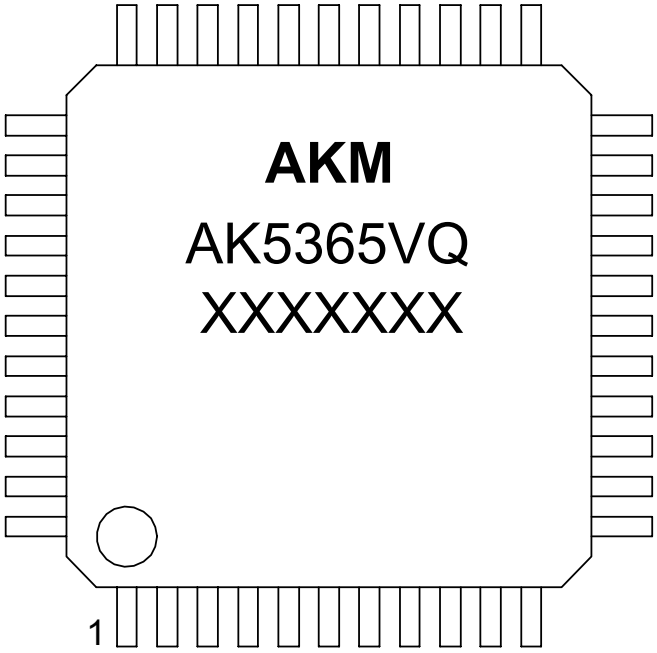
44pin LQFP (Unit: mm)



■ Material & Lead finish

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



XXXXXXX : Date Code Identifier (7 digits)

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