FAIRCHILD SEMICONDUCTOR®

October 2006

FDFC2P100

Integrated P-Channel PowerTrench® MOSFET and Schottky Diode

-20V, -3A, 150mΩ

Features

- Max $r_{DS(on)}$ = 150mΩ at V_{GS} = -4.5V, I_D = -3.0A
- Max $r_{DS(on)}$ = 200mΩ at V_{GS} = -2.5V, I_D = -2.2A
- Low Gate Charge (3.4nC typ)
- Compact industry standard SuperSOT™-6 package

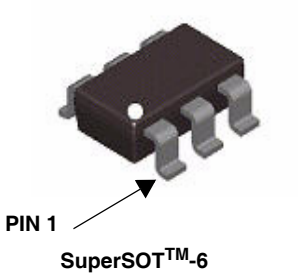
Schottky:

- V_F < 0.45 V at I_F = 1A
- RoHS Compliant

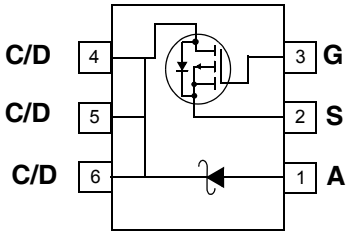
General Description

The FDFC2P100 combine the exceptional performance of Fairchild's PowerTrench MOSFET technology with a very low forward voltage drop Schottky barrier rectifier in an SSOT-6 package.

This device is designed specifically as a single package solution for DC to DC converters. It features a fast switching, low gate charge MOSFET with very low on-state resistance. Significant improvement of Thermal Characteristics and Power Dissipation via replacement of independently connected Schottky with internal connection of Schottky Diode Cathode pn to P-Channel PowerTrench MosFET Drain pin.



SuperSOT™-6



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DS}	Drain to Source Voltage		-20	V
V_{GS}	Gate to Source Voltage		±12	V
I_D	Drain Current -Continuous	(Note 1a)	-3	A
	-Pulsed		-6	
P_D	Power Dissipation	(Note 1a)	1.5	W
		(Note 1b)	0.8	
V_{RRM}	Schotty Repetitive Peak Reverse Voltage		20	V
I_O	Schotty Average Forward Current	(Note 1a)	1	A
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	87	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	166	

Package Marking and Ordering Information

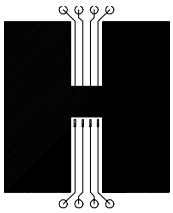
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
.100	FDFC2P100	SSOT-6	7”	8mm	3000units

Electrical Characteristics T_J = 25°C unless otherwise noted

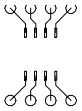
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250μA, V_{GS} = 0V	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250μA, referenced to 25°C		-12		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0V, V_{DS} = -16V			-1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±12V, V_{DS} = 0V			±100	μA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250μA	-0.6	-0.9	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250μA, referenced to 25°C		3		mV/°C
$r_{DS(on)}$	Drain to Source On-Resistance	V_{GS} = -4.5V, I_D = -3.0A		95	150	mΩ
		V_{GS} = -2.5V, I_D = -2.2A		150	200	
		V_{GS} = -4.5V, I_D = -3.0A, T_J = 125°C		130	252	
g_{FS}	Forward Transconductance	V_{DS} = -5V, I_D = -3.0A		5.4		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -10V, V_{GS} = 0V, f = 1MHz		335	445	pF
C_{oss}	Output Capacitance			80	105	pF
C_{rss}	Reverse Transfer Capacitance			40	60	pF
R_g	Gate Resistance	f = 1MHz		6		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -10V, I_D = -3.0A, V_{GS} = -4.5V, R_{GEN} = 6Ω		9	16	ns
t_r	Rise Time			11	20	ns
$t_{d(off)}$	Turn-Off Delay Time			12	22	ns
t_f	Fall Time			4	8	ns
$Q_{g(TOT)}$	Total Gate Charge at -10V	V_{GS} = 0V to -10V, V_{DD} = -4.5V, I_D = -3.0A		3.4	4.7	nC
Q_{gs}	Gate to Source Gate Charge			0.9		nC
Q_{gd}	Gate to Drain “Miller” Charge			1.0		nC
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain tio Source Diode forward Current				-1.2	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = -1.2A (Note 2)		-0.8	-1.2	V
t_{rr}	Reverse Recovery Time	I_F = -3.0A, di/dt = 100A/μs		17		ns
Q_{rr}	Reverse Recovery Charge			5		nC
Schottky Diode Characteristics						
I_R	Reverse Leakage	V_R = 20V	T_J = 25°C		26	400	μA
			T_J = 100C		2.7	20	mA
		V_R = 10V	T_J = 25°C		23	200	μA
			T_J = 100°C		2.5	10	mA
V_F	Forward Voltage	I_F = 500mA	T_J = 25°C		0.31	0.4	V
			T_J = 100°C		0.24	0.35	
		I_F = 1A	T_J = 25°C		0.37	0.45	
			T_J = 100°C		0.3	0.42	

Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 87°C/W when mounted on a $1in^2$ pad of 2 oz copper



b) 166°C/W when mounted on a minimun pad

2: Pulse Test: Pulse Width $\leq$300 ms, Duty Cycle < 2.0%

Typical Characteristics T_J = 25°C unless otherwise noted

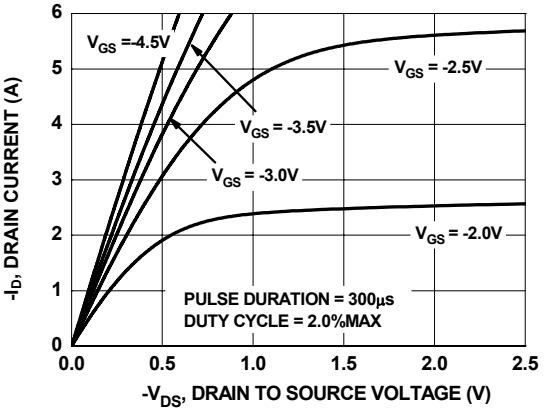


Figure 1. On Region Characteristics

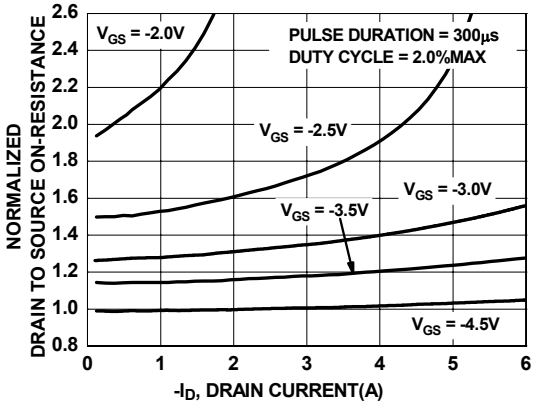


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

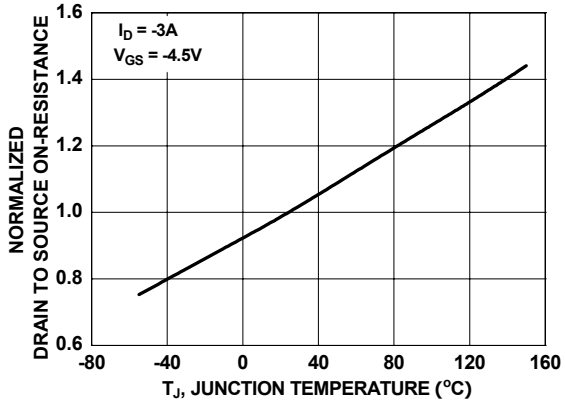


Figure 3. Normalized On-Resistance vs Junction Temperature

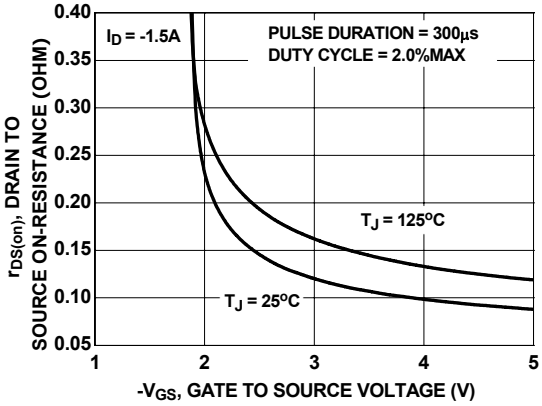


Figure 4. On-Resistance vs Gate to Source Voltage

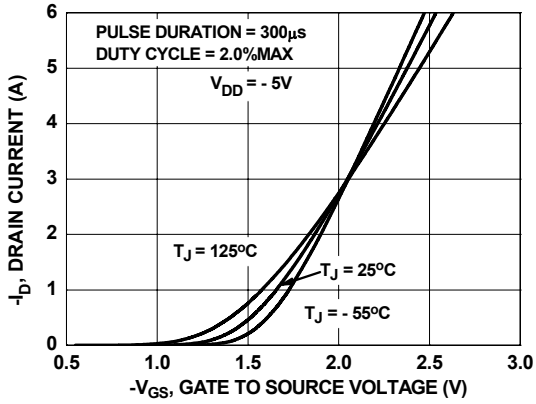


Figure 5. Transfer Characteristics

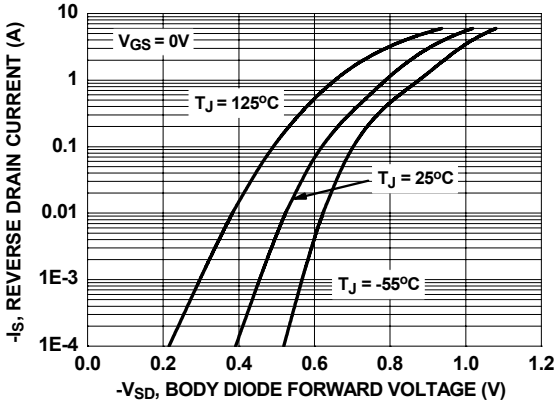


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

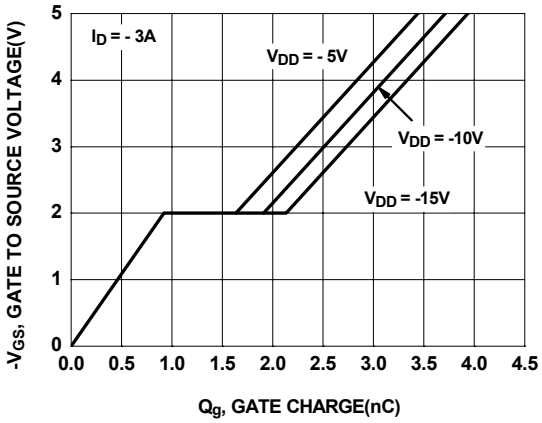


Figure 7. Gate Charge Characteristics

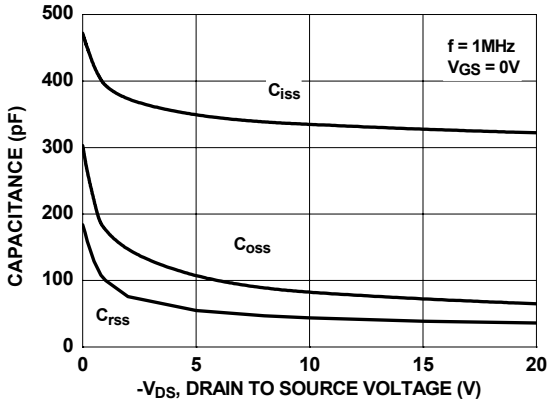


Figure 8. Capacitance vs Drain to Source Voltage

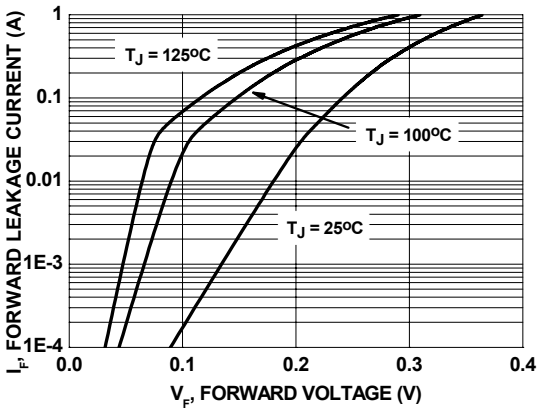


Figure 9. Schottky Diode Forward Voltage

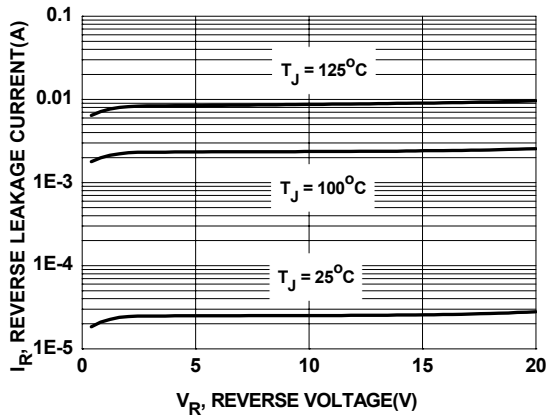


Figure 10. Schottky Diode Reverse Current

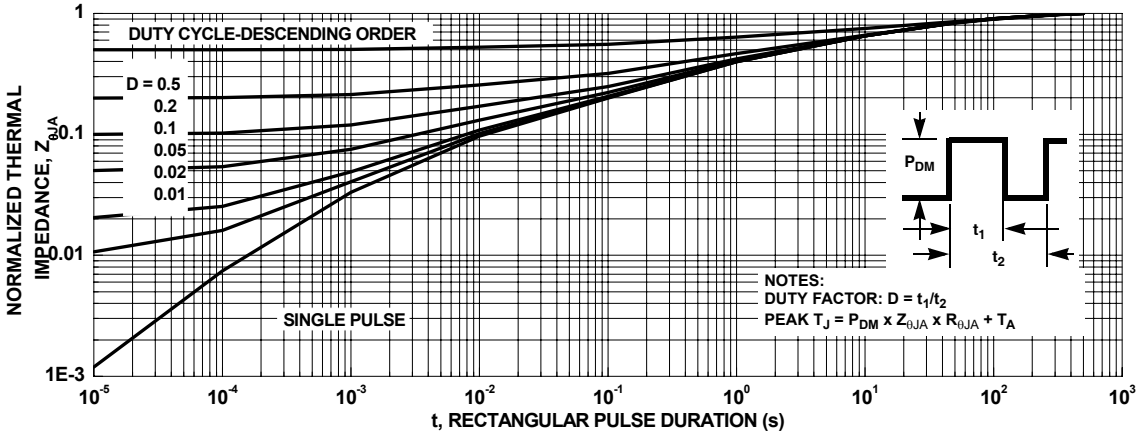


Figure 11. Transient Thermal Response Curve

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