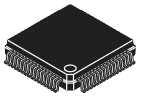
Battery cell controller IC

The 33772 is a SMARTMOS lithium ion Battery Cell Controller IC designed for automotive applications, such as hybrid electric (HEV) and electric vehicles (EV) along with industrial applications, such as energy storage systems (ESS), and uninterruptible power supply (UPS) systems. The device performs ADC conversions of the differential cell voltages and current, as well as battery Coulomb counting and battery temperature measurements. The information is digitally transmitted through SPI or transformer isolation to a microcontroller for processing.

33772

BATTERY CELL CONTROLLER IC



AE SUFFIX (PB-FREE)
98ASA00173D
48-PIN LQFP-EP

Features

- 5.0 V ≤ V_{PWR} ≤ 30 V operation, 40 V transient
- 3 to 6 cells management
- Isolated 2.0 Mbps differential communication or 4.0 Mbps SPI
- Addressable on initialization
- Synchronized cell voltage/current measurement with Coulomb count
- Total stack voltage measurement
- Seven GPIO/temperature sensor inputs
- 5.0 V at 5.0 mA reference supply output
- Automatic over/undervoltage & temperature detection routable to fault pin
- Integrated Sleep mode over/undervoltage & temperature monitoring
- Onboard 300 mA passive cell balancing with diagnostics
- Hot plug capable
- Detection of internal and external faults, as open lines, shorts, and leakages
- Single chip ASIL C capable
- Fully compatible with the MC33771 for max 14 cells

Applications

- Automotive: 12 V and high-voltage battery packs
- E-bikes, e-scooters
- Energy storage systems
- Uninterruptible power supply (UPS)

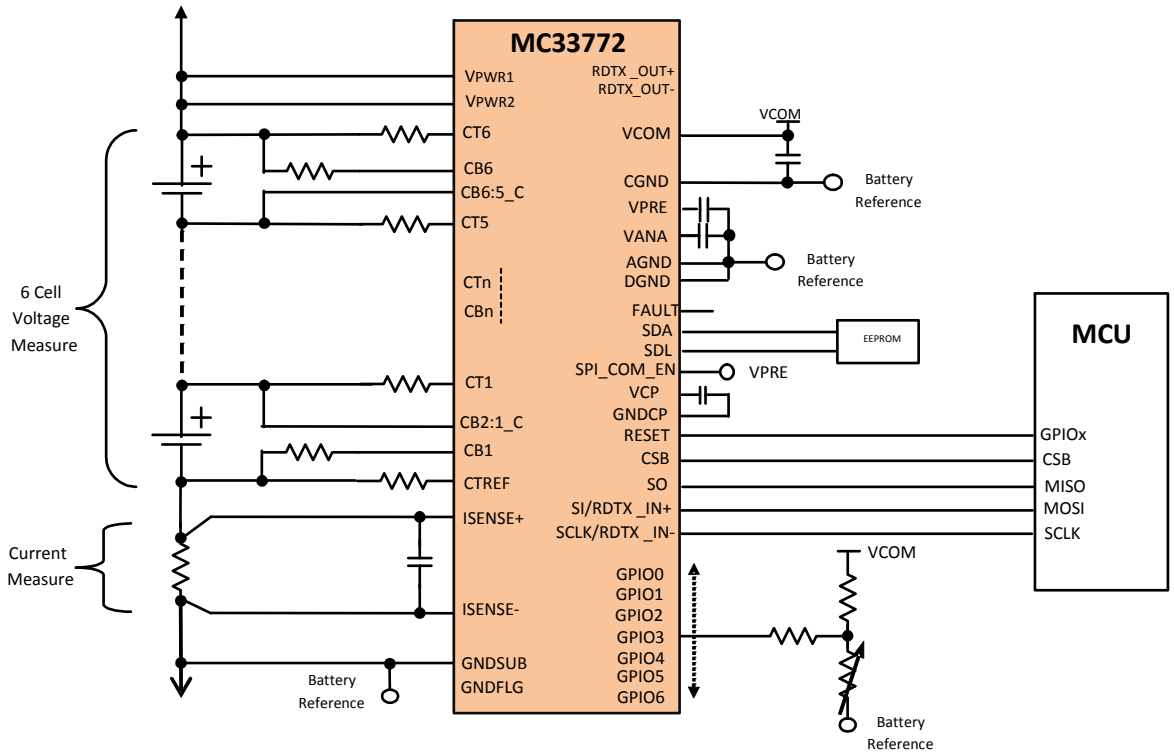


Figure 1. Simplified application diagram of SPI communication context

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

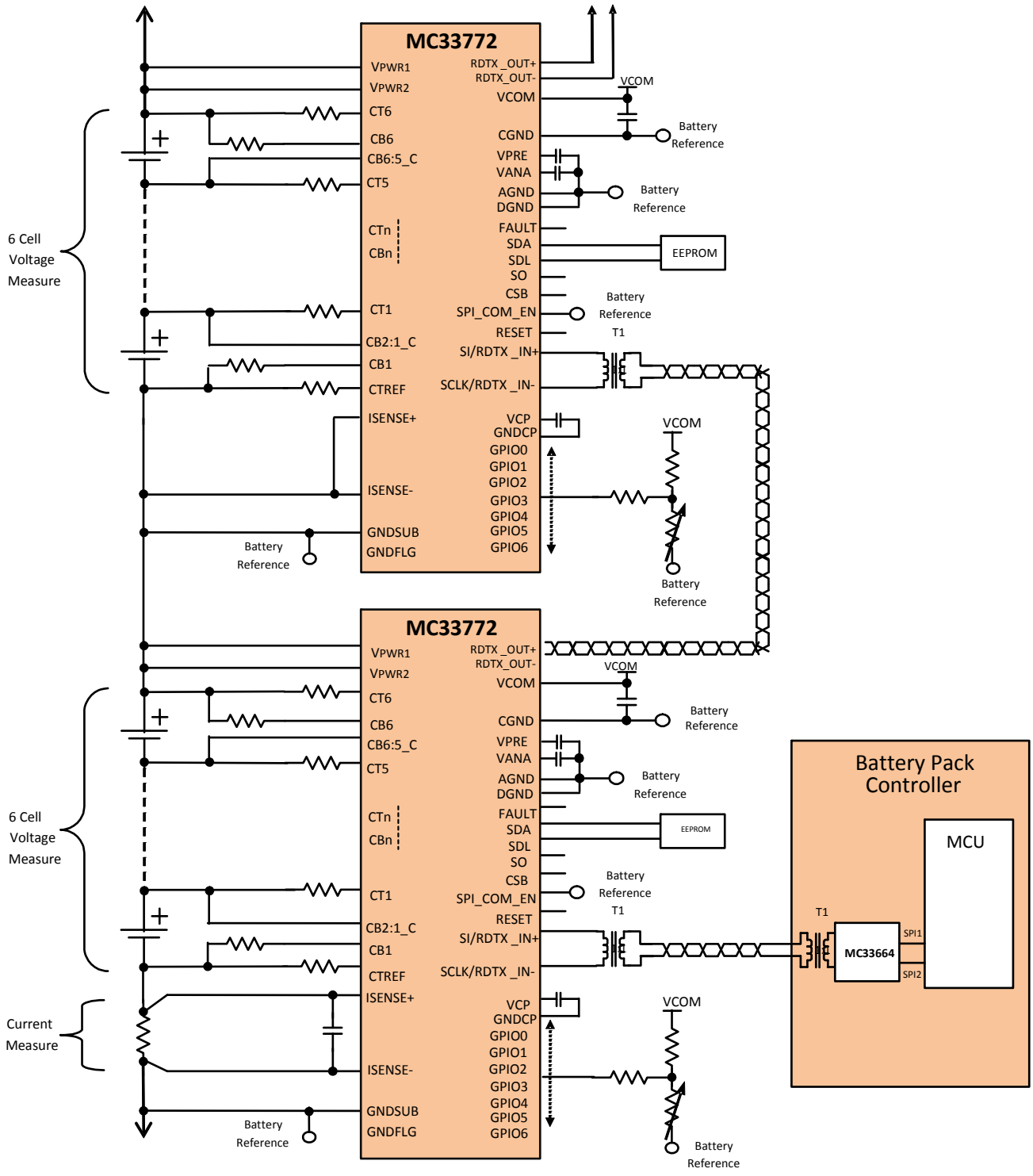


Figure 2. Simplified application diagram of twisted pair line communication with isolation transformers

Table 1. Orderable part variations

Part number [1]	Communication type	Calibration type	Temperature	Number of cells	Package
PC33772ASP1	SPI version	Type N	-40 °C to 125 °C	Three to six cells	48 Pin LQFP-EP
PC33772ATP1	TPL version				
PC33772ASP3	SPI version	Type F			
PC33772ATP3	TPL version				
PC33772ASP5	SPI version	Type T			
PC33772ATP5	TPL version				

Notes

1. To order parts in Tape & Reel, add the R2 suffix to the part number.

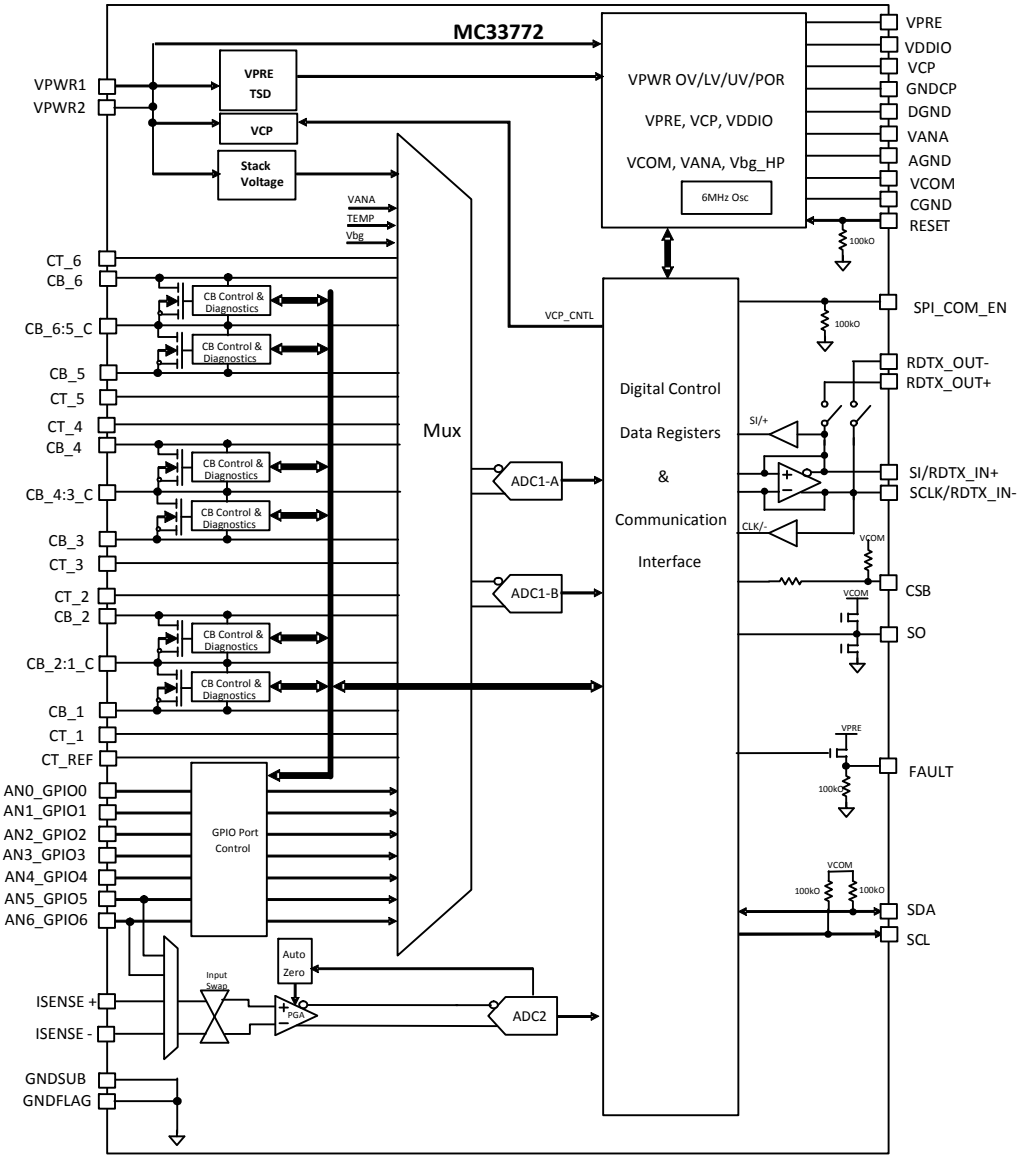


Figure 3. Simplified internal block diagram

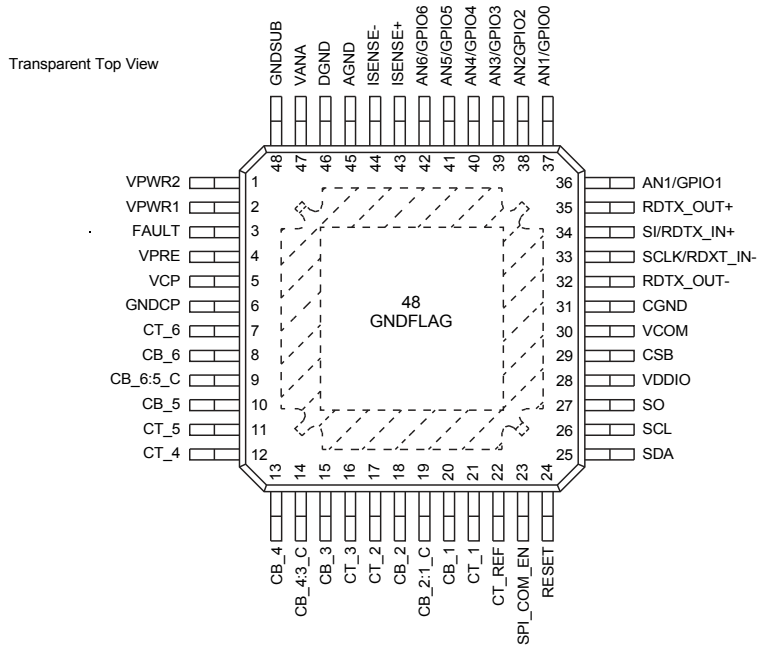


Figure 4. 33772 pinout diagram

Table 2. 33772 pin definitions

Pin number	Pin name	Definition
1	VPWR2	Power input to the 33772
2	VPWR1	Power input to the 33772
3	FAULT	Fault output dependent on user defined internal or external faults. If not used, it must be left open.
4	VPRE	Pre-regulator voltage. Connect to a 470 nF capacitor
5	VCP	Charge pump capacitor. Connect to a 10 nF
6	GNDCP	Charge pump capacitor ground
7	CT_6	Cell pin 6 input. Terminate to LPF resistor
8	CB_6	Cell balance driver. Terminate to cell 6 cell balance load resistor
9	CB_6:5_C	Cell balance 6:5 common. Terminate to cell 6 & 5 common pin
10	CB_5	Cell balance driver. Terminate to cell 5 cell balance load resistor
11	CT_5	Cell pin 5 input. Terminate to LPF resistor
12	CT_4	Cell pin 4 input. Terminate to LPF resistor
13	CB_4	Cell balance driver. Terminate to cell 4 cell balance load resistor
14	CB_4:3_C	Cell balance 4:3 common. Terminate to cell 4 & 3 common pin
15	CB_3	Cell balance driver. Terminate to cell 3 cell balance load resistor
16	CT_3	Cell pin 3 input. Terminate to LPF resistor

Pin number	Pin name	Definition
17	CT_2	Cell pin 2 input. Terminate to LPF resistor
18	CB_2	Cell balance driver. Terminate to cell 2 cell balance load resistor
19	CB_2:1_C	Cell Balance 2:1 common. Terminate to cell 2 & 1 common pin
20	CB_1	Cell balance driver. Terminate to cell 1 cell balance load resistor
21	CT_1	Cell pin 1 input. Terminate to LPF resistor
22	CT_REF	Cell pin REF input. Terminate to LPF resistor
23	SPI_COM_EN	SPI communication enable, pin must be high for SPI to be active.
24	RESET	RESET is an active high input. RESET has an internal pull-down. If not used, it can be tied to GND.
25	SDA	I^2C data
26	SCL	I^2C clock
27	SO	SPI serial output
28	VDDIO	IO voltage for I^2C and SPI interfaces. Voltage level corresponding to Logic 1 are the same as VDDIO
29	CSB	SPI chip select
30	VCOM	Communication regulator output, decouple with 2.2 µF ceramic
31	CGND	Communication decoupling ground, terminate to GNDSUB
32	RDTX_OUT-	Receive/transmit output negative

Table 2. 33772 pin definitions (continued)

Pin number	Pin name	Definition
33	SCLK/RDTX_IN-	SPI clock or receive/transmit input negative
34	SI/RDTX_IN+	SPI serial input or receiver/transmit input positive
35	RDTX_OUT+	Receive/transmit output positive
36	AN0/GPIO0	General purpose analog input or GPIO
37	AN1/GPIO1	General purpose analog input or GPIO
38	AN2/GPIO2	General purpose analog input or GPIO
39	AN3/GPIO3	General purpose analog input or GPIO
40	AN4/GPIO4	General purpose analog input or GPIO
41	AN5/GPIO5	General purpose analog input or GPIO
42	AN6/GPIO6	General purpose analog input or GPIO
43	ISENSE+	Current measurement input+
44	ISENSE-	Current measurement input–
45	AGND	Analog ground, terminate to GNDSUB
46	DGND	Digital ground, terminate to GNDSUB
47	VANA	Precision ADC analog supply. Decouple with ceramic 47 nF ceramic capacitor to AGND
48	GNDSUB	Ground reference for device, terminate to reference of battery cluster. Note: GNDREF is an alias of it.
49	GNDFLAG	Device flag, terminate to lowest potential of battery cluster

Table 3. Key parameters

Characteristics noted under SPI mode conditions 5.0 V ≤ V_{PWR} ≤ 30 V, TPL mode: 7.0 V ≤ V_{PWR} ≤ 30 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.
Before starting any development, it is recommended to request a copy of the full 33772 data sheet.

Symbol	Characteristic	Typ.	Unit	Notes
Power management				
I_{VPWR}	Supply Current (base value) • Normal mode, Cell Balance OFF, ADC Inactive, Communication Inactive, I_{VCOM} = 0 mA	5.8	mA	
$I_{VPWR(CBON)}$	Supply Current adder to set all 6 Cell Balance switches ON	0.97	mA	
$I_{VPWR(ADC)}$	Delta Supply Current to perform ADC conversions (addend) • ADC1-A,B continuously converting • ADC2 continuously converting	 2.9 1.17	mA	
$I_{VPWR(SS)}$	Supply Current in Sleep mode, Communication Inactive, Cell Balance OFF, Oscillator Monitor ON • SPI mode • TPL mode	 32 50	µA	
$t_{VPWR(FILTER)}$	V_{PWR} OV, LV, UV Filter	50	µs	
VPRE power supply				
$V_{VPRE(UV\_TH)}$	Undervoltage Threshold for V_{CP} minus V_{PRE}	4.25	V	
VCP power supply				
$V_{CP(UV\_TH)}$	Undervoltage Threshold for V_{CP} minus V_{PRE}	1.5	V	
VCOM power supply				
V_{COM}	VCOM Output Voltage	5.0	V	
$V_{COM(UV)}$	VCOM Undervoltage Fault Threshold	4.5	V	
V_{COM_HYS}	VCOM Undervoltage Hysteresis	100	mV	
VDDIO power supply				
$t_{VCOM(FLT\_TIMER)}$	VCOM Undervoltage Fault Timer	10	µs	
$t_{VCOM(RETRY)}$	VCOM Fault Retry Timer	10	ms	
$R_{VCOM(SS)}$	VCOM Sleep Mode Pull-down Resistor	2.0	kΩ	

Table 3. Key parameters (continued)

Characteristics noted under SPI mode conditions 5.0 V ≤ V_{PWR} ≤ 30 V, TPL mode: 7.0 V ≤ V_{PWR} ≤ 30 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.
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Symbol	Characteristic	Typ.	Unit	Notes
VANA power supply				
V_{ANA}	VANA Output Voltage (NOT USED BY EXTERNAL CIRCUITS) • Decouple with 47 nF X7R 0603 or 0402	2.65	V	
$V_{ANA(UV)}$	VANA Undervoltage Fault Threshold	2.4	V	
V_{ANA_HYS}	VANA Undervoltage Hysteresis	50	mV	
$t_{VANA(FLT\_TIMER)}$	VANA Undervoltage Fault Timer	11	µs	
$V_{ANA\ (OV)}$	VANA Overvoltage Fault Threshold	2.8	V	
$t_{VANA(RETRY)}$	VANA Fault Retry Timer	10	ms	
R_{VANA_RPD}	VANA Sleep Mode Pull-down Resistor	1.0	kΩ	
ADC1-A, ADC1-B				
$CTn_{(LEAKAGE)}$	Cell Terminal Input Leakage Current	10	nA	
$CTn_{(FV)}$	Cell Terminal Input Current - Functional Verification	1.0	mA	
CT_N	Cell Terminal Input Current During Conversion	100	nA	
R_{PD}	Cell Terminal Open Load Detection Pull-down Resistor	950	Ω	
V_{VPWR_RES}	VPWR Terminal Measurement Resolution	2.4415	mV/LSB	
$V_{CT\_ANx\_RES}$	Cell Voltage and ANx Resolution in 15-bits MEAS_xxxx registers	152.5925	µV/LSB	
t_{VCONV}	Single Channel Net Conversion Time • 16-Bit Resolution	25.36	µs	
V_{V_NOISE}	• 16-Bit Resolution	400	µVrms	
ADC2/current sense module				
I_{ISENSE_OL}	ISENSE Open Load injected current	130	µA	
V_{ISENSE_OL}	ISENSE Open Load detection threshold	460	mV	
V_{2RES}	ADC Resolution	0.6	µV/LSB	
V_{PGA_SAT}	PGA saturation half-range • Gain = 256 • Gain = 64 • Gain = 16 • Gain = 4	 4.9 19.5 78.1 150.0	mV	
V_{PGA_ITH}	Voltage threshold for PGA gain increase • Gain = 256 • Gain = 64 • Gain = 16 • Gain = 4	 - 2.344 9.375 37.50	mV	
V_{PGA_DTH}	Voltage threshold for PGA gain decrease • Gain = 256 • Gain = 64 • Gain = 16 • Gain = 4	 4.298 17.188 68.750 -	mV	
t_{PGA_SETTLE}	PGA settling time after a chopper event	14.0	µs	
t_{ICONV}	ADC Conversion Time including PGA settling time • 16-Bit Resolution	37.67	µs	
V_{I_NOISE}	Noise at 16-bit Conversion	3.01	µVrms	

Table 3. Key parameters (continued)

Characteristics noted under SPI mode conditions 5.0 V ≤ V_{PWR} ≤ 30 V, TPL mode: 7.0 V ≤ V_{PWR} ≤ 30 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.
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Symbol	Characteristic	Typ.	Unit	Notes
ADC2/current sense module (continued)				
V_{I_NOISE}	Noise Error at 13-bit Conversion	8.33	µVrms	
ADC_{CLK}	ADC2 and ADC1-A,B Clocking Frequency	6.0	MHz	
Cell balance drivers				
$V_{DS(CLAMP)}$	Cell Balance Driver VDS Active Clamp Voltage • Clamp Energy tbd	11	V	
$V_{OUT(FLT\_TH)}$	Output Fault Detection Voltage Threshold • Balance OFF (Open Load) • Balance ON (Shorted Load)	0.55	V	
R_{PD_CB}	Output OFF Open Load Detection Pull-down Resistor • Balance OFF, Open Load Detect Disabled	2.0	kΩ	
$R_{DS(on)}$	Drain-to-Source ON Resistance • I_{OUT} = 300 mA, T_J = 105 °C • I_{OUT} = 300 mA, T_J = 25 °C • I_{OUT} = 300 mA, T_J = -40 °C	– 0.5 0.4	Ω	
t_{ON}	Cell Balance Driver Turn On • R_L = 15 Ω	350	µs	
t_{OFF}	Cell Balance Driver Turn Off • R_L = 15 Ω	200	µs	
$t_{BAL\_DEGLICTH}$	Short/Open Detect Filter Time	20	µs	
Internal temperature measurement				
IC_TEMP1_RES	IC Temperature Resolution	0.032	K/LSB	
T_{SD_TH}	Thermal Shutdown	170	°C	
T_{SD_HYS}	Thermal Shutdown Hysteresis	10	°C	
General purpose input/output GPIOx				
$V_{OL(TH)}$	Analog Input Open Pin Detect Threshold	0.15	V	
R_{OPENPU}	Internal Open detection Pull-down Resistor	5.0	kΩ	
	GPIO0 WU De-glitch Filter	50	µs	
	GPIO0 Daisy Chain De-glitch Filter both edges	20	µs	
	GPIO2 Convert Trigger De-glitch Filter	2.0	µs	
Reset input				
$t_{RESETFLT}$	RESET De-glitch Filter	100	µs	
R_{RESET_PD}	Input Logic Pull-down (RESET)	100	kΩ	
SPI_COM_EN input				
V_{HYS}	Input Hysteresis	125	mV	
$R_{SPI\_COM\_EN\_PD}$	Input Pull-down Resistor (SPI_COM_EN)	100	kΩ	
Bus switch for TPL communication				
RX_{TERM}	Bus Termination Resistor (open resistor when bus switch is closed)	300	Ω	

Remark: if the bus switch is closed, the termination resistor is open, else the termination resistor is connected. At the end of the daisy chain the switch must be open, so the transmission line is properly terminated.

Table 3. Key parameters (continued)

Characteristics noted under SPI mode conditions 5.0 V ≤ V_{PWR} ≤ 30 V, TPL mode: 7.0 V ≤ V_{PWR} ≤ 30 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.
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Symbol	Characteristic	Typ.	Unit	Notes
Digital interface				
	FAULT Output (High Active, I_{OH} = 1.0 mA)	4.9	V	
	FAULT Output Pull-down Resistance	100	kΩ	
V_{HYS}	Input Hysteresis • SI/RDTX_IN+, SCLK/RDTX_IN-, CSB, SDA, SCL	80	mV	
R_{SCLK_PD}	Input Logic Pull-down Resistance (SCLK/RDTX_IN-, SI/RDTX+)	20	kΩ	
$R_{\_PU}$	Input Logic Pull-up Resistance to V_{COM} (CSB, SDA, SCL)	100	kΩ	
CSB_{WU_FLT}	CSB Wake-up De-glitch Filter, Low to High Transition	50	µs	
System timing				
t_{CELL_CONV}	Time needed to acquire all 6 cell voltages and the current after an on demand conversion • 16-Bit Resolution	208	µs	
t_{SYNC}	V/I time synchronization • ADC1-A,B at 16-Bit, ADC2 at 16-Bit	113	µs	
t_{WAKE_DELAY}	Time between wake pulses	600	µs	
t_{IDLE}	Idle time out after POR	60	s	
t_{WAKE_INIT}	Wake-up signaling time out after POR	0.75	s	
t_{DIAG}	Diagnostic Mode Time-out	1.0	s	
t_{EOC}	SOC to Data Ready (includes post processing of data) • 16-Bit Resolution	520	µs	
t_{SETTLE}	Time after SOC to begin converting with ADC1-A,b	12.28	µs	
t_{CLST_TPL}	Time needed to send a SOC command and read back 6 cell voltages, 7 temperatures, 1 current, 1 Coulomb counter with TPL communication working at 2.0 Mbps and ADC1-A,B configured as follows: • 16-Bit Resolution	1.16	ms	
t_{CLST_SPI}	Time needed to send a SOC command and read back 6 cell voltages, 7 temperatures, 1 current, 1 Coulomb counter with SPI communication working at 4.0 Mbps and ADC1-A,B configured as follows: • 16-Bit Resolution	0.86	ms	
t_{I2C_ACCESS}	EEPROM Access Time, EEPROM Write (depends on device selection)	5.0	ms	
$t_{WAVE\_DC\_BITx}$	Daisy Chain Duty Cycle OFF Time • $t_{WAVE\_DC\_BITx}$ = 00	500	µs	
$t_{WAVE\_DC\_BITx}$	Daisy Chain Duty Cycle OFF Time • $t_{WAVE\_DC\_BITx}$ = 01	1.0	ms	
$t_{WAVE\_DC\_BITx}$	Daisy Chain Duty Cycle OFF Time • $t_{WAVE\_DC\_BITx}$ = 10	10	ms	
$t_{WAVE\_DC\_BITx}$	Daisy Chain Duty Cycle OFF Time • $t_{WAVE\_DC\_BITx}$ = 11	100	ms	
$t_{WAVE\_DC\_ON}$	Daisy Chain Duty Cycle ON Time	500	µs	
t_{SLEEP}	Time out to enter Sleep Mode in the absence of TPL communication	1024	ms	

Table 3. Key parameters (continued)

Characteristics noted under SPI mode conditions 5.0 V ≤ V_{PWR} ≤ 30 V, TPL mode: 7.0 V ≤ V_{PWR} ≤ 30 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.
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Symbol	Characteristic	Typ.	Unit	Notes
Transformer interface				
t_{RES}	Slave Response After Write Command (echo)	2.35	µs	
	Time Between Slave Response Messages (Q)	1.5	µs	
	Start of Message (S)	500	ns	
	Start of Message Delay (T)	250	ns	
	Bit Time (U)	250	ns	
	Bit Delay (V)	250	ns	
	Message Duration (R)	21.25	µs	
$VRDTX_{INTH}$	Differential Receiver Threshold	0.74	V	
$VRDTX_{INHYS}$	Differential Receiver Threshold Hysteresis	130	mV	
$V_{RDTX(PK\_DIFF)}$	Amplifier Differential Output Voltage	2.5	V	
V_{RDTX_BIAS}	Transformer Bias Voltage • Driver tri-state	2.5	V	

Revision	Date	Description of changes
2.0	8/2016	• Added revision history table.

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