

## **TRF4900** RF Evaluation Kit

## User's Guide

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Mixed-Signal RF Products

SWRU003B

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#### Preface

## **Read This First**

#### About This Manual

This document is intended to introduce the TRF4900 evaluation module (EVM) and familiarize the reader with setting up and testing the TRF4900 EVM using the evaluation software in a typical laboratory environment.

#### How to Use This Manual

This document contains the following chapters:

- □ Chapter 1 Overview
- □ Chapter 2 Evaluation Board
- □ Chapter 3 Software User's Guide

#### Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to <u>you</u>.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

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## Chapter 1

## **Overview**

This chapter provides an overview of the TRF4900 evaluation module (EVM).

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#### 1.1 Purpose

The TRF4900 evaluation module (EVM) provides a platform for lab prototype evaluation of the Texas Instruments TRF4900.

The TRF4900 EVM board evaluates the RF performance of the TRF4900. It contains a PC parallel port interface and operates from 850 MHz to 950 MHz from 2.2 V to 3.6 V. The TRF4900 EVM contains two SMA connectors that allow the user to observe transmitted data, to test the VCO tuning range, or to feed in an external RF input. The transmitted data can be viewed on a spectrum analyzer as either a single output frequency or in FSK mode at data rates up to 30 kbps. Although higher data rates are achievable with the TRF4900, the TRF4900 EVM is designed to operate at data rates up to 30 kbps at room temperature.

#### 1.2 EVM Setup

The 3.5-inch diskette supplied with the TRF4900 contains the software required to demonstrate the TRF4900. Complete the following steps to set up the TRF4900 for evaluation.

- **Step 1:** Place the 3.5-inch diskette into the floppy disk drive of the computer being used to evaluate the TRF4900.
- Step 2: Copy the TRF4900.exe file to the hard drive.
- Step 3: Connect a DB25 female to a DB25 male cable between the TRF4900 evaluation board and the PC parallel port. The DB25 female end of the cable is connected to the TRF4900. The DB25 male end of the cable is connected to the desired LPT port of the PC (LPT1 or LPT2).
- **Step 4:** Connect a dc power supply capable of 10 V 200 mA between the red power supply pin and ground on the TRF4900 evaluation board.
- Step 5: Verify that the power supply output is set to 8 V.
- Step 6: Turn the power supply on.
- **Step 7:** If the jumper at JP4 is installed, verify that LED3 (the red power on LED) is illuminated.
- Step 8: Run the TRF4900.exe file on the PC.
- Step 9: Press the Send Words Now (F12) button located on the main program screen.
- Step 10: Verify that LED1 (the green lock detect LED) is illuminated. When the lock detect LED is illuminated, the PLL is locked on frequency.

#### Note:

The actual icons/windows on the computer screen may differ from those shown in the user's guide, due to software version upgrades.

The schematics shown in this user's guide may not match the current revision, due to PCB and component upgrades.

Always check the TI website for the latest schematics and software.

#### 1.3 Block Diagram

Figure 1–1 shows the block diagram for the TRF4900.



Figure 1–1. TRF4900 Block Diagram

## Chapter 2

## **Evaluation Board**

This chapter describes the EVM and its operation.

#### Topic

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#### 2.1 Schematics



NOTES: 1 DNP: DO NOT PLACE 2 TBD: TO BE DETERMINED 3 SAT: SELECT AT TEST



#### 2.1.1 Top Side Silkscreen and Drawing





#### 2.1.2 Bottom Side Silkscreen and Drawing

2.2 F	arts Lis	st						
Count	RefDes	Value	PatternName	Description	Manufacturer	Part Number	Distributor	Distributor P/N
2	C19	0.01 μF	0603	Ceramic chip capacitor	Venkel	C0603X7R500-103KNB	Venkel	C0603X7R500-103KNB
	C22	0.01 μF	0603	Ceramic chip capacitor	Venkel	C0603X7R500-103KNB	Venkel	C0603X7R500-103KNB
7	ß	0.1 µF	0603	Ceramic chip capacitor	Venkel	C0603Y5V160-104ZNB	Venkel	C0603Y5V160-104ZNB
	C5	0.1 µF	0603	Ceramic chip capacitor	Venkel	C0603Y5V160-104ZNB	Venkel	C0603Y5V160-104ZNB
	C7	0.1 µF	0603	Ceramic chip capacitor	Venkel	C0603Y5V160-104ZNB	Venkel	C0603Y5V160-104ZNB
	C14	0.1 µF	0603	Ceramic chip capacitor	Venkel	C0603Y5V160-104ZNB	Venkel	C0603Y5V160-104ZNB
	C16	0.1 µF	0603	Ceramic chip capacitor	Venkel	C0603Y5V160-104ZNB	Venkel	C0603Y5V160-104ZNB
	C18	0.1 μF	0603	Ceramic chip capacitor	Venkel	C0603Y5V160-104ZNB	Venkel	C0603Y5V160-104ZNB
	C21	0.1 μF	0603	Ceramic chip capacitor	Venkel	C0603Y5V160-104ZNB	Venkel	C0603Y5V160-104ZNB
2	C17	1 µF	1206 Tantalum	Tantalum capacitor				
	C20	1 µF	1206 Tantalum	Tantalum capacitor				
Ł	C13	1.5 –10 pF	9341 SERIES	Trimmer capacitor	Johanson	9341–3SL	Newark	95F9901
с	C4	3.3 pF	0603	Ceramic chip capacitor	Venkel	C0603COG500-3R3CNB	Venkel	C0603COG500-3R3CNB
	C8	3.3 pF	0603	Ceramic chip capacitor	Venkel	C0603COG500-3R3CNB	Venkel	C0603COG500-3R3CNB
	C3	3.3 pF	0603	Ceramic chip capacitor	Venkel	C0603COG500-3R3CNB	Venkel	C0603COG500-3R3CNB
2	C11	10 pF	0603	Ceramic chip capacitor	Venkel	C0603COG500-100JNB	Venkel	C0603COG500-100JNB
	C12	10 pF	0603	Ceramic chip capacitor	Venkel	C0603COG500-100JNB	Venkel	C0603COG500-100JNB
٢	C15	10 μF	6032 C case	Tantalum capacitor				
٢	C6	120 pF	0603	Ceramic chip capacitor	Venkel	C0603COG500-121JNB	Venkel	C0603COG500-121JNB
٢	C2	470 pF	0603	Ceramic chip capacitor	Venkel	C0603X7R500-471JNB	Venkel	C0603X7R500-471JNB
٢	C10	1000 pF	0603	Ceramic chip capacitor	Venkel	C0603X7R500-102KNB	Venkel	C0603X7R500-102KNB
۲	G	4700 pF	0603	Ceramic chip capacitor	Venkel	C0603X7R500-472KNB	Venkel	C0603X7R500-472KNB
-	ca1	25.6 MHz	HC45/U gull wing	Resistance weld miniature crystal	International Crystal Mfg.	865842		
٢	CQ1_A1		CX-1-SM	Surface-mount quartz crystal	CFP – (CMAC frequency products)	18 MHz CX-1 SMI		
1	CQ1_B1		ATS-SM series	Crystal	CTS Reeves	ATS256SM-T	Digi-Key	CTX51?TR-ND
4	CR1		MELF3 (MINIMELF)	Fast switching diode	Diode INC	LL4148	Digi-Key	LL4148CT-ND

Count	RefDes	Value	PatternName	Description	Manufacturer	Part Number	Distributor	Distributor P/N
4	CR2		MELF3 (MINIMELF)	Fast switching diode	Diode INC	LL4148	Digi-Key	LL4148CT-ND
	CR3		MELF3 (MINIMELF)	Fast switching diode	Diode INC	LL4148	Digi-Key	LL4148CT-ND
	CR4		MELF3 (MINIMELF)	Fast switching diode	Diode INC	LL4148	Digi-Key	LL4148CT-ND
1	CR5		SMB	Rectifier	Diode INC	S1JBT	Digi-Key	S1JBDICT-ND
1	IC1		TSSOP24_M	Single chip RF transmitter	Texas Instruments	TRF4900		
1	IC2		SO20WB	Octal buffers and line drivers with 3-state outputs	Texas Instruments	SN74LVT244BDW	Digi-Key	296-1707-5-ND
2	J1		SMA_H	SMA brass connector – horizontal/PC mount	Johnson Components	142-0701-801	Newark	90F2624
	J2		SMA_H	SMA brass connector – horizontal/PC mount	Johnson Components	142-0701-801	Newark	90F2624
2	JP2		Jumper-3 pin	Breakaway headers	AMP	4-103239-0	Newark	90F7725
	JP3		Jumper-3 pin	Breakaway headers	AMP	4-103239-0	Newark	90F7725
1	L1	6.8 nH	0603	Surface-mount inductor	Murata	LQW1608		
1	L2	10 nH	0603	Surface-mount inductor	Murata	LQW1608		
-	LED1	LDET	LED, S type	Surface-mount LED-Gull wing-S type-green	Panasonic	LN1371SG-(TR)	Digi-Key	P516CT-ND
-	LED2	Enable	LED, S type	Surface-mount LED-Gull wing-S type-amber	Panasonic	LN1471SY-(TR)	Digi-Key	P517CT-ND
-	LED3	VCC	LED, S type	Surface-mount LED-Gull wing-S type-red	Panasonic	LN1271R–(TR)	Digi-Key	P490CT-ND
٦	P1		DB25M	Subminiature D connector	AMP	745783-4	Newark	90F5485
7	JP1	0	0603	Chip resistor	Venkel	CR0603-16W-000B	Venkel	CR0603-16W-000B
	JP4	0	0603	Chip resistor	Venkel	CR0603-16W-000B	Venkel	CR0603-16W-000B
٢	R7	1.0M	0603	Chip resistor	Venkel	CR0603-16W-105JB	Venkel	CR0603-16W-105JB
-	R1	6.2k	0603	Chip resistor	Venkel	CR0603-16W-622JB	Venkel	CR0603-16W-622JB

Count	RefDes	Value	PatternName	Description	Manufacturer	Part Number	Distributor	Distributor P/N
14	R5	10k	0603	Chip resistor	Venkel	CR0603-16W-103JB	Venkel	CR0603-16W-103JB
	R6	10k	0603	Chip resistor	Venkel	CR0603-16W-103JB	Venkel	CR0603-16W-103JB
	R15	10k	0603	Chip resistor	Venkel	CR0603-16W-103JB	Venkel	CR0603-16W-103JB
	R16	10k	0603	Chip resistor	Venkel	CR0603-16W-103JB	Venkel	CR0603-16W-103JB
	R17	10k	0603	Chip resistor	Venkel	CR0603-16W-103JB	Venkel	CR0603-16W-103JB
	R19	10k	0603	Chip resistor	Venkel	CR0603-16W-103JB	Venkel	CR0603-16W-103JB
	R20	10k	0603	Chip resistor	Venkel	CR0603-16W-103JB	Venkel	CR0603-16W-103JB
	R21	10k	0603	Chip resistor	Venkel	CR0603-16W-103JB	Venkel	CR0603-16W-103JB
	R22	10k	0603	Chip resistor	Venkel	CR0603-16W-103JB	Venkel	CR0603-16W-103JB
	R23	10k	0603	Chip resistor	Venkel	CR0603-16W-103JB	Venkel	CR0603-16W-103JB
	R24	10k	0603	Chip resistor	Venkel	CR0603-16W-103JB	Venkel	CR0603-16W-103JB
	R28	10k	0603	Chip resistor	Venkel	CR0603-16W-103JB	Venkel	CR0603-16W-103JB
	R29	10k	0603	Chip resistor	Venkel	CR0603-16W-103JB	Venkel	CR0603-16W-103JB
	R30	10k	0603	Chip resistor	Venkel	CR0603-16W-103JB	Venkel	CR0603-16W-103JB
-	R3	51	0603	Chip resistor	Venkel	CR0603-16W-510JB	Venkel	CR0603-16W-510JB
9	R4	100	0603	Chip resistor	Venkel	CR0603-16W-101JB	Venkel	CR0603-16W-101JB
	R12	100	0603	Chip resistor	Venkel	CR0603-16W-101JB	Venkel	CR0603-16W-101JB
	R13	100	0603	Chip resistor	Venkel	CR0603-16W-101JB	Venkel	CR0603-16W-101JB
	R14	100	0603	Chip resistor	Venkel	CR0603-16W-101JB	Venkel	CR0603-16W-101JB
	R26	100	0603	Chip resistor	Venkel	CR0603-16W-101JB	Venkel	CR0603-16W-101JB
	R27	100	0603	Chip resistor	Venkel	CR0603-16W-101JB	Venkel	CR0603-16W-101JB
2	R2, R38	100k	0603	Chip resistor	Venkel	CR0603-16W-104JB	Venkel	CR0603-16W-104JB
з	R33	220	0603	Chip resistor	Venkel	CR0603-16W-221JB	Venkel	CR0603-16W-221JB
	R34	220	0603	Chip resistor	Venkel	CR0603-16W-221JB	Venkel	CR0603-16W-221JB
	R35	220	0603	Chip resistor	Venkel	CR0603-16W-221JB	Venkel	CR0603-16W-221JB
2	R31	360	0603	Chip resistor	Venkel	CR0603-16W-361JB	Venkel	CR0603-16W-361JB
	R36	360	0603	Chip resistor	Venkel	CR0603-16W-361JB	Venkel	CR0603-16W-361JB
1	R32	500	P1S Panasonic	Surface-mount trimmer potentiometer	Panasonic	#EVM-1SSX50BXX	Digi-Key	P1S501CT-ND
2	R18	510	0603	Chip resistor	Venkel	CR0603-16W-511JB	Venkel	CR0603-16W-511JB
	R25	510	0603	Chip resistor	Venkel	CR0603-16W-511JB	Venkel	CR0603-16W-511JB

Count	RefDes	Value	PatternName	Description	Manufacturer	Part Number	Distributor	Distributor P/N
4	R8	TBD	0603	Chip resistor	Venkel		Venkel	
	R9	TBD	0603	Chip resistor	Venkel		Venkel	
	R10	TBD	0603	Chip resistor	Venkel		Venkel	
	R11	TBD	0603	Chip resistor	Venkel		Venkel	
5	71		SC-79	Hyperabrupt tuning varactor	Alpha Industries	SMV1247-079	Nu Horizons Electronic Corp.	SMV1247-079
	V2		SC-79	Hyperabrupt tuning varactor	Alpha Industries	SMV1247-079	Nu Horizons Electronic Corp.	SMV1247-079
٦	VR1		DPAK CASE369A-13	Three-terminal adustable output positive voltage regulator	On Semiconductor	LM317MDT	Newark	06F9320
٢	VR2		SO8NB	Three-terminal adustable output positive voltage regulator	On Semicondictor	LM317LBD	Newark	06F9304
1	ZR1		SMBJ-BI	Transient voltage suppressor	Vishay/Liteon	SMBJ8.5CA	Digi-Key	SMBJ8.5AGICT-ND
1	8.0V	RED	PC test point	Color coded PC test point (red)	Components Corp.	TP-105-01-02	Newark	97B3257
80	CLOCK	WHT	PC test point	Color coded PC test point (white)	Components Corp.	TP-105-01-09	Newark	97B3253
	DATA	WHT	PC test point	Color coded PC test point (white)	Components Corp.	TP-105-01-09	Newark	97B3253
	LDET	WHT	PC test point	Color coded PC test point (white)	Components Corp.	TP-105-01-09	Newark	97B3253
	MODE	WHT	PC test point	Color coded PC test point (white)	Components Corp.	TP-105-01-09	Newark	97B3253
	STDBY	WHT	PC test point	Color coded PC test point (white)	Components Corp.	TP-105-01-09	Newark	97B3253
	STROBE	WHT	PC test point	Color coded PC test point (white)	Components Corp.	TP-105-01-09	Newark	97B3253
	TXDATA	WHT	PC test point	Color coded PC test point (white)	Components Corp.	TP-105-01-09	Newark	97B3253
	TP1	WHT	PC test point	Color coded PC test point (white)	Components Corp.	TP-105-01-09	Newark	97B3253
3	TP2		SMD test point	Surface-mount test point	Components Corp.	TP-107-01	Newark	97B2647
	TP3		SMD test point	Surface-mount test point	Components Corp.	TP-107-01	Newark	97B2647
	TP4		SMD test point	Surface-mount test point	Components Corp.	TP-107-01	Newark	97B2647
4	FOOT1		Hardware	Bumpon hemisphere $0.44 \times 20$ clear	Electronic Specialty Markets/3M	70070107373	Digi-Key	SJ5303-7-ND

#### 2.3 EVM DC Voltage Setup

The evaluation board should be used with a dc power supply voltage of 8 V nominal. Figure 2–1 details the dc voltage supply setup for the TRF4900 EVM.

#### Figure 2–1. TRF4900 EVM DC Voltage Setup



#### 2.4 Serial Interface and PC Port Pin Out

Figure 2–2 details the serial interface portion of the TRF4900 EVM.

#### Figure 2–2. TRF4900 EVM Serial Interface



P1 Computer Interface Connector Pin Number	Function
2	DATA
3	CLOCK
4	STROBE
5	MODE
7	STDBY
9	TXDATA
18 thru 25	Ground

#### 2.5 Standard PC Parallel Port

• • •
V
С
D

A standard PC parallel port is configured as follows:

View Is Looking at Connector Side of DB-25 Male Connector

#### Pin Description

1	Strobe	PC Output
2	Data 0	PC Output
3	Data 1	PC Output
4	Data 2	PC Output
5	Data 3	PC Output
6	Data 4	PC Output
7	Data 5	PC Output
8	Data 6	PC Output
9	Data 7	PC Output
10	ACK	PC Input
11	Busy	PC Input
12	Paper Empty	PC Input
13	Select	PC Input
14	Auto Feed	PC Output
15	Error	PC Input
16	Initialize Printer	PC Output
17	Select Input	PC Output

Pin Assignments Note: 8 Data Outputs

4 Misc Other Outputs

5 Data Inputs

Note: Pins 18–25 Are Ground

Note: The TRF4900 EVM uses pins 2–9 for signals from the PC to the EVM.

#### 2.6 Jumper Connections

The default position of the jumpers on the TRF4900 EVM are configured as shown below.



#### 2.6.1 Jumper Description

The jumpers on the TRF4900 EVM are used for the following purposes:

🗋 JP1

Jumper JP1 connects the VCO tank circuit to the loop filter of the PLL circuit. The only reason to remove jumper JP1 is to test the tuning range of the VCO tank circuit with an external power supply. The default state for jumper JP1 is JP1-1 to JP1-2. Jumper JP1 is a 0- $\Omega$  0603 resistor.

Jumper JP2 can be used to pull the STDBY line up to V<sub>CC</sub> (JP2-1 to JP2-2) or pull down to ground (JP2-2 to JP2-3), if a computer connection is not installed. The primary purpose for JP2 is as a test point to monitor the state of the STDBY line. The default state for jumper JP2 is not connected.

🗋 JP3

Jumper JP3 can be used to pull the MODE line up to V<sub>CC</sub> (JP3-1 to JP3-2) or pull down to ground (JP3-2 to JP3-3), if a computer connection is not installed. The primary purpose for JP3 is as a test point to monitor the state of the MODE line. The default state for jumper JP3 is not connected.

🗋 JP4

Jumper JP4 connects the Power-On LED to the output of the VR2 voltage regulator. The default state for jumper JP4 is JP4-1 to JP4-2. Jumper JP4 is a  $0-\Omega$ , 0603 resistor.

<sup>🗋</sup> JP2

#### 2.7 Connectors and Test Points

The following information describes the TRF4900 EVM connectors and test points.

#### 2.7.1 Connectors

🗋 P1

P1 is the PC parallel port interface and is a male DB25 connector. P1 is connected to the LPT1 or LPT2 port of the computer on which the TRF4900 software is running.

🗋 J1

TX\_OUT is an SMA female connector which is connected to the transmitter output of the TRF4900.

□ J2 VCO\_TANK

VCO\_TANK is an SMA female connector used with resistors R8, R9, R10, R11, and capacitor C6 to directly feed in an external VCO signal. Resistors R8, R9, R10, and R11 are used to form a *T* attenuator. The components for this option are not installed on the EVM.

#### 2.7.2 Test Points (TP)

🗋 TP1

Test point TP1 is used to monitor the tuning voltage applied to the VCO circuit by the PLL circuit.

- □ LDET TP The LDET test point is used to monitor the lock detect line of the TRF4900.
- MODE TP

The MODE test point is used to monitor the MODE line.

STDBY TP

The STDBY test point is used to monitor the STDBY line.

- CLOCK TP The CLOCK test point is used to monitor the CLOCK signal from the PC.
- DATA TP
   The DATA test point is used to monitor the DATA signal from the PC.

#### □ STROBE TP

The STROBE test point is used to monitor the STROBE signal from the PC.

□ TXDATA TP

The TXDATA test point is used to monitor the transmitted data. Transmit data from an external source can also be applied at this point.

#### 2.7.3 Adjustments

Resistor R32 is varied to adjust the VCC1 voltage applied to IC1 (TRF4900).

#### 2.7.4 LED Indicators

#### U VCC LED

If JP4 is installed, the VCC LED is illuminated when voltage is applied to IC1.

#### LDET LED

The LDET LED is illuminated when the lock detect line IC1–23 (TRF4900) is high, indicating that the PLL circuit is locked.

#### ENABLE LED

The ENABLE LED is illuminated when the STDBY line from the computer is in the high state.

## Chapter 3

## **Software User's Guide**

This chapter describes the Windows-based software application that accompanies the EVM.

#### Topic

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#### 3.1 Introduction

A Windows-based software application accompanies the evaluation board. The software is intended for use in either a Windows 95/98 or Windows NT environment. If the Windows NT environment is used, the Windows NT driver software must accompany the software. However, if the operating system is Windows 95/98, the software application can run on its own.

Both the Windows NT Driver and the TRF4900 software are provided on diskette. Your system administrator must install the Windows NT Driver if you do not have administrative privileges on your computer. The TRF4900 software can run from the floppy disk by following these steps:

- 1) Click on the Start button on the desktop
- 2) Click on the Run button
- 3) Type A:\ TRF4900.exe and press OK

#### 3.2 Main Program Screen

The screen shown in Figure 3–1 appears on your monitor.

#### Figure 3–1. Main Program Screen

Cry Fre	vstal or Clock equency	Transmit Fre	equency	Double Click Here With the Left Mouse Button to Obtain Chip Layout Screen
🛹 TRF4900 V2.3		Main Program		_ 🗆 ×
<u>File E</u> dit <u>G</u> o <u>H</u> elp				
CLK 25.6	Desired Freq. 915	- MHz	Help TRF4900 Cp	ntrol Software
PreScaler 256	Actual Freq. 915.000	0000 MHz	Double Click	HERE for a Chip Layout.
Mode Options PLL On	VCO On NF		Note: FM/FS automatically the LPF amp data switch i	K demodulator is y enabled if the limiter and lifier are enabled and the is set to FSK reception.
Pwr Amp 0 dB 💌		м Езк	Press Enter ( Words.	on Any Input to Send ALL
Output Parameters			Words	Send Words Now (F12)
Enable On	TXData Off	Mode 0	A 00100011	11011111100000000 Mpde 0
Clock Width 345	Strobe Widtl	h 675	B 01100011	11011111000000000 Mode 1
			⊂ 10111100	00001111000000000 Mode 1
Operation Mode:	Mode 0 TXData	:Off Chip On	D 11011111	11111111000000000 Mode 0
Computer	Printer Port	P	ress to Progra	am the TRF4900

NOTE: When word bits are displayed in RED, the Send Words Now (F12) button on the main program screen must be pressed for changes to be updated.

The main program screen is divided into seven main sections as follows:

#### 3.2.1 Synthesizer

This section is used to set the crystal/clock (CLK) frequency, the Desired Freq., and the PreScaler value of the divide-by-N of the PLL. From these inputs, the actual frequency and bit values of Words A and B are calculated.

#### 3.2.2 Mode Options

This section allows the user to control various features of the TRF4900. The following is a brief summary of the four controls.

- 1) PLL Turns the phase-locked loop on or off.
- 2) VCO The voltage controlled oscillator (VCO) is always on.
- 3) Pwr Amp Allows the power amp to be set to off, 20-dB attenuation, 10-dB attenuation, or 0-dB attenuation states.
- 4) LPT Port Allows the user to change between the LPT1 and the LPT2 ports of the controlling computer.

#### 3.2.3 Output Parameters

This section allows the user to turn the TRF4900 Enable, TXData, and Mode control lines on and off. When the mode control line is off, Mode 0 is defaulted. When the mode control line is on, Mode 1 is defaulted. Mode 0 initializes using Words A and D; Mode 1 initializes using Words B and C.

Clock Width and Strobe Width allow the clock and strobe pulse widths to be increased or decreased.

#### 3.2.4 PLL and MM Options

Allows the change of the APLL value (0, 20, 40...140), the NPLL value (256, 512), and the Modulation Mode (FSK).

#### 3.2.5 Help

Gives a brief description of each control box. For example, after clicking the PLL box in the Mode Options section on the main program screen, the Help box will read:

Phase-Lock Loop 0: Off 1: On Valid in Mode 0 or 1.

Most of the other control boxes follow this format. The first line indicates what portion of the TRF4900 is being controlled. The next two lines indicate the bit value. If the PLL is off, bit 12 of Words C and D are equal to 0. If it is on, bit 12 is equal to 1. The last line indicates this control works in both Mode 0 and Mode 1.

Double clicking in the Help box on the main program screen activates the chip layout screen.

#### 3.2.6 Words

This section updates the binary words after changes are made to the control options. Clicking on the box next to the word can individually send each word. Clicking on the *Send Words Now (F12)* button on the main program screen or pressing F12 on the keyboard, sends all the words to the TRF4900.

#### 3.2.7 Operation Mode

Operation mode shows whether the TRF4900 is enabled, which mode (0 or 1) is selected, and whether the transmit (TX) data line is on or off.

#### 3.2.8 Changing Values on the Main Program Screen

Synthesizer Section					
CLK	Type the desired clock frequency inside the box or use the arrows located at the right side of the box.				
Desired Freq.	Type the desired transmit or LO receive frequency inside the box or use the arrows located at the right side of the box.				
PreScaler	Click inside the box to change divide-by-N value between 256 and 512. The value of NPLL under PLL and MM Options changes when the PreScaler value changes.				
Mode Options					
PLL	Click inside the box to turn the PLL on or off (turn on for transmit).				
VCO	The VCO is always on. Clicking has no effect.				
Pwr Amp	Use the arrow at the side of the box to select the desired power amplifier attenuation.				
Output Parameters					
Enable	Click inside the box to turn the TRF4900 on or off.				
TXData	Click inside the box to switch the TXData line between high and low.				
Mode	Click inside the box to switch the mode line between 0 and 1.				
Clock Width	Type inside the box to increase or decrease the clock pulse width (this should not be changed during normal use).				
Strobe Width	Type inside the box to increase or decrease the strobe pulse width (this should not be changed during normal use).				

PLL and MM Options					
APLL:	Use the arrows beside the box to select from values of 0, 20, 40, 60, 80, 100, 120, and 140.				
NPLL:	Click inside the box to change the divide-by-N value between 256 and 512. The value of PreScaler under Synthesizer changes when the NPLL value changes.				
MM:	Modulation Mode is fixed to FSK Modulation Mode.				
LPT Port					
LPT_x:	Click inside the box to chose between PC parallel ports LPT 1 or LPT 2.				
Help					
Help:	When any box on the main program screen is selected (clicked inside of box with mouse), the Help screen displays the valid selections for that box. Double clicking inside the Help box cause the chip layout screen to be displayed as shown in Figure 3–2.				
	PLL and MM Op APLL: NPLL: MM: LPT Port LPT_x: Help Help:				

#### 3.3 Chip Layout Screen

The chip layout screen can be accessed by double clicking on the left mouse button in the Help section of the main program screen. The chip layout screen appears as a simplified internal schematic of the TRF4900 as shown in Figure 3–2.

Figure 3–2. Chip Layout Screen



- The Mode Options (e.g., the Power Amp, PLL, etc.) may be controlled from the chip layout screen, as well as from the main program screen. Changes made in either the main program screen or the chip layout screen simultaneously update both screens. The user can also control the chip enable, TXData, and mode control lines from the chip layout screen.
- □ The user can select FSK Modulation. The FSK Test button, located on the chip layout screen, will allow the user to transmit data using the TRF4900. Options for use with the FSK Test button are the pulse repetition frequency (PRF), which is defaulted to 100 Hz, and the Run Time (Min), which can be set in minutes. For example, if you want the test to run for five minutes, set Run Time (Min) to 5.
- □ The PLL/Modulation Options button brings up the PLL/Modulation Options screen as shown in Figure 3–3. This button is activated only when the PLL is on.

#### 3.4 PLL/Modulation Options Screen

The PLL/Modulation Options screen is accessed by pressing the PLL/Modulation Option button, located on the chip layout screen, and is displayed as shown in Figure 3–3.

#### Figure 3–3. PLL/Modulation Options Screen



The PLL/Modulations Options screen is divided into the following four sections:

🗋 APLL

Controls the acceleration factor for the PLL. The values are 0, 20, 40, 60, 80, 100, 120, and 140. Any changes are automatically updated in the PLL and MM Options section of the main program screen after pressing the *Send Bits* button located on the PLL screen.

D NPLL

Controls the N-Divider of the PLL. The NPLL can be set to either 256 or 512. Any changes are automatically updated in the NPLL box on the main program screen after pressing the *Send Bits* button located on the PLL screen.

Modulation Mode

Allows the user to select FSK modulation. Any changes are automatically updated in the MM box on the main program screen after pressing the *Send Bits* button located on the PLL screen.

□ FSK Frequency Register

This section acts as a calculator and sets bits 20–13 of Word D to the user defined bits. The bits of the FSK deviation register (DV7–DV0) can be set individually by double clicking inside each *DVx* box. After setting all bits, press the *Send Bits* button located on the PLL/Modulation Options screen. The bits of the frequency register will be mapped to Word D on the main program screen, and highlighted in green. Furthermore, Fout: TX\_Data High (MHz), Fout: TX\_Data Low (MHz) frequencies, and their difference (Delta Fout kHz), are calculated and displayed.

Press the *Send Bits* button located on the PLL/Modulation Options screen to program the TRF4900. Press the *Close* button to return to the chip layout screen.

#### 3.5 Testing of Transmitter

To test the transmitter section of the TRF4900, perform the following steps:

Step 1: Test Setup:

Set up the test bench as shown in Figure 3–4.

Figure 3–4. Block Diagram for Testing of the TRF4900 EVM Transmitter Section



#### Step 2: Software Programming:

To test the TRF4900 transmitter section, set the main program screen and the chip layout screen as shown in Figure 3–5 and Figure 3–6.

#### Figure 3–5. Main Program Screen

Transmit Frequency —	Double Click Here With Left Mouse Button to Obtain Chip Layout View			
TRF4900 V2.3  File Edit Go Help  Synthesizer	Main Program			
CLK 25.6 MHz Desired Freq, 915 Actual Freq, 915.00 PreScaler 256 Freq, Error 0	MHz 00000 MHz MHz Update CLK	TRF4900 Control Software Double Click HERE for a Chip Layout.		
Mode Options PLL On VCO On M	PLL and MM Options APLL 140 + NPLL 256	the LPF amplifier are enabled and the data switch is set to FSK reception.		
Pwr Amp 0 dB  LPT_X 1 Output Parameters		Words. Send Words Now (F12)		
Enable On TXData Off Clock Width 345 Strobe Wid	Mode 0	A         001000111011111000000000         Mode 0           B         011000111011111000000000         Mode 1		
Operation Mode: Mode 0 TXDat	a:Off Chip On	D 110111111111111000000000 Mode 0		

#### Chip Layout Screen of TRF4900 Software for Transmitter Testing





After setup is complete, press the *Send Words* button on the chip layout screen or the *Send Words Now (F12)* button on the main program screen to send the programming words to the TRF4900.

#### Step 3: Spectrum Analyzer Setup and Clock Offset Procedure

Setup the spectrum analyzer to observe the following:



#### Figure 3–7. Spectrum Analyzer

#### **Clock Offset Procedure**

- 1) Use the test setup as shown in Figure 3–4 and transmitter software setup shown in Figure 3–5 and Figure 3–6.
- 2) Observe the frequency reading on the frequency counter.
- 3) Subtract 915.000000 MHz from the frequency counter reading.
- 4) Enter the difference value in the Freq. Error box in the main program screen as shown in Figure 3–8.
- Note: If the difference value is negative, enter sign, followed by the difference value.
   Example: Frequency counter reading is 914.996000 MHz
   Subtracting 915.000 MHz from 914.996 MHz will yield

   a difference of –4000 Hz. This difference is entered in the Freq. Error block as –0.004 MHz (see Figure 3–8).
- 6) Press the Update CLK button on the main program screen.
- 7) Verify that clock frequency is updated as shown in Figure 3–9.
- 8) Pressing the Update CLK button twice clears the frequency offset.

Figure 3–8. Input of Frequency Error

Frequency Error is entered here	7	Press Update CLK button
✓ TRF4900 V2.3         File       Edit       Go       Help         Synthesizer         CLK       25.6       ✓       MHz       Desired Freq. 915,000         Actual Freq. 915,000       Actual Freq. 915,000       Freq. Error       0.4000         PreScaler       256       Freq. Error       -0.4000         Mode Options       PLL       On       VCO       On         Pwr Amp       0 dB       LPT_x       1       MM	Main Program MHz MHz MHz MHz Update CLK and MM Options LL 140 × LL 256 1 FSK	Help Desired Chip Operating Frequency Press Enter to Send All Four Words.
Output Parameters         Enable       On       TXData       Off         Clock Width       345       Strobe Width         Operation Mode:       Mode 0       TXData:	Mode 0 675 Off Chip On	Words Send Words Now (F12) A 001000111011111000000000 Mode 0 B 011000111011111000000000 Mode 1 C 10111100000111100000000 Mode 1 D 11001000000111100000000 Mode 0

Figure 3–9. Main Panel Display After Clock Offset Is Applied

🛹 TRF4900 V2.3		Main Progr	am		-	. 🗆 X
<u>File E</u> dit <u>G</u> o <u>H</u> elp						
Synthesizer CLK 25.588809 - MH; PreScaler 256	Desired Freq. 915 Actual Freq. 914 Freq. Error 0	5.000 <mark>.</mark> MHz 1.999817 MHz MHz Qpaa	e CLM	Help Desired Chip Op Press Enter to S	erating Frequency iend All Four Word	, s.
Mode Options		PLL and MM Optic	ns			
PLL On	VCO On	APLL 140	-			
Pwr Amp 0 dB 💌	LPT_X 1	MM FSK				
Output Parameters				Words	Send Words Nov	w (F12)
Enable On	TXData Off	Mode 0		A 0010001111	00001000000000	Mode 0
Clock Width 345	Clock Width 345 Strobe Width 675			B 0110001110	11111000000000	Mode 1
			_	< 1011110000	01111000000000	Mode 1
Operation Mode:	Mode 0 TXData:Off Chip On		D 1100100000	01111000000000	Mode 0	

#### Step 4: FSK Modulation Output Test

On the chip layout screen press the *PLL/Modulation Options* button.

#### The PLL/Modulation Options View Is Set Up as Shown in Figure 3–11.

Figure 3–10. Chip Layout View for FSK Modulation Output Test



- □ Set the DVx bits, as shown in Figure 3–11, by double clicking inside each DVx box to set the value to either a 1 or 0. For this example only DV6 is set to a 1.
- □ Press the *Send Bits* button located on the PLL/Modulation Options screen, to obtain the results shown in Figure 3–11.
- Press the Close button located on the PLL/Modulation Options screen.

Figure 3–11. PLL/Modulation Options Screen



- □ Press the Send Words button on the chip layout screen or the Send Words Now (F12) on the main program screen.
- Press the FSK Test button on the chip layout screen, as shown in Figure 3–10, to start the FSK test.
- □ Set up the spectrum analyzer to observe the spectrum analyzer display as shown in Figure 3–12.



#### Figure 3–12. FSK Output From Transmitter

**Note:** This is FSK modulation with  $f_1$  equal to 915.0 MHz,  $f_2$  equal to 915.10-MHz and 100-Hz data rate. The  $f_1$  frequency is the 0 frequency. The  $f_2$  frequency is the 1 frequency.

Figure 3–13. Block Diagram for Testing of the TRF4900 EVM Transmitter Section With an External Pulse Generator



To use an external pulse generator to supply transmit data, set up the test bench as shown in Figure 3–13.

Perform the FSK modulation output test as described in the previous section. In this new setup, an external pulse generator is providing the modulation. The FSK Test button on the chip layout screen does not need to be pressed to start the FSK test.



Figure 3–14. FSK Output From Transmitter With an External Modulation

**Note:** This is FSK modulation with  $f_1$  equal to 915.0 MHz,  $f_2$  equal to 915.10-MHz and 1000-Hz data rate. The  $f_1$  frequency is the 0 frequency. The  $f_2$  frequency is the 1 frequency.