

N-Channel Power MOSFET

60V, 300mA, 2Ω

FEATURES

- Low $R_{DS(ON)}$ to minimize conductive losses
- Logic level
- Low gate charge for fast power switching
- ESD Protected 2.5KV (HBM)
- RoHS Compliant
- Halogen-free according to IEC 61249-2-21

KEY PERFORMANCE PARAMETERS

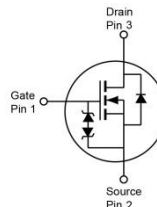
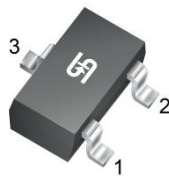
PARAMETER	VALUE	UNIT
V_{DS}	60	V
$R_{DS(on)}$ (max)	$V_{GS} = 10V$	2
	$V_{GS} = 4.5V$	4
Q_g	0.91	nC

APPLICATIONS

- Low Side Load Switching
- Level Shift Circuits
- General Switch Circuits



SOT-23



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current (Note 1)	I_D	$T_A = 25^\circ\text{C}$	300
		$T_A = 125^\circ\text{C}$	134
Pulsed Drain Current	I_{DM}	1.2	A
Total Power Dissipation	P_D	$T_A = 25^\circ\text{C}$	357
		$T_A = 125^\circ\text{C}$	71
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE

PARAMETER	SYMBOL	MAXIMUM	UNIT
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	350	$^\circ\text{C/W}$

Thermal Performance Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. The $R_{\theta JA}$ limit presented here is based on mounting on a 1 in² pad of 2 oz copper.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	BV_{DSS}	60	--	--	V
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	$V_{GS(TH)}$	1	1.4	2.5	V
Gate-Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	I_{GSS}	--	--	± 10	μA
Drain-Source Leakage Current	$V_{GS} = 0\text{V}, V_{DS} = 60\text{V}$	I_{DSS}	--	--	1	μA
	$V_{GS} = 0\text{V}, V_{DS} = 60\text{V}$ $T_J = 125^\circ\text{C}$		--	--	100	
Drain-Source On-State Resistance (Note 3)	$V_{GS} = 10\text{V}, I_D = 300\text{mA}$	$R_{DS(on)}$	--	1.5	2	Ω
	$V_{GS} = 4.5\text{V}, I_D = 210\text{mA}$		--	1.6	4	
Forward Transconductance (Note 3)	$V_{DS} = 5\text{V}, I_D = 300\text{mA}$	g_{fs}	--	0.5	--	S
Dynamic (Note 3)						
Total Gate Charge	$V_{GS} = 4.5\text{V}, V_{DS} = 30\text{V},$ $I_D = 300\text{mA}$	Q_g	--	0.91	--	nC
Gate-Source Charge		Q_{gs}	--	0.33	--	
Gate-Drain Charge		Q_{gd}	--	0.32	--	
Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 30\text{V}$ $f = 1.0\text{MHz}$	C_{iss}	--	30	--	pF
Output Capacitance		C_{oss}	--	15	--	
Reverse Transfer Capacitance		C_{rss}	--	6	--	
Switching (Note 3)						
Turn-On Delay Time	$V_{GS} = 10\text{V}, V_{DS} = 30\text{V},$ $I_D = 300\text{mA}, R_G = 6\Omega$	$t_{d(on)}$	--	4	--	ns
Turn-On Rise Time		t_r	--	10	--	
Turn-Off Delay Time		$t_{d(off)}$	--	20	--	
Turn-Off Fall Time		t_f	--	50	--	
Source-Drain Diode						
Forward Voltage (Note 2)	$V_{GS} = 0\text{V}, I_S = 300\text{mA}$	V_{SD}	--	--	1.4	V
Reverse Recovery Time	$I_S = 300\text{mA},$ $di/dt = 100\text{A}/\mu\text{s}$	t_{rr}	--	12	--	ns
Reverse Recovery Charge		Q_{rr}	--	3	--	nC

Notes:

1. Silicon limited current only.
2. Pulse test: Pulse Width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
3. Switching time is essentially independent of operating temperature.

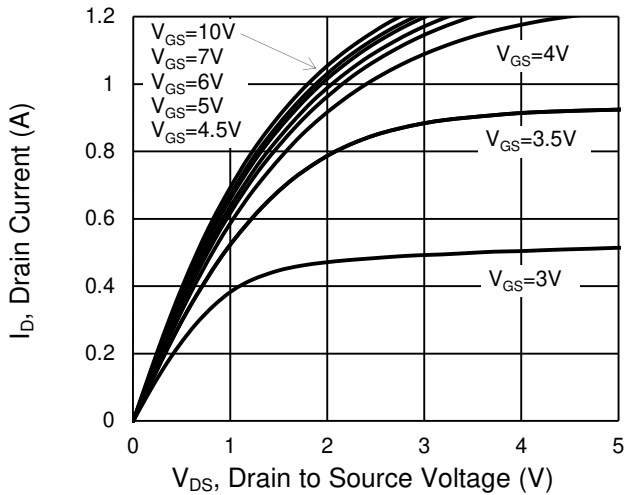
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM2N7002KCX RFG	SOT-23	3,000pcs / 7" Reel

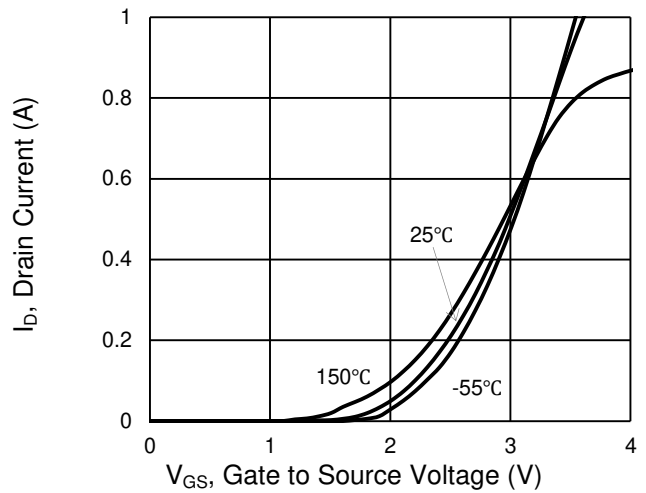
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

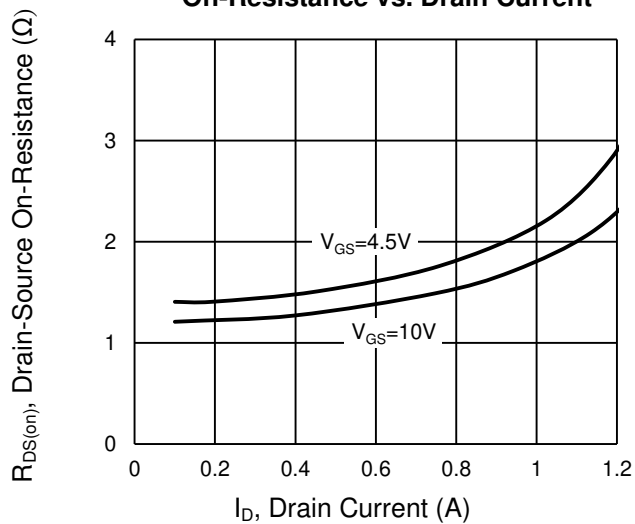
Output Characteristics



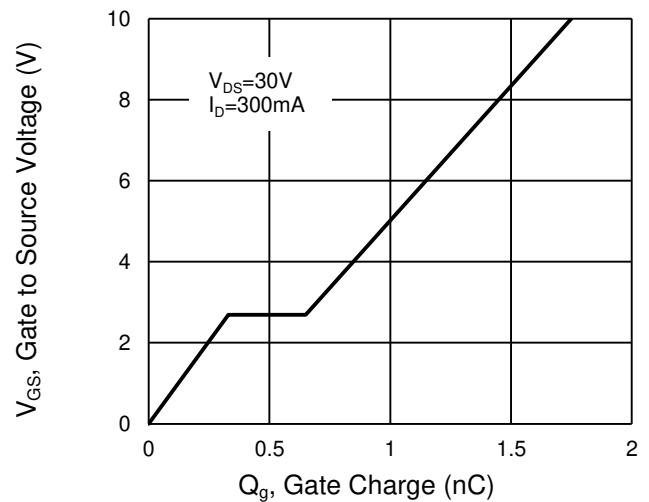
Transfer Characteristics



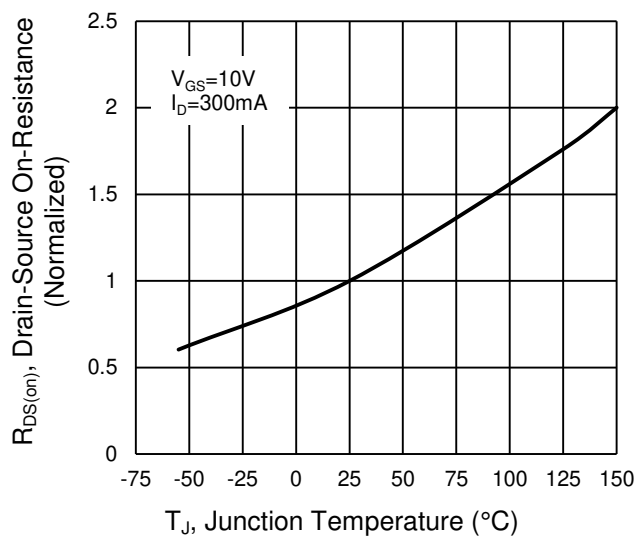
On-Resistance vs. Drain Current



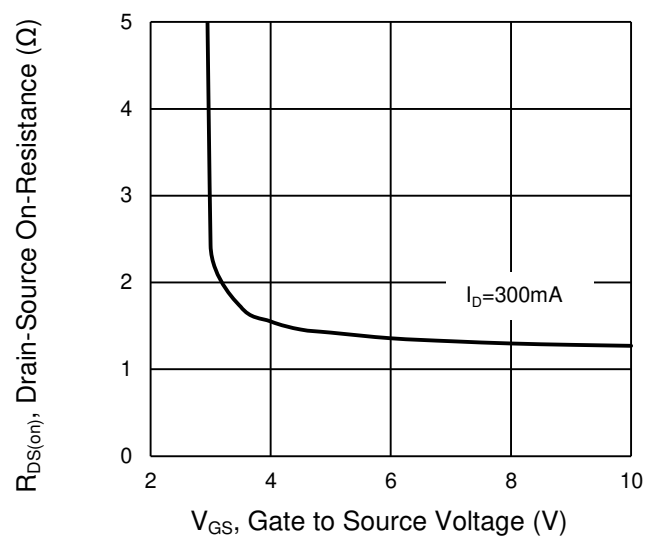
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



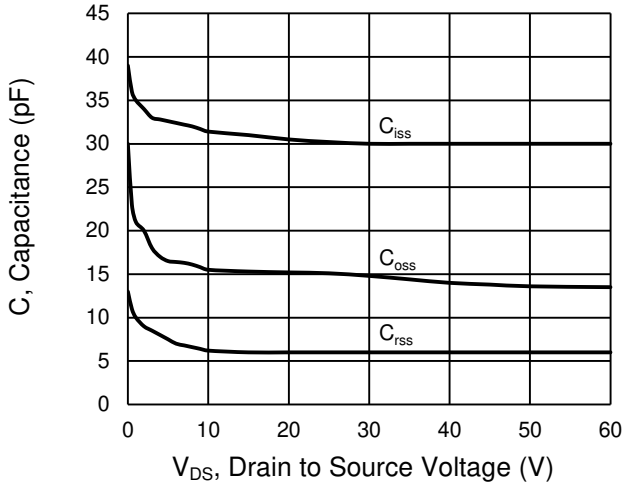
On-Resistance vs. Gate-Source Voltage



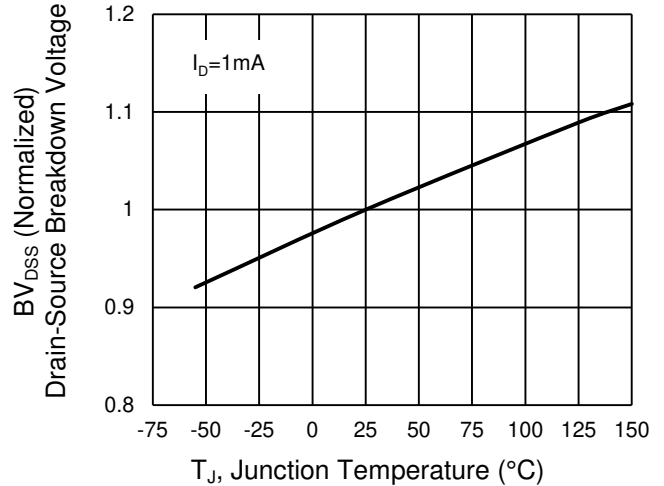
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

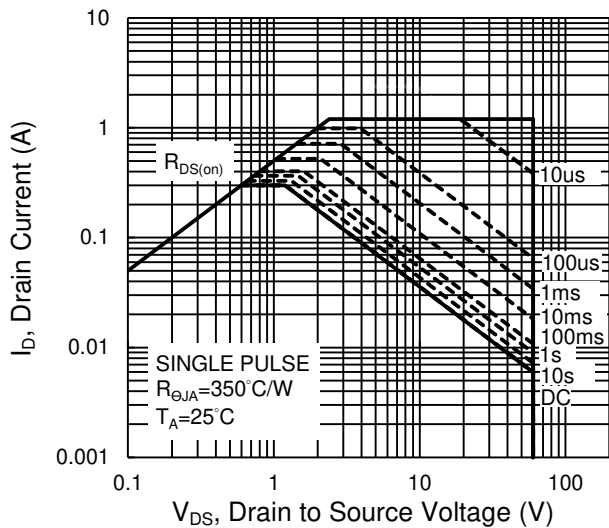
Capacitance vs. Drain-Source Voltage



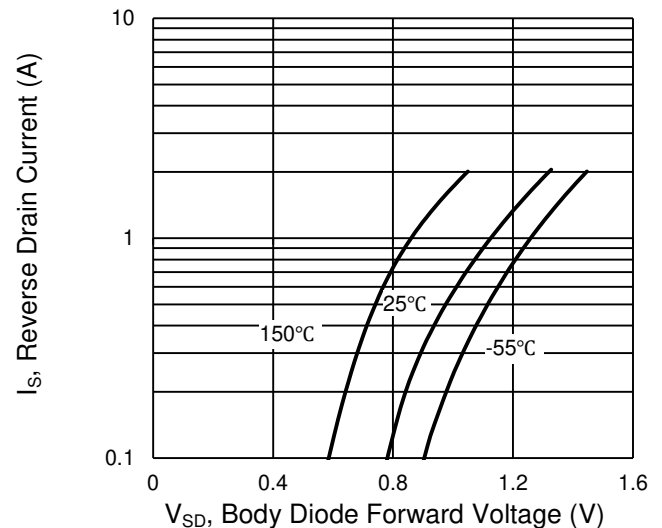
BV_{DSS} vs. Junction Temperature



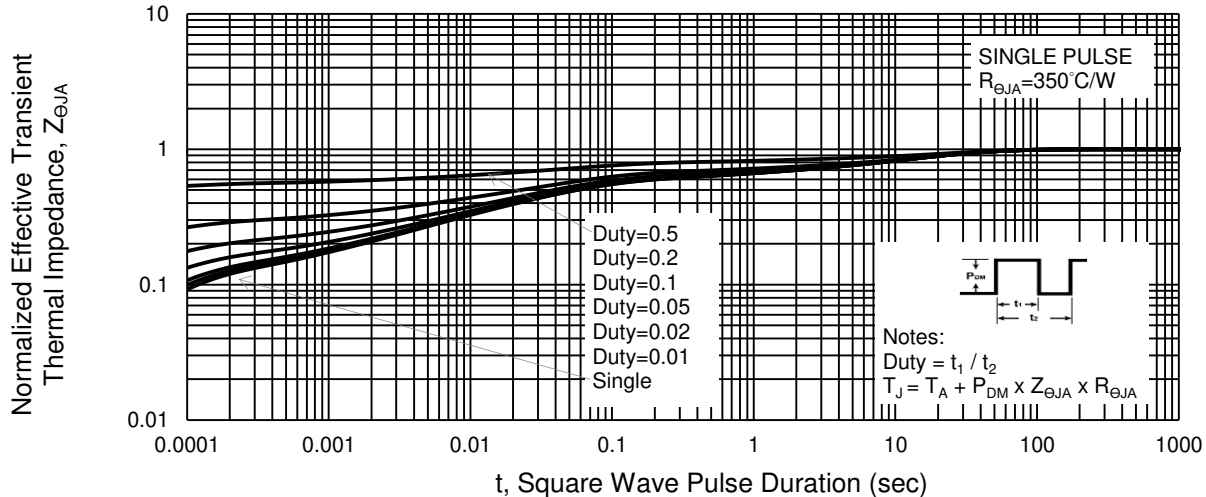
Maximum Safe Operating Area, Junction-to-Ambient



Source-Drain Diode Forward Current vs. Voltage

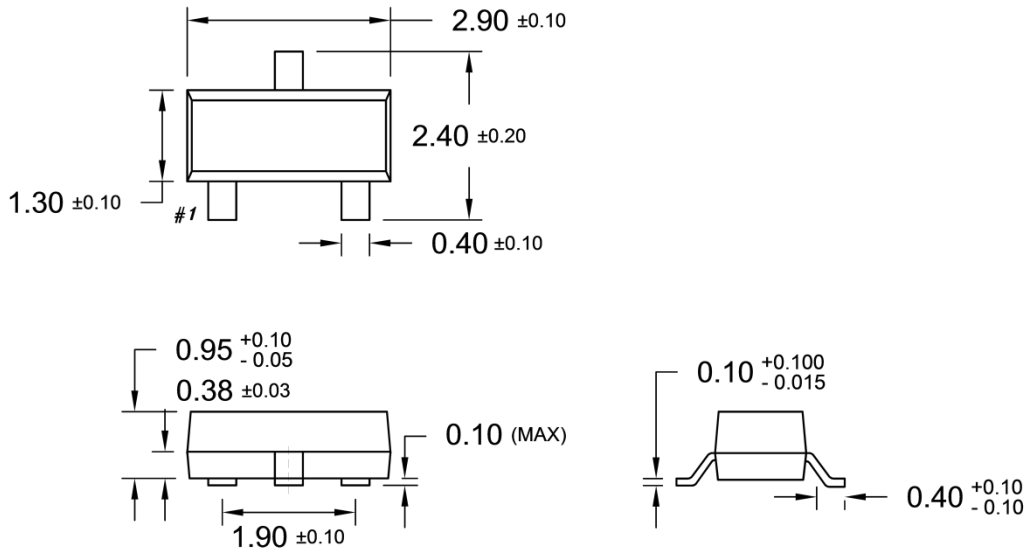


Normalized Thermal Transient Impedance, Junction-to-Ambient

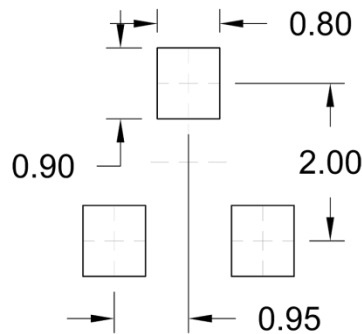


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

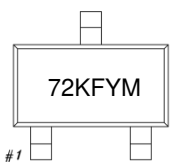
SOT-23



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- 72K** = Device code
 - F** = Site Code
 - Y** = Year Code
 - M** = Month code
- | | | | |
|---------------|---------------|---------------|---------------|
| O =Jan | P =Feb | Q =Mar | R =Apr |
| S =May | T =Jun | U =Jul | V =Aug |
| W =Sep | X =Oct | Y =Nov | Z =Dec |

Notice

Specifications of the products displayed herein are subject to change without notice. TSC or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Purchasers are solely responsible for the choice, selection, and use of TSC products and TSC assumes no liability for application assistance or the design of Purchasers' products.

Information contained herein is intended to provide a product description only. No license, express or implied, to any intellectual property rights is granted by this document. Except as provided in TSC's terms and conditions of sale for such products, TSC assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of TSC products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify TSC for any damages resulting from such improper use or sale.