Brief Description

The ZSPM4023-09 is a constant-frequency, synchronous DC/DC buck regulator featuring adaptive on-time control architecture. The ZSPM4023-09 operates over a 4.5V to 28V supply range (24V typical). It has an internal linear regulator that provides a regulated 5V to power the internal control circuitry. The ZSPM4023-09 operates at a constant 600kHz (typical) switching frequency in continuous-conduction mode and can be used to provide up to 9A of output current. The output voltage is adjustable from 5.5V down to 0.8V.

Under medium to heavy loads, the ZSPM4023-09 provides high efficiency and ultra-fast transient response via its rapid-control architecture. Under light load conditions, it maintains high efficiency and a superior transient response by transitioning to variable-frequency, discontinuous mode operation with its ultra-light-load architecture.

The ZSPM4023-09 offers a full suite of protection features to ensure protection of the IC during fault conditions. These include under-voltage lockout to ensure proper operation under power-sag conditions; thermal shutdown; internal soft-start to reduce inrush current; foldback current limiting; and "hiccup" mode short-circuit protection. The ZSPM4023-09 includes a power good (PG) output to allow simple sequencing.

Benefits

- Ultra-light load efficiency – up to 80% at 10mA
- Up to 95% efficiency
- Feedback reference accuracy as high as ±1%

Features

- Rapid-control architecture enables operation with a high input/output voltage ratio (e.g., V_{IN} = 28V and V_{OUT} = 0.8V) and small output capacitance
- Adjustable output voltage from 0.8V to 5.5V
- Universally compatible with most output capacitors—stable with zero to high ESR
- Power good (PG) output
- Foldback current limiting and "hiccup" mode short-circuit protection
- Safe start-up into pre-biased loads

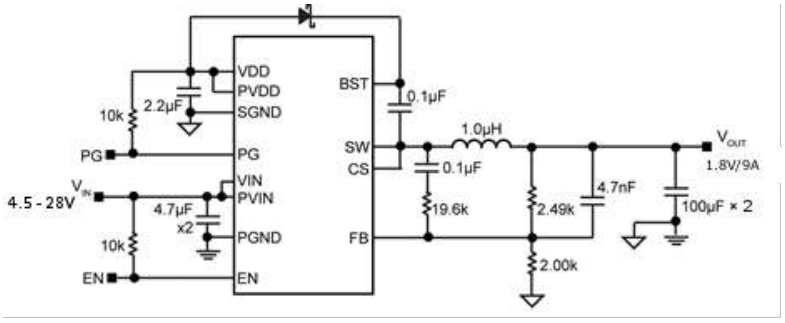
Available Support

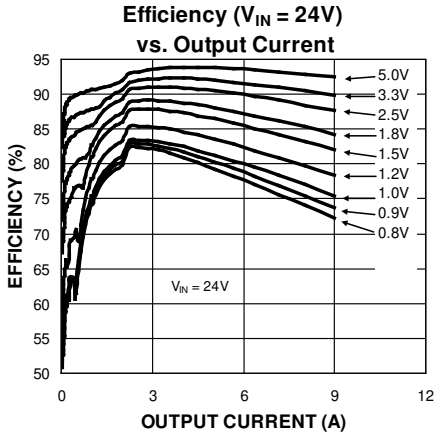
- Evaluation Kit
- Support documentation

Physical Characteristics

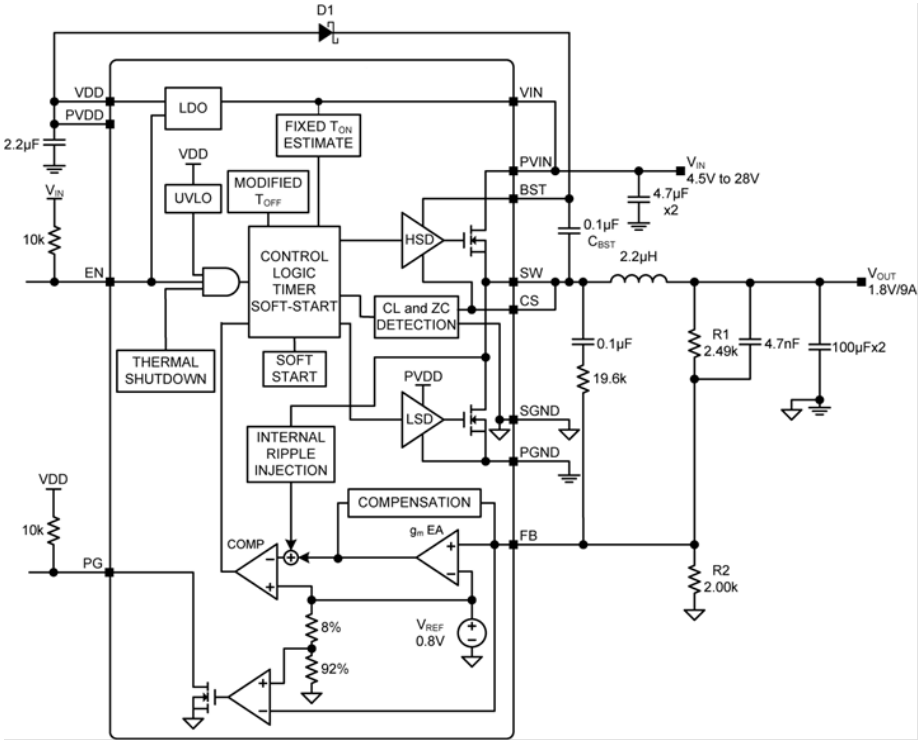
- Input voltage range: 4.5V to 28V
- Output current: up to 9A
- Switching frequency: 600kHz
- Junction temperature: –40°C to +125°C
- 28-pin 5mm × 6mm QFN package

ZSPM4023-09 Typical Application





ZSPM4023-09 Functional Diagram



Typical Applications

- *Servers, work stations*
- *Routers, switches, and telecom equipment*
- *Base stations*

Ordering Information

Product Sales Code	Description	Package
ZSPM4023AA1W09	ZSPM4023-09 QFN28 5mmx6mm — Temperature range: –40°C to +125°C	7” reel with 1000 ICs
ZSPM4023-09-KIT	Evaluation Kit for ZSPM4023-09, including ZSPM4023-09 Evaluation Board.	Kit

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1 IC Characteristics

The absolute maximum ratings are stress ratings only. The device might not function or be operable above the operating conditions given in section 1.2. Stresses exceeding the absolute maximum ratings might also damage the device. In addition, extended exposure to stresses above the recommended operating conditions might affect device reliability. IDT does not recommend designing to the “Absolute Maximum Ratings.”

1.1. Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Voltage PVIN pin to PGND pin	$V_{PVIN(max)}$		–0.3	+29	V
Voltage VIN pin to PGND pin	$V_{IN(max)}$		–0.3	V_{PVIN}	V
Voltage PVDD or VDD pin to PGND pin	$V_{PVDD(max)}$ $V_{VDD(max)}$		–0.3	+6V	V
Voltage SW or CS pin to PGND pin	$V_{SW(max)}$ $V_{CS(max)}$		–0.3	(V_{PVIN} +0.3V)	V
Voltage BST pin to SW pin			–0.3	6	V
Voltage BST pin to PGND pin	$V_{BST(max)}$		–0.3	35	V
Voltage EN pin to PGND pin	$V_{EN(max)}$		–0.3	(V_{IN} + 0.3V)	V
Voltage FB or PG pin to PGND pin	$V_{FB(max)}$ $V_{PG(max)}$		–0.3	(V_{DD} + 0.3V)	V
Voltage PGND pin to SGND pin			–0.3	+0.3	V
Junction Temperature	T_J			+150	°C
Storage Temperature	T_S		–65	+150	°C
Lead Temperature (soldering, 10s)				260	°C
ESD Rating [1]		Human body model, 1.5kΩ in series with 100pF	1000		V

1) Devices are ESD sensitive. Handling precautions are recommended.

1.2. Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (PVIN, VIN pins)	V_{PVIN}, V_{IN}		4.5		28	V
Bias Voltage (PVDD, VDD pins)	V_{PVDD}, V_{DD}		4.5		5.5	V
Enable Input	V_{EN}		0		V_{IN}	V
Junction Temperature [1]	T_J		–40		+125	°C
QFN28 Package Thermal Resistance [1]	θ_{JA}	Junction to ambient		28		°C/W
	θ_{JC}	Junction to case		2.5		°C/W

1) Maximum Power Dissipation $PD_{(MAX)} = (T_{J(MAX)} – T_A)/ \theta_{JA}$, where θ_{JA} depends upon the printed circuit layout and T_A is the ambient temperature. See section 3.2.

1.3. Electrical Parameters

Unless noted otherwise, test conditions for typical values are V_{PVIN} = V_{IN} = V_{EN} = 12V; V_{BST} – V_{SW} = 5V; T_A = 25°C.

Yellow shaded values indicate that –40°C ≤ T_J ≤ +125°C is a condition requirement.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Input						
Input Voltage Range	V_{IN}, V_{VPIN}		**4.5**		**28**	V
Quiescent Supply Current	I_{VDD}	V_{FB} = 1.5V (non-switching)		450	**750**	µA
Shutdown Supply Current	I_{VDD}	V_{EN} = 0V		5	**10**	µA
V_{DD} Supply Voltage						
VDD Output Voltage	V_{DD}	V_{IN} = 7V to 28V, I_{DD} = 25mA	**4.8**	5	**5.4**	V
VDD UVLO Threshold		V_{DD} rising	**3.7**	4.2	**4.5**	V
VDD UVLO Hysteresis				400		mV
Dropout Voltage (VIN – VDD)		I_{DD} = 25mA		380	**600**	mV
DC/DC Controller						
Output-Voltage Adjustment Range (V_{OUT})			0.8		**5.5**	V
Reference						
Feedback (FB) Reference Voltage		0°C ≤ T_J ≤ 85°C	**0.792**	0.8	**0.808**	V
		–40°C ≤ T_J ≤ 125°C	**0.788**	0.8	**0.812**	
Load Regulation		I_{OUT} = 3A to 9A (Continuous Mode)		0.25		%
Line Regulation		V_{IN} = 4.5 to 28V		0.25		%
FB Bias Current		V_{FB} = 0.8V		50	**500**	nA
Enable Control						
EN Logic Level High			**1.8**			V
EN Logic Level Low					**0.6**	V
EN Bias Current		V_{EN} = 12V		6	**30**	µA
Oscillator						
Switching Frequency	f_{SW}		**450**	600	**750**	kHz
Maximum Duty Cycle [1)]	D_{MAX}	V_{FB} = 0V		82		%
Minimum Duty Cycle	D_{MIN}	V_{FB} = 1.0V		0		%
Minimum Off-time				300		ns
Soft-Start						
Soft-Start time				5		ms
Short-Circuit Protection						
Current–Limit Threshold		V_{FB} = 0.8V, T_J = 25°C	12.5	15	20	A

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		V_{FB} = 0.8V, T_J = 125°C	11.25	15	20	A
Short–Circuit Current Limit		V_{FB} = 0V		4		A
Internal FETs						
Top MOSFET	$R_{DS\ (ON)}$	I_{SW} = 3A		27		mΩ
Bottom MOSFET	$R_{DS\ (ON)}$	I_{SW} = 3A		10.5		mΩ
SW Leakage Current		V_{EN} = 0V			**60**	µA
VIN Leakage Current		V_{EN} = 0V			**25**	µA
Power Good						
PG Threshold Voltage		Sweep V_{FB} from Low to High	**85**	92	**95**	$\%V_{OUT}$
PG Hysteresis		Sweep V_{FB} from High to Low		5.5		$\%V_{OUT}$
PG Delay Time		Sweep V_{FB} from Low to High		100		µs
PG Low Voltage		Sweep $V_{FB} < 0.9 \times V_{NOM}$, I_{PG} = 1mA		70	**200**	mV
Thermal Protection						
Over-Temperature Shutdown		T_J rising		160		°C
Over-Temperature Shutdown Hysteresis				15		°C

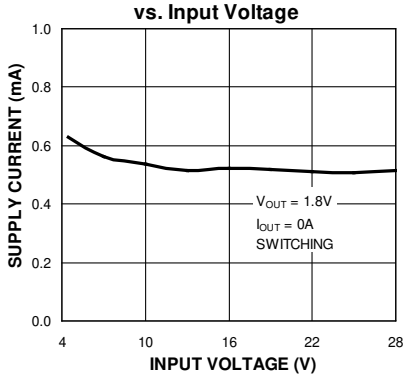
Notes:

1) The maximum duty–cycle is limited by the fixed mandatory off-time (t_{OFF}) of 300ns (typical).

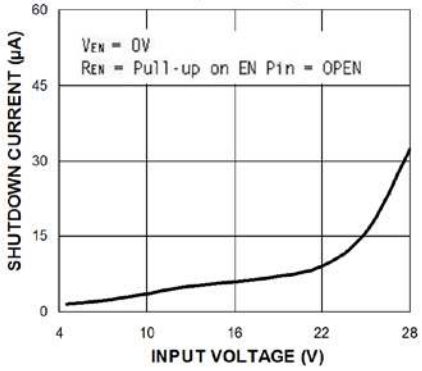
1.4. Typical Characteristics

Note: For graphs marked with an asterisk **(*)**, the die temperature measurement was taken at the hottest point on the ZSPM4023-09 case mounted on a 5 in^2 × 0.62 in, four-layer FR-4 PCB with 2oz finish copper weight per layer; see section 3.2. Actual results will depend upon the size of the PCB, ambient temperature, and proximity to other heat emitting components.

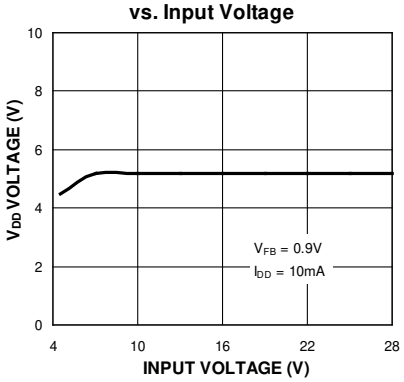
V_{IN} Operating Supply Current vs. Input Voltage



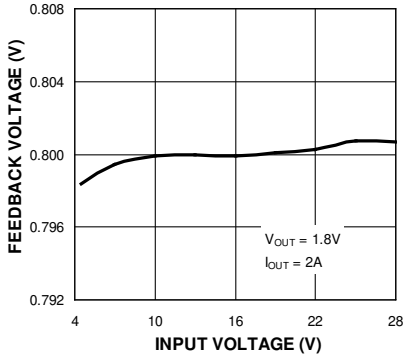
V_{IN} Shutdown Current vs. Input Voltage



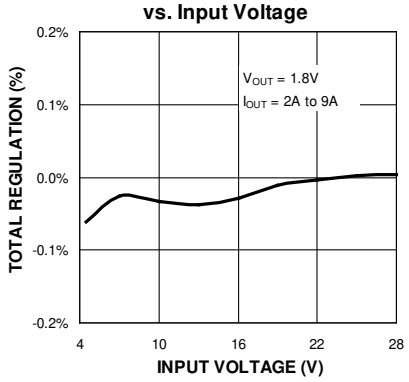
V_{DD} Output Voltage vs. Input Voltage



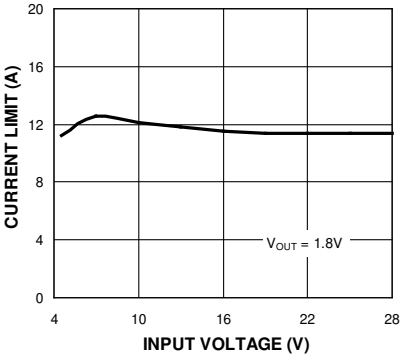
Feedback Voltage vs. Input Voltage



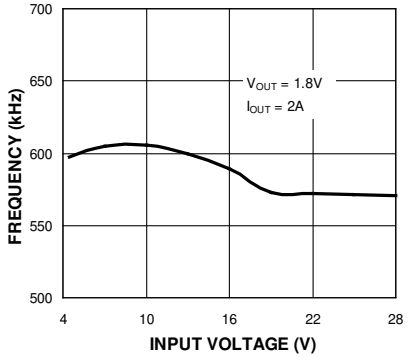
Total Regulation vs. Input Voltage



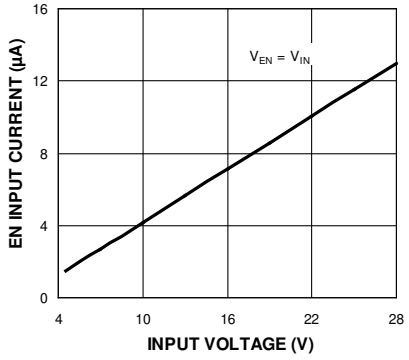
Current Limit vs. Input Voltage



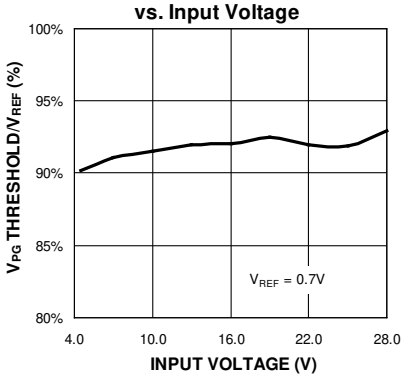
Switching Frequency vs. Input Voltage



Enable Input Current vs. Input Voltage

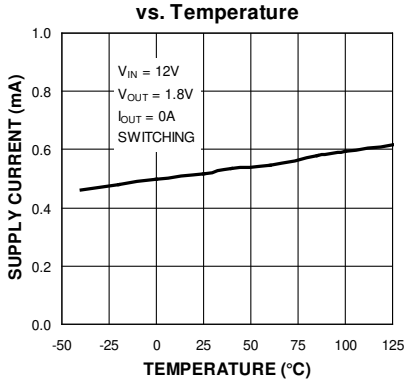


PG/V_{REF} Ratio vs. Input Voltage

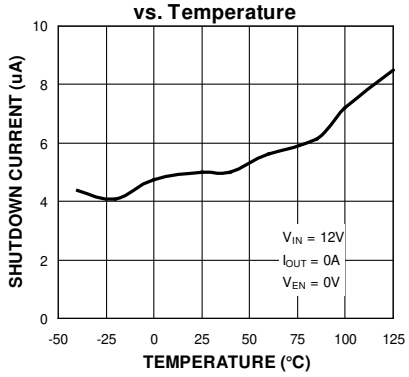


Typical Characteristics (Continued)

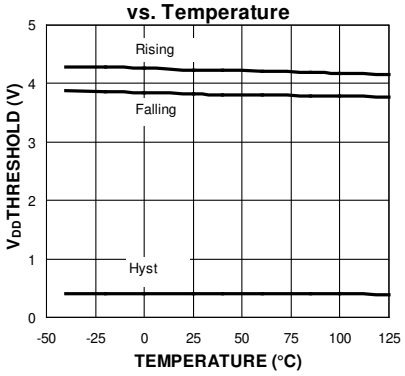
V_{IN} Operating Supply Current vs. Temperature



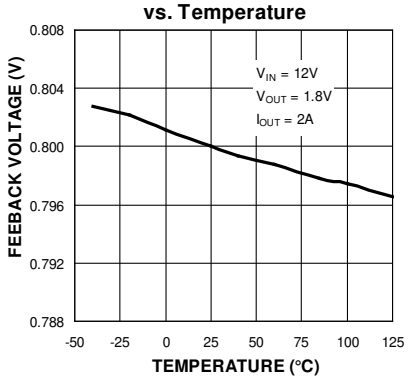
V_{IN} Shutdown Current vs. Temperature



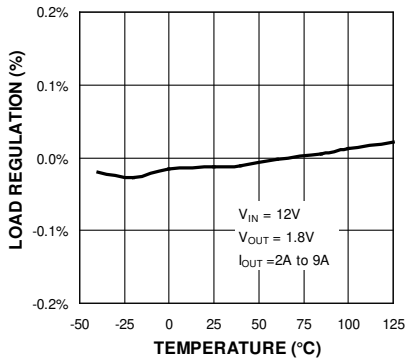
V_{DD} UVLO Threshold vs. Temperature



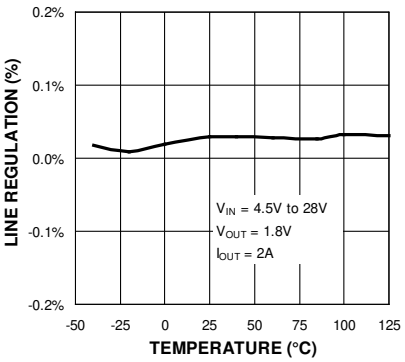
Feedback Voltage vs. Temperature



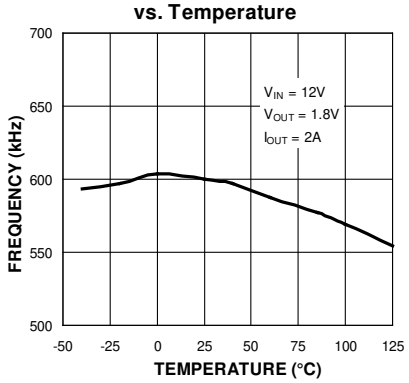
Load Regulation vs. Temperature



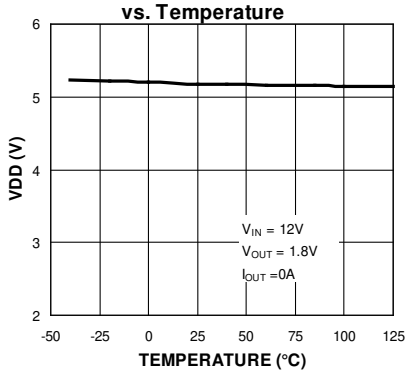
Line Regulation vs. Temperature



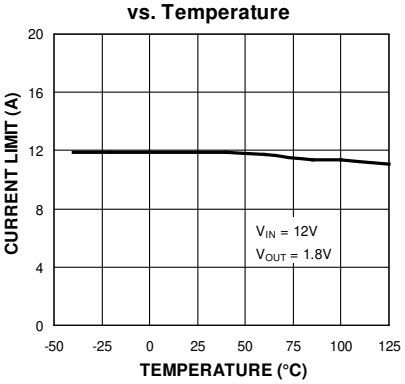
Switching Frequency vs. Temperature



V_{DD} vs. Temperature

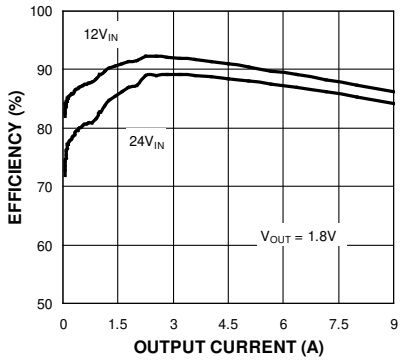


Current Limit vs. Temperature

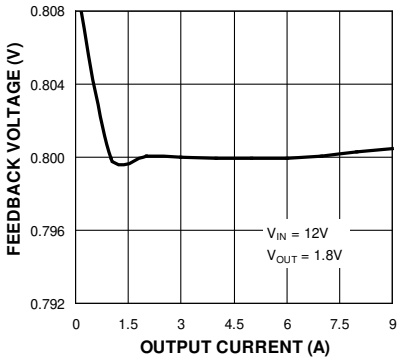


Typical Characteristics (Continued)

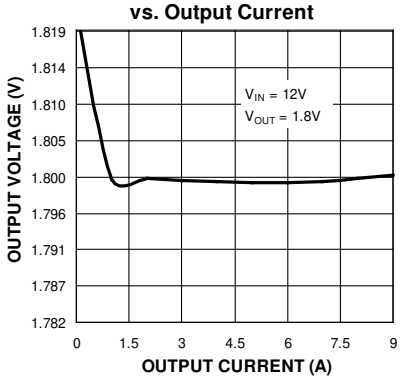
Efficiency vs. Output Current



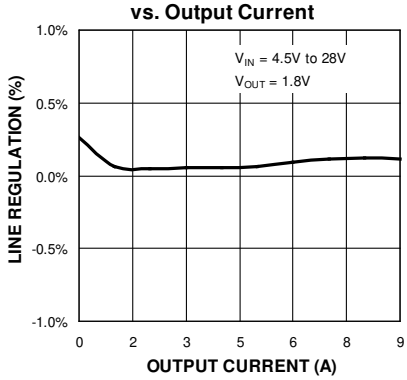
Feedback Voltage vs. Output Current



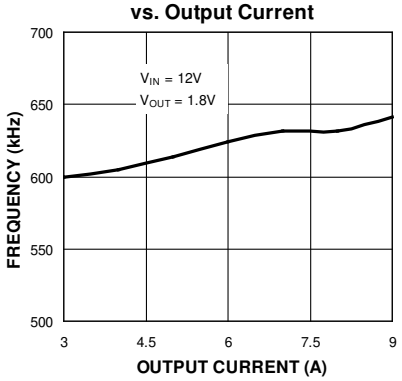
Output Voltage vs. Output Current



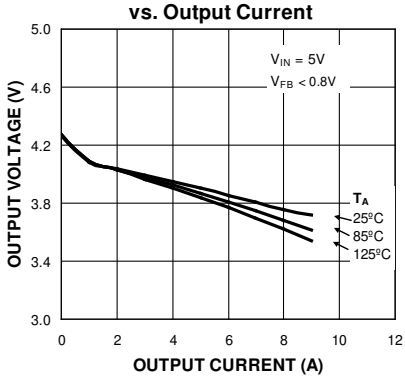
Line Regulation vs. Output Current



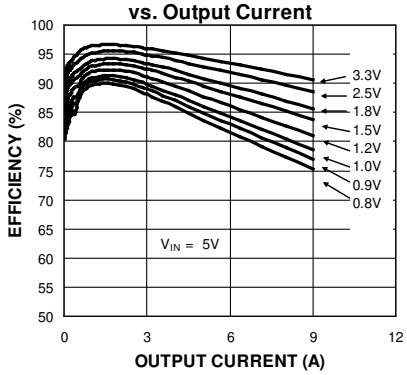
Switching Frequency vs. Output Current



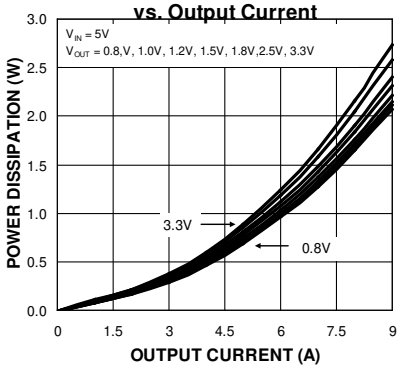
Output Voltage (V_{IN} = 5V) vs. Output Current



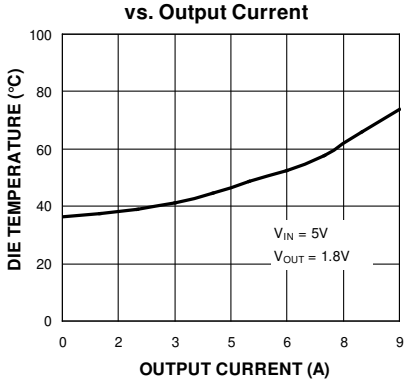
Efficiency (V_{IN} = 5V) vs. Output Current



IC Power Dissipation (VIN = 5V) vs. Output Current

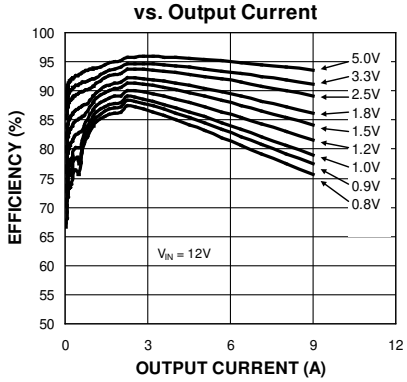


Die Temperature* (V_{IN} = 5V) vs. Output Current

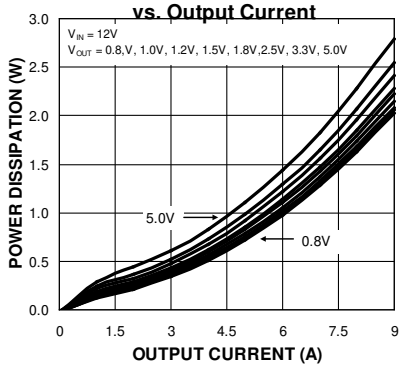


Typical Characteristics (Continued)

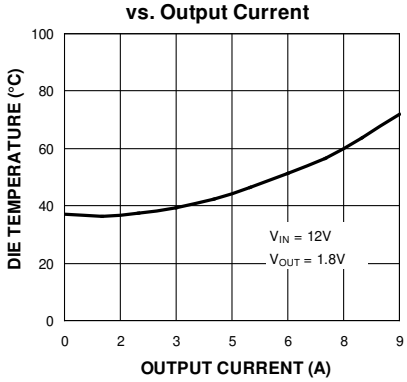
Efficiency (V_{IN} = 12V) vs. Output Current



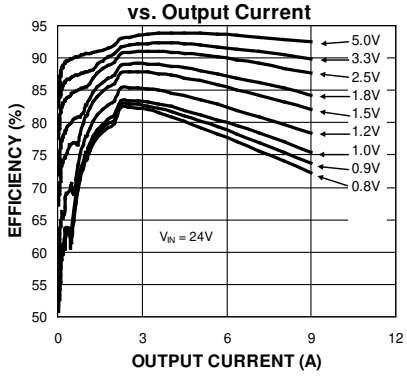
IC Power Dissipation (VIN = 12V) vs. Output Current



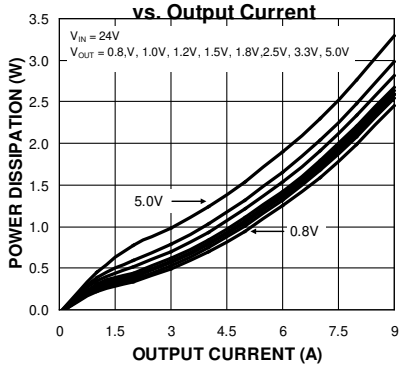
Die Temperature* (V_{IN} = 12V) vs. Output Current



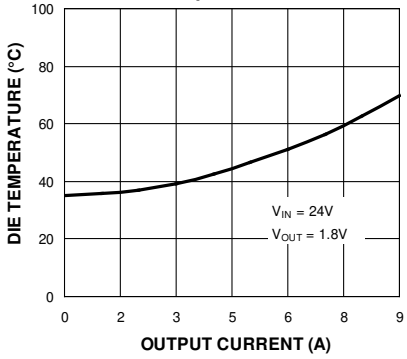
Efficiency (V_{IN} = 24V) vs. Output Current



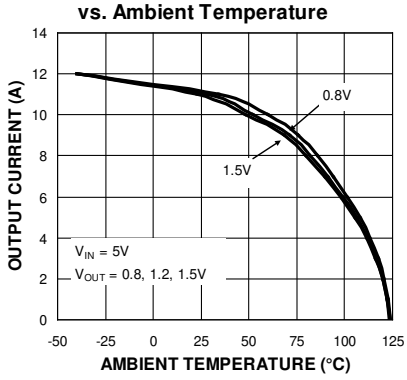
IC Power Dissipation (VIN = 24V) vs. Output Current



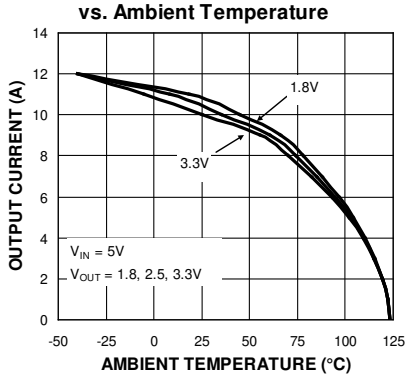
Die Temperature* (V_{IN} = 24V) vs. Output Current



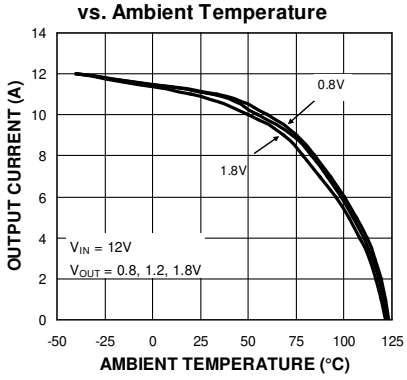
Thermal Derating* vs. Ambient Temperature



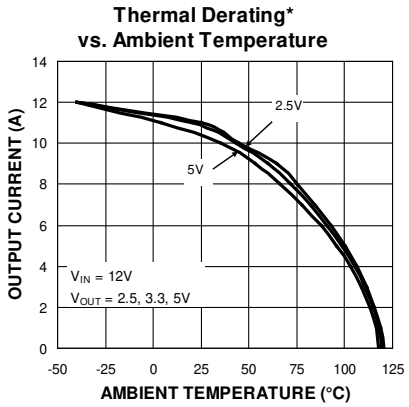
Thermal Derating* vs. Ambient Temperature

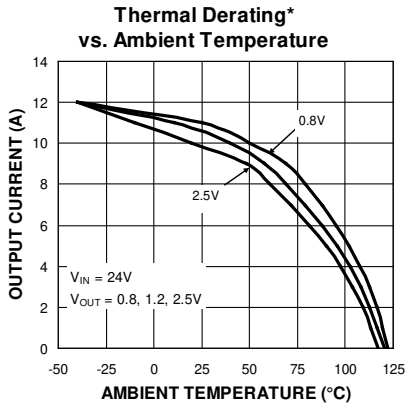


Thermal Derating* vs. Ambient Temperature



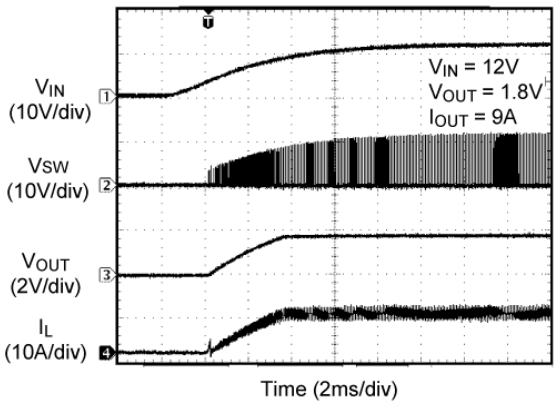
Typical Characteristics (Continued)



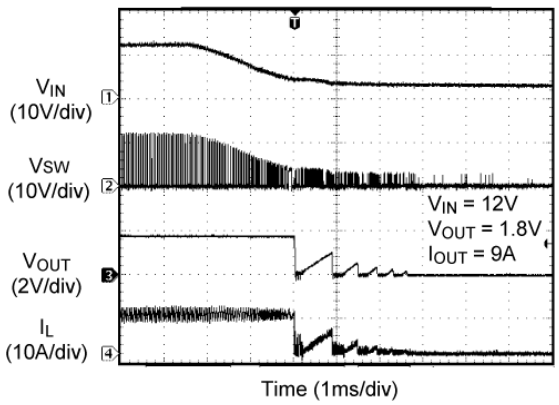


1.5. Functional Characteristics

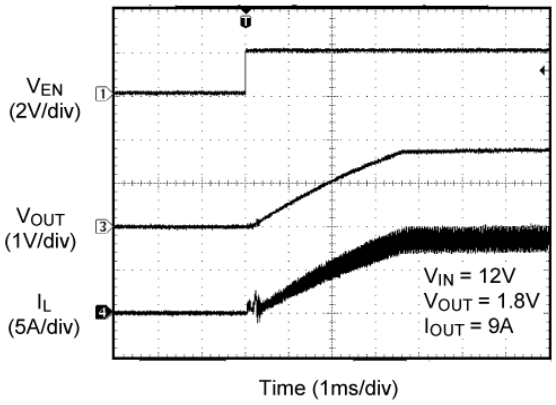
V_{IN} Soft Turn-On



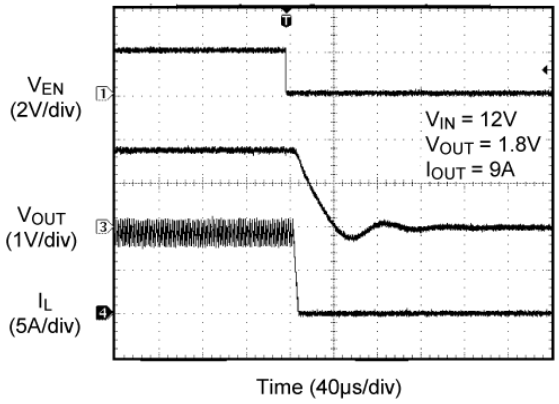
V_{IN} Soft Turn-Off



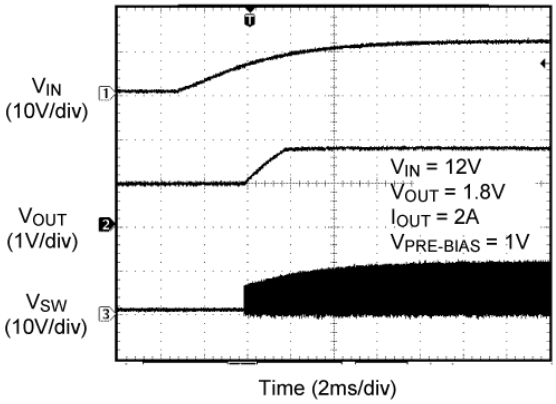
Enable Turn-On Delay and Rise Time



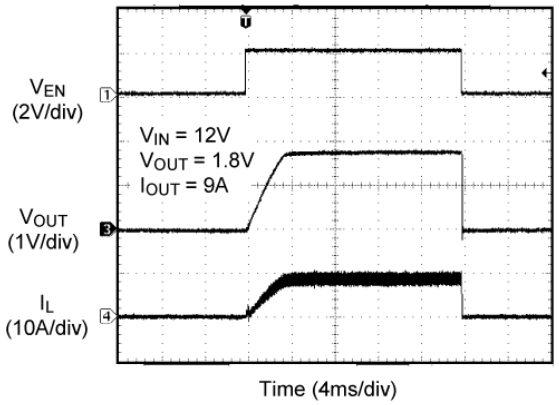
Enable Turn-Off Delay and Fall Time



V_{IN} Start-up with Pre-biased Output

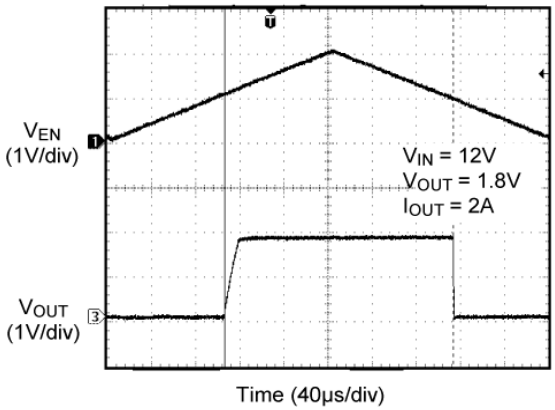


Enable Turn-On/turn-Off

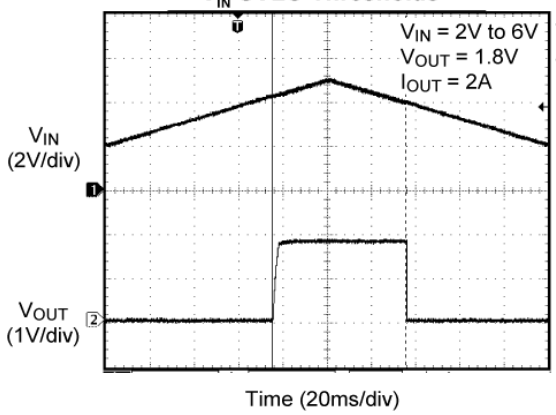


Functional Characteristics (Continued)

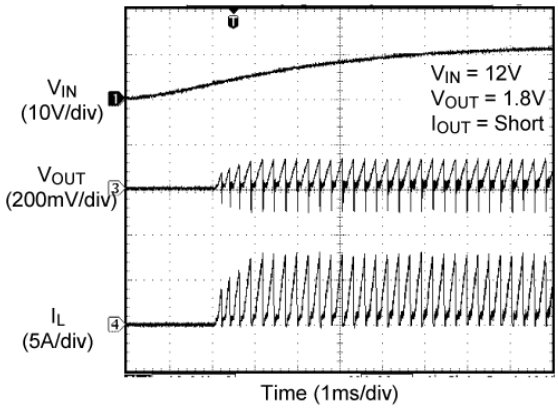
Enable Thresholds



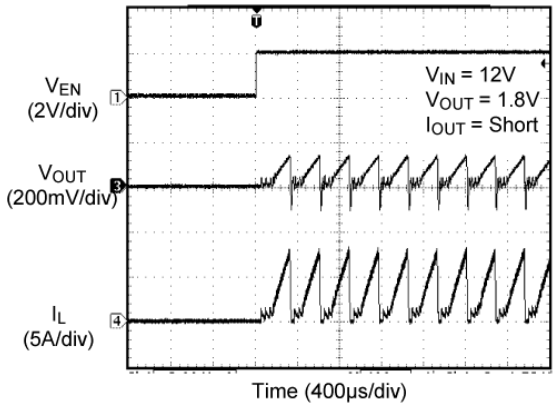
V_{IN} UVLO Thresholds



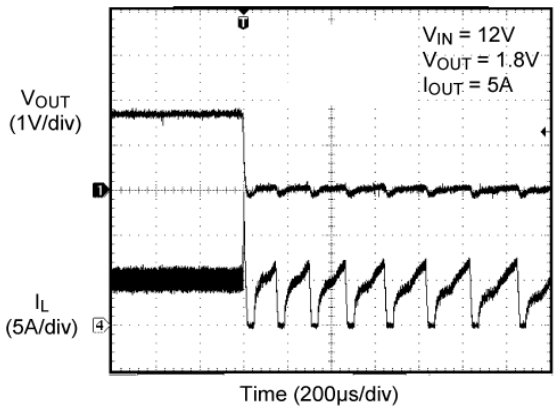
Power Up into Short Circuit



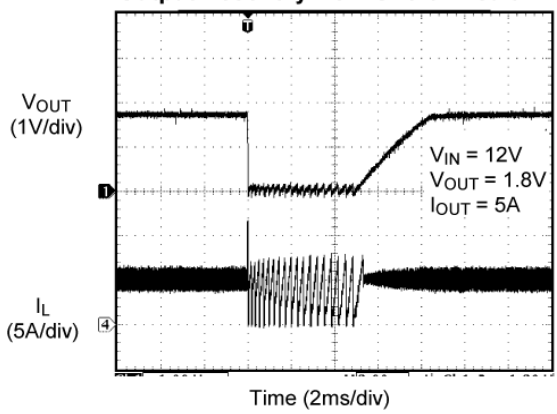
Enabled into Short



Short Circuit

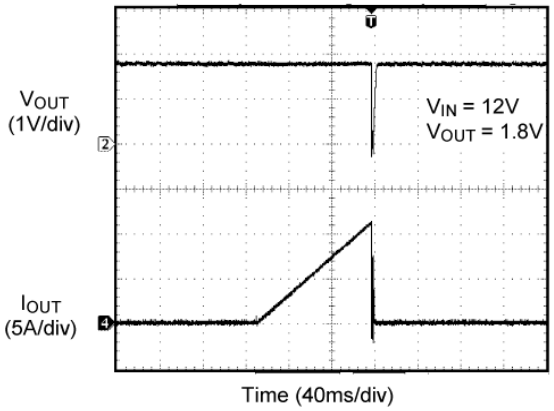


Output Recovery from Short Circuit

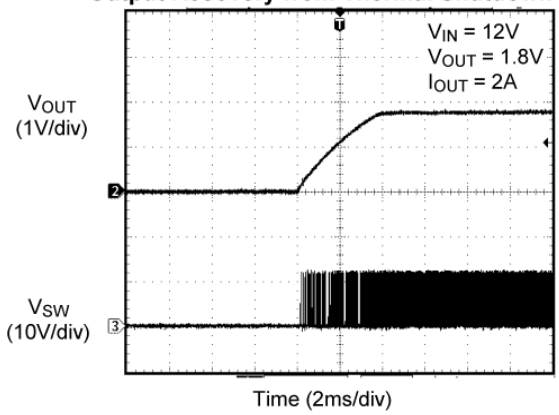


Functional Characteristics (Continued)

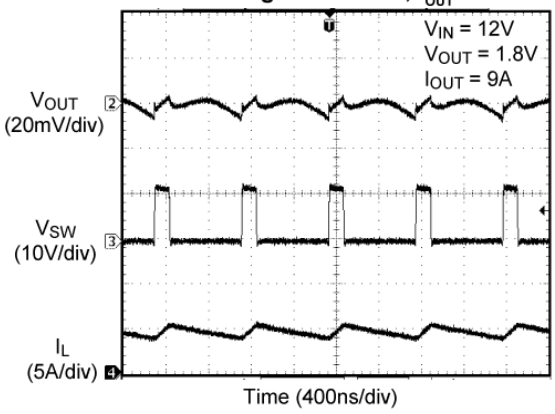
Peak current Limit Threshold



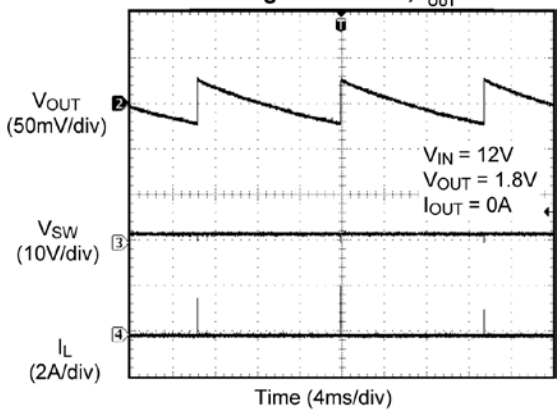
Output Recovery from Thermal Shutdown



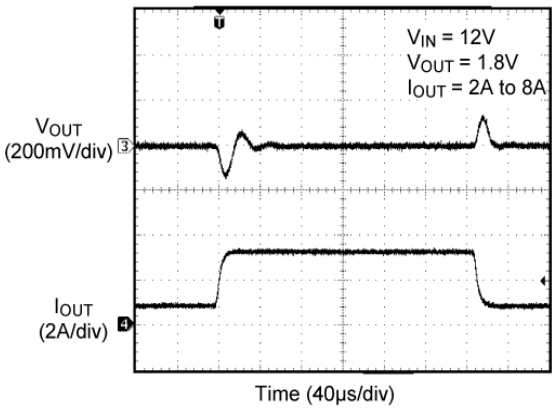
Switching Waveforms; I_{OUT} = 9A



Switching Waveforms; I_{OUT} = 0A



Transient Response



2 Functional Description

2.1. Overview

The ZSPM4023-09 is an adaptive on-time synchronous step-down DC/DC regulator with an internal 5V linear regulator and a power good (PG) output. It is designed to operate over a wide input voltage range from 4.5V to 28V and provides a regulated output voltage at up to 9A of output current. The output voltage is determined by a resistor divider network as explained in section 3.1.5. An adaptive on-time control scheme is employed to obtain a constant switching frequency and to simplify the control compensation. Over-current protection is implemented without the use of an external sense resistor. The ZSPM4023-09 includes an internal soft-start function that reduces the power supply input surge current at start-up by controlling the output voltage rise time.

Figure 2.1 Functional Diagram

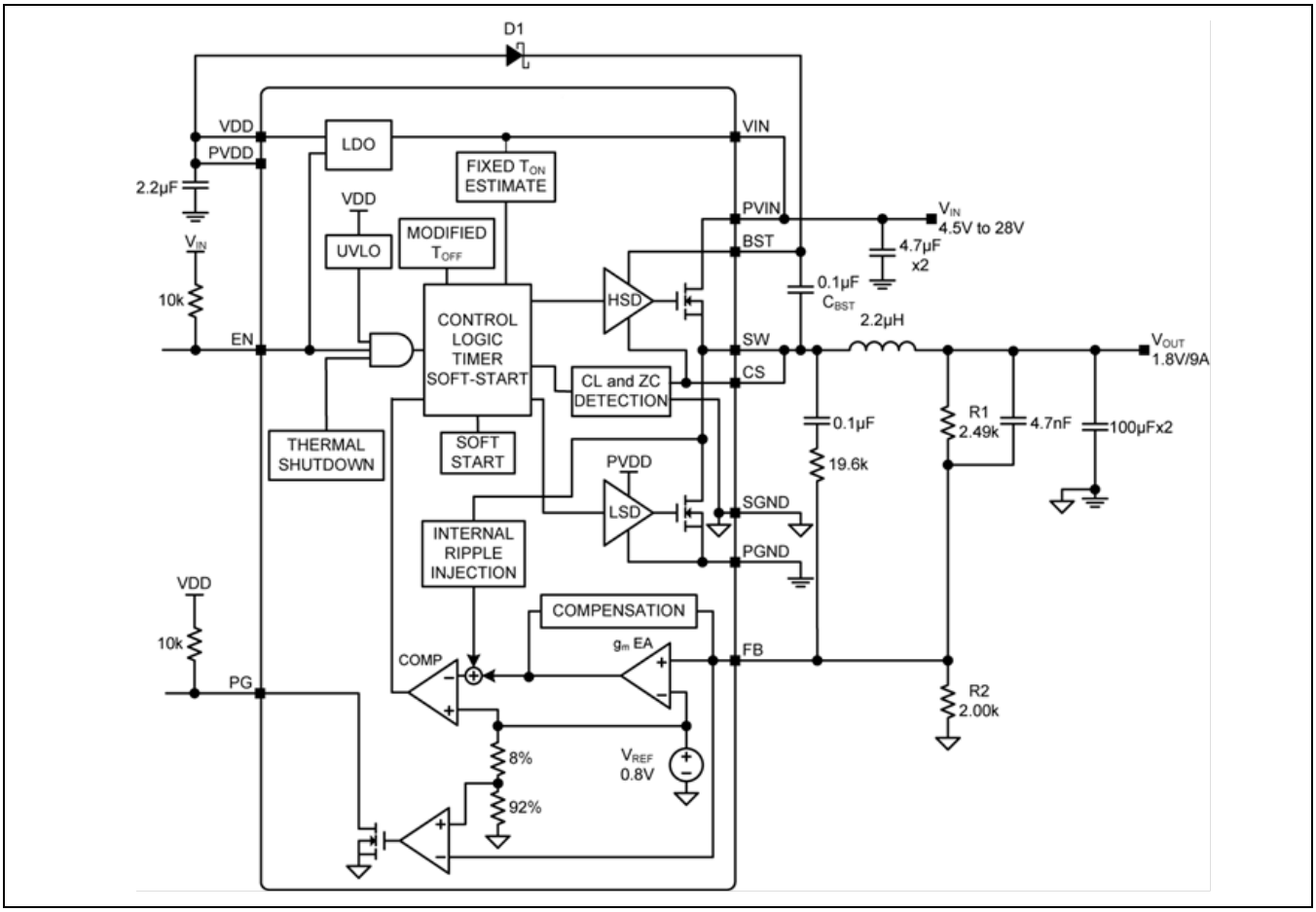
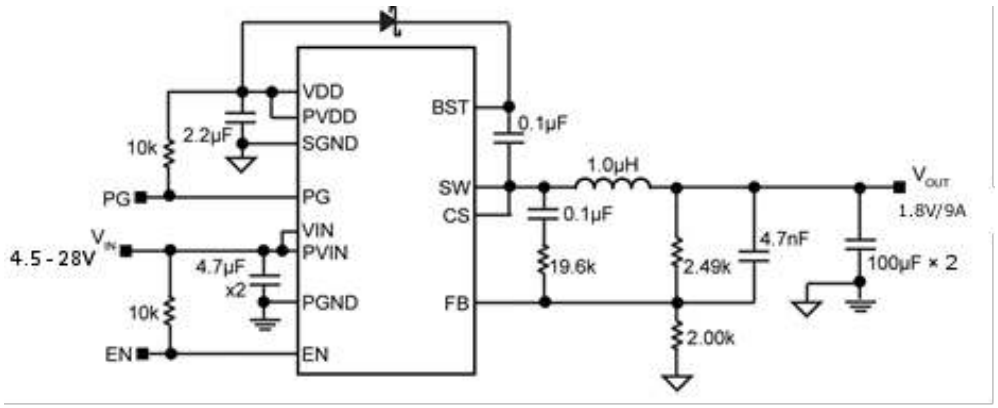


Figure 2.2 Typical Application Circuit



2.2. Pin Configuration and Description

The ZSPM4023-09 is available in a 28-pin 5mm × 6mm QFN package. The pin-out is shown in Figure 2.3. The mechanical drawing of the package is in Figure 4.1.

Figure 2.3 Pin Configuration 28-Pin 5mm × 6mm QFN (JL)—Top View

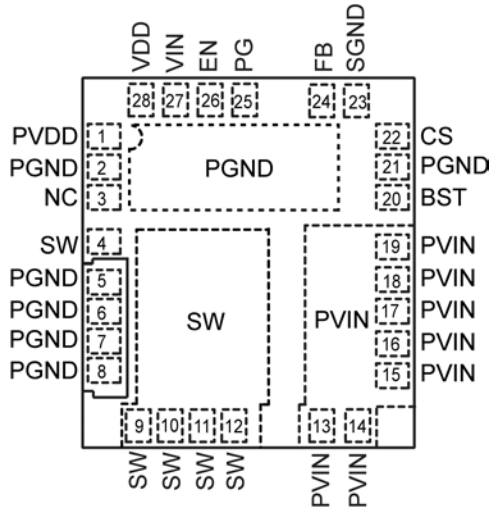


Table 2.1 Pin Descriptions

Pin	Name	Description
1	PVDD	5V internal linear regulator output. The PVDD supply is the power MOSFET gate drive supply voltage, and it is created from V_{IN} by the internal LDO. When V_{IN} < +5.5V, PVDD should be tied to the PVIN pins. A 2.2µF ceramic capacitor from the PVDD pin to the PGND (pin 2) must be placed next to the ZSPM4023-09.
2	PGND	Power ground. PGND is the ground path for the ZSPM4023-09 buck converter power stage. The PGND pins connect to the ground for the low-side N-channel internal MOSFET gate drive supply, the source of the low-side MOSFET, the negative terminals of input capacitors, and the negative terminals of output capacitors. The loop for the power ground should be as small as possible and separate from the signal ground (SGND) loop.
3	NC	No connection.
4	SW	Switch node output. This is the internal connection for the high-side MOSFET source and low-side MOSFET drain. Due to the high-speed switching on this pin, the SW pin should be routed away from sensitive nodes.
5	PGND	See pin 2.
6	PGND	See pin 2.
7	PGND	See pin 2.
8	PGND	See pin 2.
9	SW	See pin 4.
10	SW	See pin 4.
11	SW	See pin 4.
12	SW	See pin 4.
13	PVIN	High-side N-channel internal MOSFET drain connection input. The PVIN operating voltage range is from 4.5V to 28V. Input capacitors between the PVIN pins and the power ground (PGND) are required, and these connections must be kept short.
14	PVIN	See pin 13.
15	PVIN	See pin 13.
16	PVIN	See pin 13.
17	PVIN	See pin 13.
18	PVIN	See pin 13.
19	PVIN	See pin 13.

Pin	Name	Description
20	BST	Boost output. This is the bootstrapped voltage to the high-side N-channel MOSFET driver. A Schottky diode is connected between the PVDD pin and the BST pin. A boost capacitor of 0.1µF is connected between the BST pin and the SW pin. A small resistor can be added at the BST pin in series with C_{BST} to slow the turn-on time of the high-side N-channel MOSFET.
21	PGND	See pin 2.
22	CS	Current sense input. The CS pin senses current by monitoring the voltage across the low-side MOSFET during the off-time. The current sensing is required for short-circuit protection. In order to sense the current accurately, use a Kelvin connection to connect the CS pin to the SW pin, which is internally connected to the low-side MOSFET drain. The CS pin is also the high-side MOSFET's output driver return.
23	SGND	Signal ground. SGND must be connected directly to the ground planes. Do not route the SGND pin to the PGND pad on the top layer (see section 5 for details).
24	FB	Feedback input. This is the input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.8V. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage.
25	PG	Power good output (open drain). The PG pin is externally tied to VDD through a 10kΩ pull-up resistor. A high output is asserted when V_{OUT} > 92% of nominal.
26	EN	Enable input. This pin allows logic-level control of the output. This pin is CMOS-compatible. Logic high = enable, logic low = shutdown. In the off state, the supply current of the device is greatly reduced (typically 5µA). Do not allow the EN pin to float—either tie the pin high to enable the ZSPM4023-09 or use a 10kΩ pull-up resistor to V_{IN} for logic-level control.
27	VIN	Power supply voltage input. This pin requires a bypass capacitor to PGND.
28	VDD	5V internal linear regulator output. The VDD supply is the power MOSFET gate drive supply voltage and the supply bus for the IC. VDD is created by internal LDO from VIN. When VIN < +5.5V, VDD should be tied to the PVIN pins. A 2.2µF ceramic capacitor from the VDD pin to SGND pins must be placed next to the ZSPM4023-09.

2.3. Theory of Operation

The ZSPM4023-09 is able to operate in either continuous mode or discontinuous mode. The operating mode is determined by the output of the zero-cross comparator (ZC) as shown in Figure 2.1.

2.3.1. Continuous Mode

In continuous mode, the output voltage is sensed by the ZSPM4023-09 feedback pin FB via the voltage divider R1 and R2, and compared to a 0.8V reference voltage V_{REF} at the error comparator through a low gain transconductance (g_m) amplifier. If the feedback voltage decreases and the output of the g_m amplifier is below 0.8V, then the error comparator will trigger the control logic and generate an on-time period.

The on-time period length is predetermined by the "FIXED t_{ON} ESTIMATE" circuitry:

$$t_{ON(estimated)} = \frac{V_{OUT}}{V_{IN} \times 600kHz} \quad (1)$$

Where

V_{OUT} = the output voltage

V_{IN} = the power stage input voltage

At the end of the on-time period, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. The off-time period length depends upon the feedback voltage in most cases. When the feedback voltage decreases and the output of the g_m amplifier is below 0.8V, the on-time period is triggered and the off-time period ends. If the off-time period determined by the feedback voltage is less than the minimum off-time $t_{OFF(MIN)}$, which is approximately 300ns, then the ZSPM4023-09 control logic will apply the $t_{OFF(MIN)}$ instead. The $t_{OFF(MIN)}$ is required to maintain enough energy in the boost capacitor (C_{BST}) to drive the high-side MOSFET.

The maximum duty cycle is obtained from the 300ns $t_{OFF(min)}$:

$$D_{max} = \frac{t_S - t_{OFF(min)}}{t_S} = 1 - \frac{300ns}{t_S} \quad (2)$$

Where

$$t_S = \frac{1}{f_{sw}} \qquad \text{For typical } f_{SW} = 600kHz,\ t_S = 1.66\mu s$$

Recommendation: Do not use ZSPM4023-09 with an off-time close to $t_{OFF(MIN)}$ during steady-state operation. Also, as V_{OUT} increases, the internal ripple injection will increase and reduce the line regulation performance. Therefore, the maximum output voltage of the ZSPM4023-09 should be limited to 5.5V and the maximum external ripple injection should be limited to 200mV. See section 3.1.5 for more details.

The actual on-time and resulting switching frequency will vary with the part-to-part variation in the rise and fall times of the internal MOSFETs, the output load current, and variations in the VDD voltage. Also, the minimum t_{ON} results in a lower switching frequency in applications with a high ratio for V_{IN} to V_{OUT}, such as 24V to 1.0V. For comparison, the minimum t_{ON} measured on the ZSPM4023-09 Evaluation Board is approximately 100ns. During load transients, the switching frequency is changed due to the varying off-time.

To illustrate the control loop operation, the steady-state and load-transient scenarios are analyzed below.

Figure 2.4 shows the ZSPM4023-09 control loop timing during steady-state operation. During the steady state, the g_m amplifier senses the feedback voltage ripple, which is proportional to the output voltage ripple and the inductor current ripple, to trigger the on-time period. The on-time is predetermined by the t_{ON} estimator. The termination of the off-time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when V_{FB} falls below V_{REF}, the off-time period ends and the next on-time period is triggered through the control logic circuitry.

Figure 2.4 ZSPM4023-09 Control Loop Timing –Continuous Mode

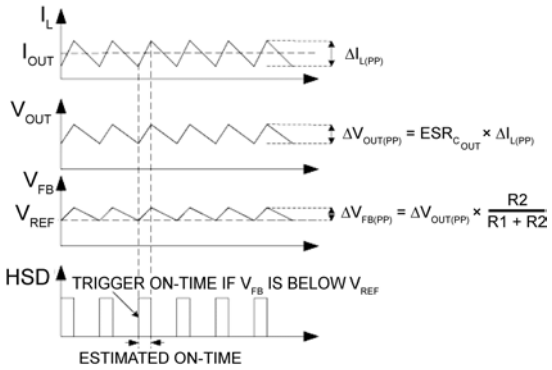
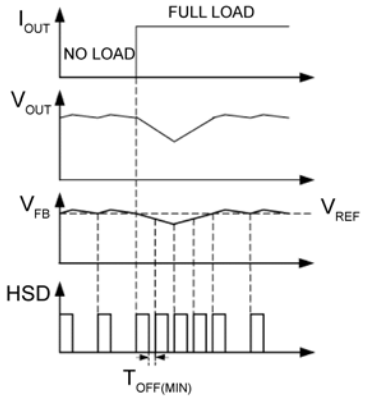


Figure 2.5 shows the operation of the ZSPM4023-09 during a load transient. The output voltage drops due to the sudden load increase, which causes the V_{FB} to be less than V_{REF}. This will cause the error comparator to trigger an on-time period. At the end of the on-time period, a minimum off-time $t_{OFF(MIN)}$ is generated to charge C_{BST} since the feedback voltage is still below V_{REF}. Then, the next on-time period is triggered due to the low feedback voltage. Therefore, the switching frequency changes during the load transient, but returns to the nominal fixed frequency once the output has stabilized at the new load current level. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small for the ZSPM4023-09 converter.

Figure 2.5 ZSPM4023-09 Load Transient Response



Unlike true current-mode control, the ZSPM4023-09 uses the output voltage ripple to trigger an on-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough. The ZSPM4023-09 control loop has the advantage of eliminating the need for slope compensation.

In order to meet the stability requirements, the ZSPM4023-09 feedback voltage ripple should be in phase with the inductor current ripple and large enough to be sensed by the g_m amplifier and the error comparator. The recommended feedback voltage ripple is 20mV to 100mV. If a low-ESR output capacitor is selected, then the feedback voltage ripple might be too small to be sensed by the g_m amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection is required to ensure proper operation. Please refer to section 3.1.4 for more details about the ripple injection technique.

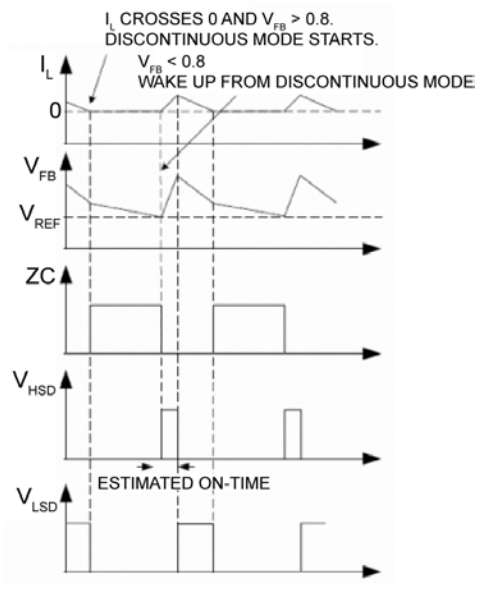
2.3.2. Discontinuous Mode

In continuous mode, the inductor current is always greater than zero; however at light loads, the ZSPM4023-09 is able to force the inductor current to operate in discontinuous mode. Discontinuous mode is where the inductor current falls to zero, as indicated by trace (I_L) shown in Figure 2.6. During this period, the efficiency is optimized by shutting down all the non-essential circuits and minimizing the supply current. The ZSPM4023-09 wakes up and turns on the high-side MOSFET when the feedback voltage V_{FB} drops below 0.8V.

The ZSPM4023-09 has a zero crossing comparator that monitors the inductor current by sensing the voltage drop across the low-side MOSFET during its ON-time. If the V_{FB} > 0.8V and the inductor current goes slightly negative, then the ZSPM4023-09 automatically powers down most of the IC circuitry and goes into a low-power mode.

Once the ZSPM4023-09 goes into discontinuous mode, both the low-side driver (LSD) and high-side driver (HSD) are low, which turns off the high-side and low-side MOSFETs. The load current is supplied by the output capacitors and V_{OUT} drops. If the drop of V_{OUT} causes V_{FB} to go below V_{REF}, then all the circuits will wake up into normal continuous mode. First, the bias currents of most circuits that had been reduced during the discontinuous mode are restored, and then a t_{ON} pulse is triggered before the drivers are turned on to avoid any possible glitches. Finally, the high-side driver is turned on. Figure 2.6 shows the control loop timing in discontinuous mode.

Figure 2.6 ZSPM4023-09 Control Loop Timing –Discontinuous Mode



During discontinuous mode, the zero-crossing comparator and the current-limit comparator are turned off. The bias current of most circuits are reduced. As a result, the total power supply current during discontinuous mode is only about 450µA, allowing the ZSPM4023-09 to achieve high efficiency in light load applications.

2.3.3. VDD Regulator

The ZSPM4023-09 provides a 5V regulated output for input voltage VIN ranging from 5.5V to 28V. When VIN < 5.5V, VDD should be tied to the PVIN pins to bypass the internal linear regulator.

2.3.4. Soft–Start

Soft-start reduces the power supply input surge current at startup by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time will draw a lower input surge current.

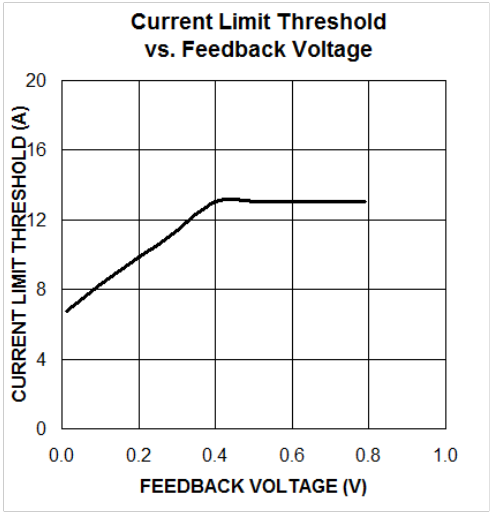
The ZSPM4023-09 implements an internal digital soft-start by making the 0.8V reference voltage V_{REF} ramp from 0 to 100% in about 5ms with 9.7mV steps. Therefore, the output voltage is controlled to increase slowly by a staircase V_{FB} ramp. Once the soft-start cycle ends, the related circuitry is disabled to reduce current consumption. VDD must be powered up at the same time or after VIN to make the soft-start function correctly.

2.3.5. Current Limit

The ZSPM4023-09 uses the $R_{DS(ON)}$ of the internal low–side power MOSFET to sense over-current conditions. This method will avoid adding the cost, board space requirements, and power losses taken by a discrete current-sense resistor. The low-side MOSFET is used because it displays much lower parasitic oscillations during switching than the high-side MOSFET.

In each switching cycle of the ZSPM4023-09 converter, the inductor current is sensed by monitoring the low-side MOSFET in the off-time period. If the inductor current is greater than 15A (typical), then the ZSPM4023-09 turns off the high-side MOSFET and a soft-start sequence is triggered. This mode of operation is called “hiccup mode” and its purpose is to protect the downstream load in case of a hard short. The load current-limit threshold has a foldback characteristic related to the feedback voltage as shown in Figure 2.7.

Figure 2.7 ZSPM4023-09 Current–Limit Foldback Characteristic



2.3.6. Power Good (PG)

The power good (PG) pin is an open drain output which indicates logic high when the output is nominally 92% of its steady-state voltage. A pull-up resistor ≥10kΩ should be connected from PG to VDD.

2.3.7. Internal MOSFET Gate Driver

The block diagram (Figure 2.1) shows a bootstrap circuit, consisting of D1 (a Schottky diode is recommended) and C_{BST}. This circuit supplies energy to the high-side drive circuit. Capacitor C_{BST} is charged while the low-side MOSFET is on, and the voltage on the SW pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to turn the MOSFET on. As the high-side MOSFET turns on, the voltage on the SW pin increases to approximately V_{IN}. Diode D1 is reverse biased and C_{BST} floats high while continuing to keep the high-side MOSFET on. The bias current of the high-side driver is less than 10mA so a 0.1µF to 1µF is sufficient to hold the gate voltage with minimal droop for the power stroke (high-side switching) cycle, i.e. ΔBST = 10mA x 1.67µs/0.1µF = 167mV. When the low-side MOSFET is turned back on, C_{BST} is then recharged through D1. A small resistor, R_G, can be placed in series with C_{BST} to slow the turn-on time of the high-side N-channel MOSFET.

The drive voltage is derived from the V_{DD} supply voltage. The nominal low-side gate drive voltage is PVDD and the nominal high-side gate drive voltage is approximately $V_{DD} – V_{DIODE}$, where V_{DIODE} is the voltage drop across D1. An approximately 30ns delay between the high-side and low-side driver transitions is used to prevent current from simultaneously flowing unimpeded through both MOSFETs.

3 Application Information

3.1. External Component Selection

3.1.1. Inductor Selection

Values for inductance, peak, and RMS currents are required in order to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents will increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value and therefore a larger and more expensive inductor. A good compromise between size, loss, and cost is to set the inductor ripple current to be equal to 20% of the maximum output current. The inductance value is calculated by equation (3).

$$L = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times f_{sw} \times 20\% \times I_{OUT(max)}} \quad (3)$$

Where

f_{SW} = switching frequency, 600kHz (nominal)

20% = ratio of AC ripple current to DC output current

$V_{IN(max)}$ = maximum power stage input voltage

The peak-to-peak inductor current ripple is

$$\Delta I_{L(pp)} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times f_{sw} \times L} \quad (4)$$

The peak inductor current is equal to the average output current plus one-half of the peak-to-peak inductor current ripple.

$$I_{L(pk)} = I_{OUT(max)} + 0.5 \times \Delta I_{L(pp)} \quad (5)$$

The RMS inductor current is used to calculate the I^2R losses in the inductor.

$$I_{L(RMS)} = \sqrt{I_{OUT(max)}^{2} + \frac{\Delta I_{L(PP)}^{2}}{12}} \quad (6)$$

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high frequency operation of the ZSPM4023-09 requires the use of ferrite materials for all but the most cost-sensitive applications. Lower cost iron powder cores can be used but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetics vendor.

Copper loss in the inductor is calculated by equation (7):

$$P_{INDUCTOR(Cu)} = I_{L(RMS)}^2 \times R_{WINDING} \quad (7)$$

The resistance of the copper wire, $R_{WINDING}$, increases with the temperature. The value of the winding resistance used should be at the operating temperature.

$$R_{WINDING(Ht)} = R_{WINDING(20°C)} \times (1 + 0.0042 \times (T_H - T_{20°C})) \quad (8)$$

Where

T_H = temperature of wire under full load

$T_{20°C}$ = ambient temperature

$R_{WINDING(20°C)}$ = room temperature winding resistance (usually specified by the manufacturer)

3.1.2. Output Capacitor Selection

The type of the output capacitor is usually determined by its equivalent series resistance (ESR). Its voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitor types are ceramic, low–ESR aluminum electrolytic, OS–CON, and POSCAP. The output capacitor's ESR is usually the main cause of the output ripple. The output capacitor ESR also affects the control loop from a stability point of view.

The maximum value of ESR is calculated with equation (9):

$$ESR_{C_{OUT}} \leq \frac{\Delta V_{OUT(pp)}}{\Delta I_{L(PP)}} \quad (9)$$

Where

$\Delta V_{OUT(pp)}$ = peak-to-peak output voltage ripple

$\Delta I_{L(PP)}$ = peak-to-peak inductor current ripple

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated in equation (10):

$$\Delta V_{OUT(pp)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{C_{OUT} \times f_{SW} \times 8}\right)^2 + \left(\Delta I_{L(PP)} \times ESR_{C_{OUT}}\right)^2} \quad (10)$$

Where

C_{OUT} = output capacitance value

f_{SW} = switching frequency

As described in section 2.3, the ZSPM4023-09 requires at least 20mV peak-to-peak ripple at the FB pin to make the g_m amplifier and the error comparator function properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitors value should be much smaller than the ripple caused by the output capacitor ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide the enough feedback voltage ripple. See section 3.1.4 for more details.

The voltage rating of the capacitor should be twice the output voltage for a tantalum capacitor and 20% greater for aluminum electrolytic or OS-CON capacitors. The output capacitor RMS current is calculated by equation (11):

$$I_{C_{OUT}(RMS)} = \frac{\Delta I_{L(PP)}}{\sqrt{12}} \quad (11)$$

The power dissipated in the output capacitor is

$$P_{DISS(C_{OUT})} = I_{C_{OUT}(RMS)}^2 \times ESR_{C_{OUT}} \quad (12)$$

3.1.3. Input Capacitor Selection

The input capacitor for the power stage input V_{IN} should be selected for ripple current rating and voltage rating. Tantalum input capacitors might fail when subjected to high inrush currents caused by turning the input supply on. A tantalum input capacitor's voltage rating should be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON, and multilayer polymer-film capacitors can handle the higher inrush currents without voltage de-rating. The input voltage ripple will primarily depend on the input capacitor's ESR. The peak input current is equal to the peak inductor current; therefore

$$\Delta V_{IN} = I_{L(pk)} \times C_{ESR} \quad (13)$$

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low, then

$$I_{CIN(RMS)} \approx I_{OUT(MAX)} \times \sqrt{D \times (1-D)} \quad (14)$$

Where

D = duty cycle

The power dissipated in the input capacitor is

$$P_{DISS(CIN)} = I_{CIN(RMS)}^{2} \times ESR_{CIN} \quad (15)$$

3.1.4. Ripple Injection

The V_{FB} ripple required for proper operation of the g_m amplifier and error comparator is 20mV to 100mV. However, the output voltage ripple is generally designed as 1% to 2% of the output voltage. For a low output voltage, such as a 1V, the output voltage ripple is only 10mV to 20mV, and the feedback voltage ripple is less than 20mV. If the feedback voltage ripple is so small that the g_m amplifier and error comparator cannot sense it, then the ZSPM4023-09 will lose control and the output voltage is not regulated. In order to have some amount of V_{FB} ripple, a ripple injection method is applied for low output voltage ripple applications. (Also see section 3.1.5 regarding internal ripple injection.)

Applications are divided into three conditions according to the amount of the feedback voltage ripple:

1. When there is enough ripple at the feedback voltage due to a large ESR for the output capacitors, the converter will be stable without any ripple injection. In this case, use the circuit shown in Figure 3.1. In this circuit, the ESR of the output capacitor is shown as a series resistance. The feedback voltage ripple is

$$\Delta V_{FB(pp)} = \frac{R_2}{R_1 + R_2} \times ESR_{C_{OUT}} \times \Delta I_{L(pp)} \quad (16)$$

   Where

   $\Delta I_{L(pp)}$ = the peak-to-peak value of the inductor current ripple

2. When there is inadequate ripple at the feedback voltage due to the small ESR of the output capacitors, use the circuit shown in Figure 3.2. The output voltage ripple is fed into the FB pin through a feed-forward capacitor C_{FF}. In this circuit, the typical C_{FF} value is between 1nF and 22nF. With the feed-forward capacitor, the feedback voltage ripple is very close to the output voltage ripple:

$$\Delta V_{FB(pp)} \approx ESR \times \Delta I_{L(pp)} \quad (17)$$

3. When there is virtually no ripple at the FB pin voltage due to the very-low ESR of the output capacitors, use the circuit shown in Figure 3.3. In this situation, the output voltage ripple is less than 20mV; therefore additional ripple must be injected into the FB pin from the switching node SW via a resistor R_{INJ} and a capacitor C_{INJ}. The injected ripple is

$$\Delta V_{FB(PP)} = V_{IN} \times K_{DIV} \times D \times (1 - D) \times \frac{1}{f_{SW} \times \tau} \quad (18)$$

$$K_{DIV} = \frac{R1//R2}{R_{INJ} + R1//R2} \quad (19)$$

Where

V_{IN} = power stage input voltage

D = duty cycle

f_{SW} = switching frequency

$\tau = (R1//R2//R_{INJ}) \times C_{FF}$ where // indicates components are in parallel; therefore use the equivalent resistance

Figure 3.1 Feedback Circuit if Sufficient Ripple is Present at FB for Stable Operation

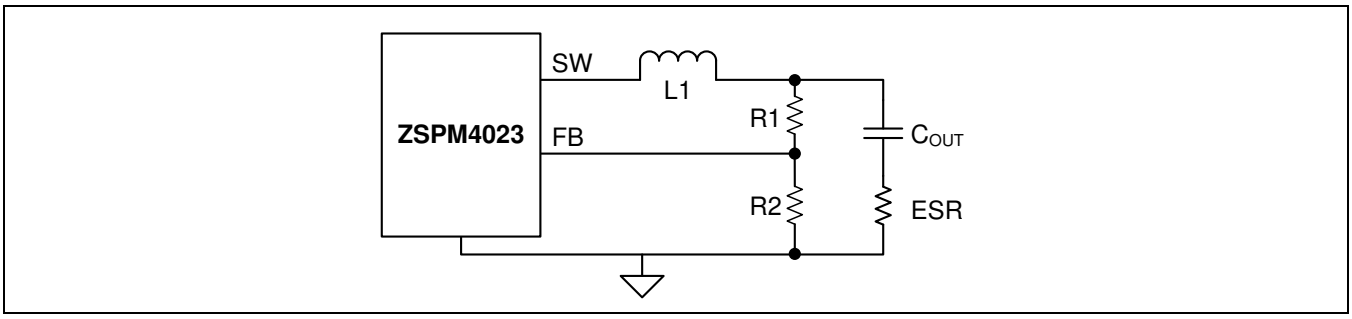


Figure 3.2 Ripple Injection Circuit for Supplementing Inadequate Ripple at FB to Prevent Unstable Operation

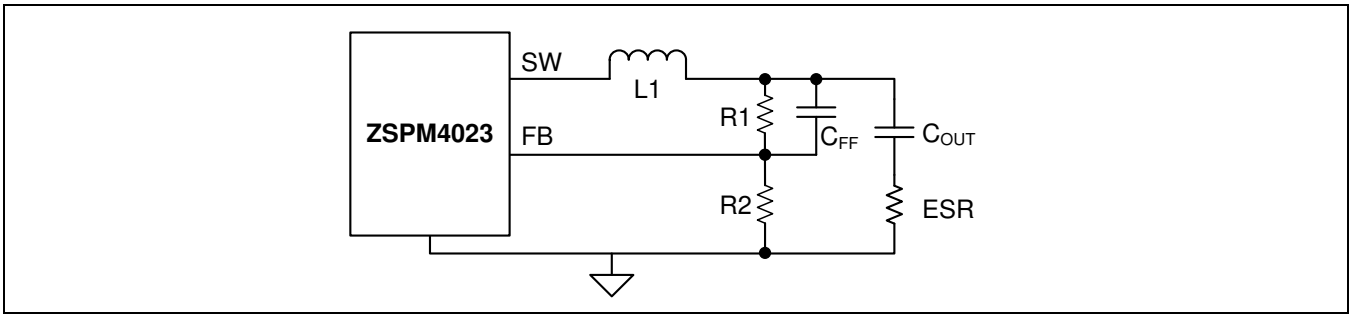
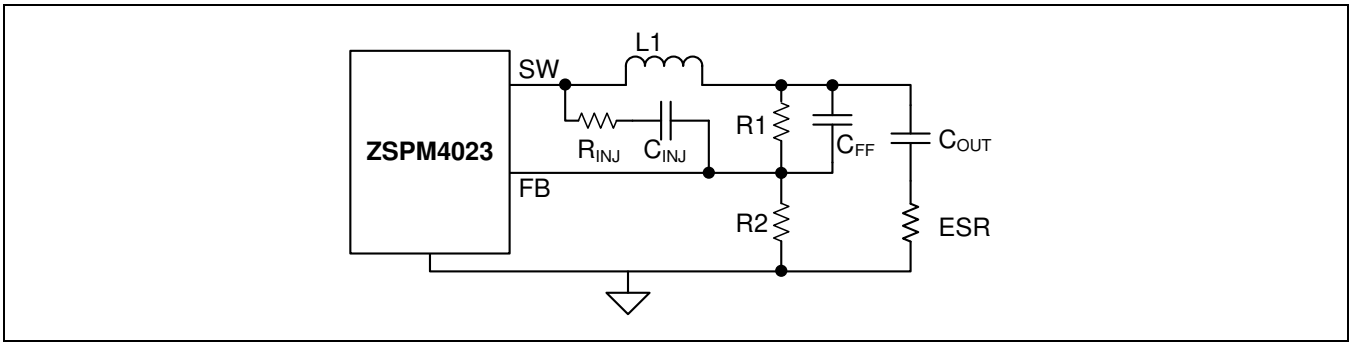


Figure 3.3 Ripple Injection Circuit for Preventing Unstable Operation if No Ripple is Present at FB



In Equations 18 and 19, it is assumed that the time constant associated with C_{FF} must be much greater than the switching period t_{SW}:

$$\frac{1}{f_{SW} \times \tau} = \frac{t_{SW}}{\tau} << 1 \tag{20}$$

If the voltage divider resistors R1 and R2 are in the kΩ range, a C_{FF} of 1nF to 22nF can easily satisfy the large time constant requirements. Also, a 100nF injection capacitor C_{INJ} is used in order to be considered as short for a wide range of the frequencies.

The process of sizing the ripple injection resistor and capacitors in Figure 3.3 requires three steps:

Step 1 Select C_{FF} to feed all output ripples into the feedback pin and ensure that the large time constant assumption is satisfied. A typical choice for C_{FF} is 1nF to 22nF if R1 and R2 are in the kΩ range.

Step 2 Select R_{INJ} according to the expected feedback voltage ripple using equation (21):

$$K_{DIV} = \frac{\Delta V_{FB(PP)}}{V_{IN}} \times \frac{f_{SW} \times \tau}{D \times (1 - D)} \tag{21}$$

Then the value of R_{inj} is obtained as

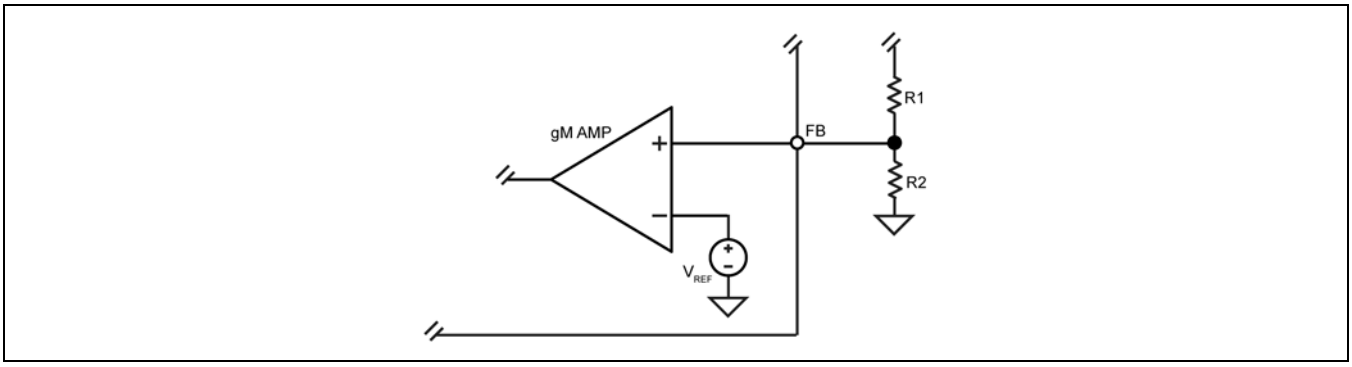
$$R_{INJ} = (R1 // R2) \times \left(\frac{1}{K_{DIV}} - 1\right) \tag{22}$$

Step 3 Select C_{INJ} as 100nF, which could be considered as a short for a wide range of the frequencies.

3.1.5. Setting the Output Voltage

The ZSPM4023-09 requires two resistors to set the output voltage as shown in Figure 3.4.

Figure 3.4 Voltage Divider Configuration



The output voltage is determined by equation (23):

$$V_O = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad (23)$$

Where

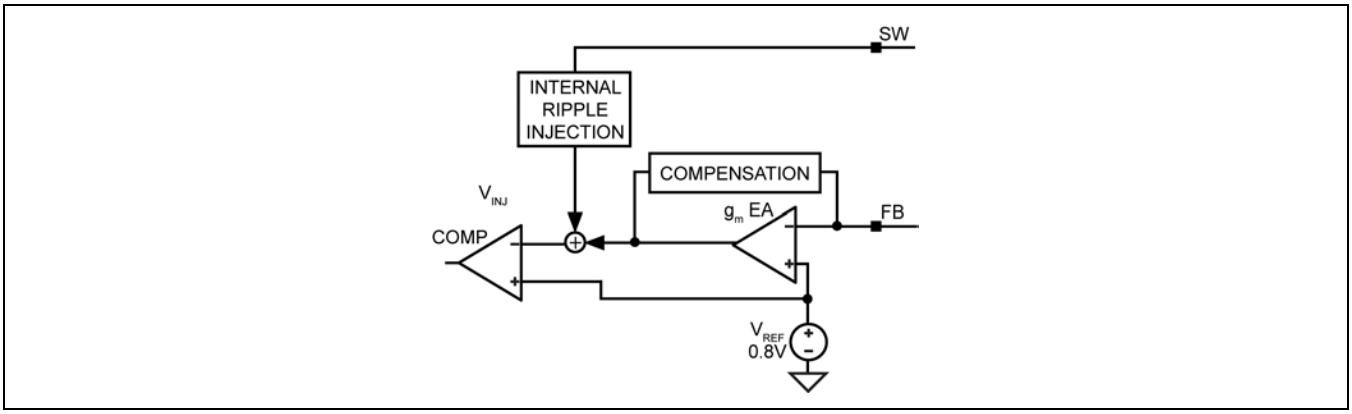
V_{FB} = 0.8V

A typical value of R1 can be between 3kΩ and 10kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small, it will decrease the efficiency of the power supply, especially at light loads. Once R1 is selected, R2 can be calculated using equation (24):

$$R2 = \frac{V_{FB} \times R1}{V_{OUT} - V_{FB}} \quad (24)$$

In addition to the external ripple injection added at the FB pin, internal ripple injection is added at the inverting input of the comparator inside the ZSPM4023-09, as shown in Figure 3.5. The inverting input voltage V_{INJ} is clamped to 1.2V. As V_{OUT} is increased, the swing of V_{INJ} will be clamped. The clamped V_{INJ} reduces the line regulation because it is reflected as a DC error on the FB terminal. Therefore, the maximum output voltage of the ZSPM4023-09 should be limited to 5.5V to avoid this problem.

Figure 3.5 Internal Ripple Injection



3.2. Thermal Measurements

Measuring the ZSPM4023-09's case temperature is recommended to ensure it is within its operating limits. Although this might seem like a very elementary task, it is easy to get erroneous results. The most common mistake is to use the standard thermal couple that comes with a thermal meter. This thermal couple wire gauge is large, typically 22 gauge, and behaves like a heat sink, resulting in a lower case measurement.

The two methods of temperature measurement are using a smaller thermal couple wire or using an infrared thermometer. If a thermal couple wire is used, it must be constructed of 36 gauge wire or higher (smaller wire size) to minimize the wire heat-sinking effect. In addition, the thermal couple tip must be covered in either thermal grease or thermal glue to make sure that the thermal couple junction is making good contact with the case of the ZSPM4023-09. Omega®* brand thermal couple (5SC-TT-K-36-36) is adequate for most applications.

Wherever possible, an infrared thermometer is recommended. The measurement spot size of most infrared thermometers is too large for an accurate reading on small form factor ICs. However, an IR thermometer from Optris®† has a 1mm spot size, which makes it a good choice for measuring the hottest point on the case. An optional stand makes it easy to hold the beam on the ZSPM4023-09 for long periods of time.

In addition to the case temperature, ambient temperature, T_A, is also of importance in the calculation of power dissipation using the equation in Note 1 of section 1.2. T_A should be measured 1 inch away from the package on the printed circuit board. This can be measured using a thermocouple or an infrared thermometer.

* Omega® is a trademark of OMEGA Engineering, Inc.

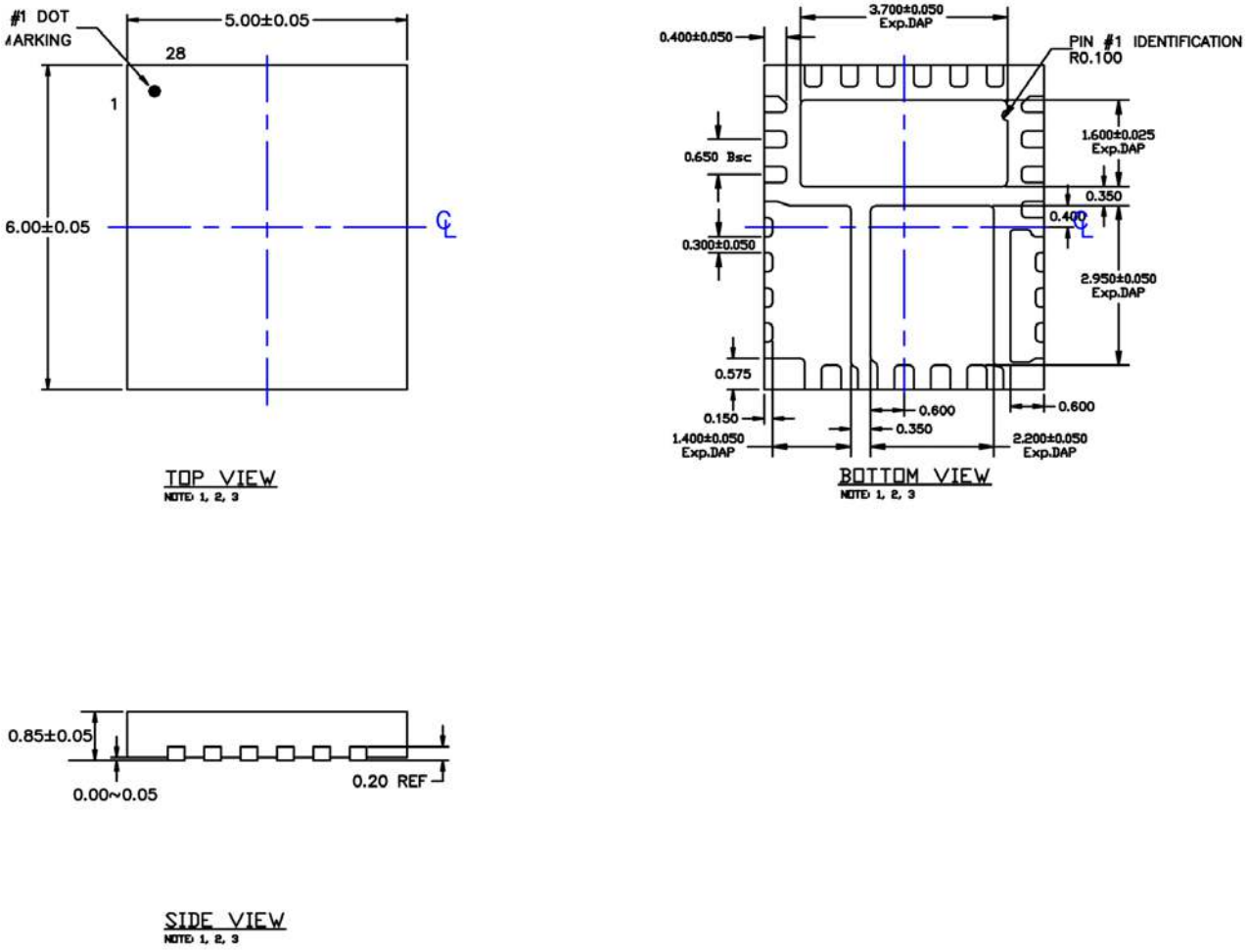
† Optris® is a trademark of Optris GmbH.

4 Mechanical Specifications

4.1. Package Dimensions

All dimensions are in millimeters.

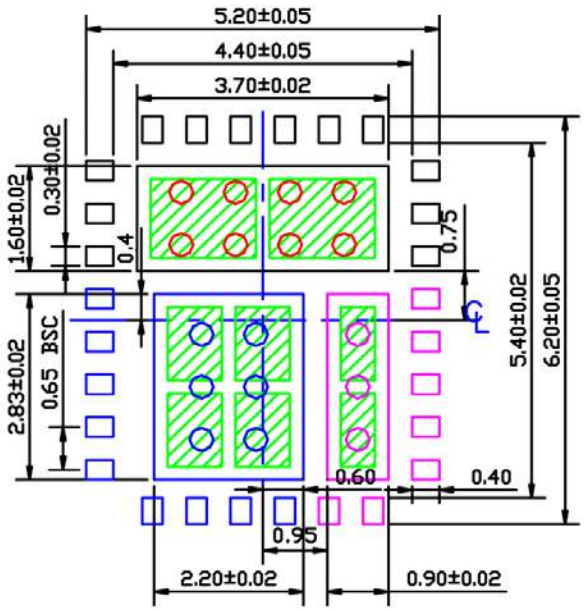
Figure 4.1 Package Drawing—28-pin 5mm × 6mm QFN (JL) Package



Notes:

1. Maximum package warpage is 0.05mm.
2. Maximum allowable burr is 0.076mm in all directions.
3. Pin 1 is on top and will be laser marked.

4.2. Recommended Land Pattern



Red circles in the land pattern represent thermal vias and must be connected to GND plane for maximum thermal performance.

Green rectangle (with shaded area) indicates solder stencil opening on exposed pad area.

Blue and Magenta colored pads indicate different potentials. **DO NOT connect to GND plane.**

	Thermal Via	Via Size/Pitch	Solder Stencil Opening/ Pitch
Red Circle/Black Pad	X	0.300 – 0.35mm/0.80mm	1.55×1.20mm/1.75mm
Blue Circle/Black Pad	X	0.300 – 0.35mm/0.80mm	0.80×1.11mm/1.31mm
Magenta Circle/Black Pad	X	0.300 – 0.35mm/0.80mm	0.50×1.11mm/1.31mm

5 PCB Layout Guidelines

IMPORTANT WARNING: To minimize EMI and output noise, follow these layout recommendations. PCB layout is critical to achieve reliable, stable, and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths. The following guidelines should be followed to ensure proper operation of the ZSPM4023-09 regulator.

5.1. ZSPM4023-09

- Place the ZSPM4023-09 close to the point-of-load (POL).
- Use wide traces to route the input and output power lines.
- Keep signal and power grounds separate and connected at only one location.

- A 2.2µF ceramic capacitor that is connected to the PVDD pin must be located immediately next to the ZSPM4023-09. The PVDD pin is very noise sensitive and placement of the capacitor is very critical. Use wide traces to connect to the PVDD and PGND pins.
- A 1µF ceramic capacitor must be placed immediately between VDD and the signal ground SGND. The SGND must be connected directly to the ground planes. Do not route the SGND pin to the PGND Pad on the top layer.

5.2. Input Capacitor

- Place the input capacitors on the same side of the board and as close to the ZSPM4023-09 as possible.
- Keep both the PVIN pin and PGND connections short.
- Place several vias to the ground plane close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not substitute any other type of capacitor for the ceramic input capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be de-rated by 50%.
- In “Hot-Plug” applications, a tantalum or electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply if power is suddenly applied.

5.3. Inductor

- Keep the connection short between the inductor and the switch node (SW).
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- Connect the CS pin directly to the SW pin to accurately sense the voltage across the low-side MOSFET.
- To minimize noise, place a ground plane underneath the inductor.
- The inductor can be placed on the opposite side of the board with respect to the ZSPM4023-09. It does not matter whether the IC or inductor is on the top or bottom as long as there is enough airflow to keep the power components within their temperature limits. The input and output capacitors must be placed on the same side of the board as the IC.

5.4. Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- The phase margin will change as the output capacitor value and ESR changes. The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.

5.5. Optional RC Snubber

Place the RC snubber on either side of the board and as close to the SW pin as possible. The intention is to damp parasitic LC resonators that are responsible for the ringing in the waveform of the signal at the SW pin. This provides damping by putting a resistor in “parallel” to the oscillating circuit.

6 Ordering Information

Product Sales Code	Description	Package
ZSPM4023AA1W09	ZSPM4023-09 QFN28 5mmx6mm — Temperature range: –40°C to +125°C	7” reel with 1000 ICs
ZSPM4023-09-KIT	Evaluation Kit for ZSPM4023-09, including ZSPM4023-09 Evaluation Board	Kit

Visit IDT’s website www.IDT.com or contact your nearest sales office for the latest version of these documents.

7 Related Documents

Document
ZSPM4023-06 Data Sheet
ZSPM4023-12 Data Sheet
ZSPM4022-06 Data Sheet
ZSPM4022-09 Data Sheet
ZSPM4022-12 Data Sheet
*ZSPM4023/4022-KIT Evaluation Kit Manual **
*ZSPM4023/4022 Application Note –Application Circuit Layout and Component Selection **

Visit the ZSPM4023 product page at www.IDT.com/ZSPM4023 or contact your nearest sales office for the latest version of these documents.

* Note: Documents marked with an asterisk (*) require a login.

8 Glossary

Term	Description
HSD	High-Side Driver
LDO	Low-Dropout Regulator
LSD	Low-Side Driver
UVLO	Under-Voltage Lockout
ZC	Zero-Crossing

9 Document Revision History

Revision	Date	Description
1.00	October 16, 2013	First release of document.
1.01	July 28, 2014	Update for cover imagery. Update for contact information.
	January 27, 2016	Changed to IDT branding.

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