19-3945; Rev 1; 7/06

IEEE 802.3af PD Interface and PWM Controllers with Integrated Power MOSFETs

General Description

The MAX5953A/MAX5953B/MAX5953C/MAX5953D integrate a complete power IC solution for Powered Devices (PD) in a Power-Over-Ethernet (PoE) system, in compliance with the IEEE 802.3af standard. The MAX5953A/MAX5953B/MAX5953C/MAX5953D provide the PD with a detection signature, a classification signature, and an integrated isolation switch with programmable inrush current control. These devices also integrate a voltage-mode PWM controller with two power MOSFETs connected in a two-switch voltage-clamped DC-DC converter configuration.

An integrated MOSFET provides PD isolation during detection and classification. All devices guarantee a leakage current offset of less than 10µA during the detection phase. A programmable current limit prevents high inrush current during power-on. The devices feature power-mode undervoltage lockout (UVLO) with wide hysteresis and long deglitch time to compensate for twisted-pair-cable resistive drop and to assure glitch-free transition between detection, classification, and power-on/-off phases. The MAX5953A/MAX5953C have an adjustable UVLO threshold with the default value compliant to the 802.3af standard, while the MAX5953B/MAX5953D have a lower and fixed UVLO threshold compatible with some legacy pre-802.3af power-sourcing equipment (PSE) devices.

The DC-DC converters are operable in either forward or flyback configurations with a wide input voltage range from 11V to 76V and up to 15W of output power. The voltage-clamped power topology enables full recovery of stored magnetizing and leakage inductive energy for enhanced efficiency and reliability. When using the high-side MOSFET, the controller can be configured as a buck converter. A look-ahead signal for driving secondary-side synchronous rectifiers can be used to increase efficiency. A wide array of protection features include UVLO, over-temperature shutdown, and short-circuit protection with hiccup current limit for enhanced performance and reliability. Operation up to 500kHz allows for smaller external magnetics and capacitors.

The MAX5953A/MAX5953B/MAX5953C/MAX5953D are available in a high-power (2.22W), 7mm x 7mm thermally enhanced thin QFN package.

Applications

- IEEE 802.3af Powered Devices
- IP Phones
- Wireless Access Nodes
- Internet Appliances
- Security Cameras
- Computer Telephony

Features

- **Powered Device Interface**
  - **Fully Integrated IEEE 802.3af-Compliant PD Interface**
  - **PD Detection and Programmable Classification Signatures**
  - **Less than 10µA Leakage Current Offset During Detection**
  - **Integrated MOSFET for Isolation and Inrush Current Limiting**
  - **Gate Output Allows External Control of the Internal Isolation MOSFET**
  - **Programmable Inrush Current Control**
  - **Programmable Undervoltage Lockout (MAX5953A/MAX5953C)**
- **DC-DC Converter**
  - **Clamped, Two-Switch Power IC for High Efficiency**
  - **Integrated High-Voltage 0.4Ω Power MOSFETs Up to 15W Output Power**
  - **Bias Voltage Regulator with Automatic High-Voltage Supply Turn-Off**
  - **11V to 76V Wide Input Voltage Range**
  - **Feed-Forward Voltage-Mode Control for Fast Input Transient Rejection**
  - **Programmable Undervoltage Lockout**
  - **Overtemperature Shutdown**
  - **Indefinite Short-Circuit Protection with Programmable Fault Integration**
  - **Integrated Look-Ahead Signal for Secondary-Side Synchronous Rectification**
  - **> 90% Efficiency with Synchronous Rectification**
  - **Up to 500kHz Switching Frequency**
- **High-Power (2.22W), 7mm x 7mm Thermally Enhanced Lead-Free Thin QFN Package**

Ordering Information

PART	PIN-PACKAGE	PKG CODE
MAX5953AUTM+	48 TQFN	T4877-6
MAX5953BUTM+	48 TQFN	T4877-6
MAX5953CUTM+	48 TQFN	T4877-6
MAX5953DUTM+	48 TQFN	T4877-6

Operating junction temperature range is 0°C to +125°C.
+Denotes lead-free package.

Pin Configuration and Typical Operating Circuit appear at end of data sheet.

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ABSOLUTE MAXIMUM RATINGS

V+ to V_{EE} ....-0.3V to +90V
OUT, PGOOD, $\overline{PGOOD}$ to V_{EE} ....-0.3V to (V+ + 0.3V)
RCLASS, GATE to V_{EE} ....-0.3V to +12V
UVLO to V_{EE} .... -0.3V to +8V
PGOOD to OUT .... -0.3V to (V+ + 0.3V)
HVIN, INBIAS, DRNH, XFRMRH,
XFRMRL to GND....................-0.3V to +80V
BST to GND .... -0.3V to +95V
BST to XFRMRH .... -0.3V to +12V
PGND to GND ....-0.3V to +0.3V
DCUVLO, RAMP, CSS, OPTO, FLTINT, RCFF,
RTCT to GND.................... -0.3V to +12V
SRC, CS to GND.................... -0.3V to +6V
REGOUT, DRVIN to GND ....-0.3V to +12V
REGOUT to HVIN .... -80V to +0.3V
REGOUT to INBIAS .... -80V to +0.3V
PPWM to GND....................-0.3V to (V_{REGOUT} + 0.3V)

Maximum Input/Output Current (Continuous)
OUT to V_{EE} 500mA
V+, RCLASS to V_{EE} 70mA
UVLO, PGOOD, $\overline{PGOOD}$ to V_{EE} 20mA
GATE to V_{EE} 80mA
REGOUT to GND 50mA
DRNH, XFRMRH, XFRMRL, SRC to GND (Average),
T_J = +125°C....................0.9A
PPWM to GND ....±20mA
Continuous Power Dissipation* (T_A = +70°C)
48-Pin TQFN 7mm X 7mm
(derate 27.8mW/°C above +70°C)....................2222mW
θ_{JA} ....36°C/W
Operating Ambient Temperature Range ....0°C to +85°C
Operating Junction Temperature Range ....0°C to +125°C
Junction Temperature ....+150°C
Storage Temperature Range ....-60°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

*As per JEDEC 51 standard.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = (V+ - V_{EE}) = 48V, GATE = PGOOD = $\overline{PGOOD}$ = unconnected, GND = OUT, HVIN = V+, UVLO = V_{EE}, T_J = 0°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C. All voltages are referenced to V_{EE}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWERED DEVICE (PD) INTERFACE							
DETECTION MODE							
Input Offset Current	I_{OFFSET}	V_{IN} = 1.4V to 10.1V (Note 2)				10	µA
Effective Differential Input Resistance (Note 3)	dR	V_{IN} = 1.4V, up to 10.1V with 1V step		550			kΩ
CLASSIFICATION MODE							
Classification Current Turn-Off Threshold	$V_{TH,CLASS}$	V_{IN} rising (Note 4)		20.8	21.8	22.5	V
Classification Current	I_{CLASS}	V_{IN} = 12.6V to 20V, R_{DISC} = 25.5kΩ (Notes 5, 6)	Class 0, R_{RCLASS} = 10kΩ	0		2	mA
			Class 1, R_{RCLASS} = 732Ω	9.17		11.83	
			Class 2, R_{RCLASS} = 392Ω	17.29		19.71	
			Class 3, R_{RCLASS} = 255Ω	26.45		29.55	
			Class 4, R_{RCLASS} = 178Ω	36.6		41.4	
POWER MODE							
Operating Supply Voltage	V_{IN}	V_{IN} = (V+ - V_{EE})				67	V
Operating Supply Current	I_{IN}	Measure at V+, not including R_{DISC}, GATE = V_{EE}, HVIN = GND = OUT			0.4	1	mA
Default Power Turn-On Voltage	$V_{UVLO,ON}$	V_{IN} increasing	MAX5953A/MAX5953C	37.4	38.6	40.2	V
			MAX5953B/MAX5953D	34.3	35.4	36.9	
Default Power Turn-Off Voltage	$V_{UVLO,OFF}$	V_{IN} decreasing, MAX5953A/MAX5953C		30			V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = (V+ - V_{EE}) = 48V, GATE = PGOOD = $\overline{PGOOD}$ = unconnected, GND = OUT, HVIN = V+, UVLO = V_{EE}, T_J = 0°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C. All voltages are referenced to V_{EE}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Default Power Turn-On/Off Hysteresis Voltage	$V_{HYST,UVLO}$	MAX5953A/MAX5953C	7.1			V
		MAX5953B/MAX5953D	4			
External UVLO Programming Range	$V_{IN,EX}$	MAX5953A/MAX5953C only (Note 7)	12		67	V
UVLO External Reference Voltage	$V_{REF,UVLO}$	V_{UVLO} increasing	2.400	2.460	2.522	V
UVLO External Reference Voltage Hysteresis	$V_{HYST,UVLO}$	Ratio to $V_{REF, UVLO}$	19.2	20	20.9	%
UVLO Bias Current	$I_{IN,UVLO}$	V_{UVLO} = 2.460V	-1.5		+1.5	µA
UVLO Input Ground-Sense Threshold	$V_{TH,G,UVLO}$	(Note 8)	50		440	mV
UVLO Input Ground-Sense Glitch Rejection				7		µs
Power Turn-Off Voltage, Undervoltage Lockout Deglitch Time	t_{OFF_DLY}	V_{IN}, V_{UVLO} falling (Note 9)	0.32			ms
Isolation Switch n-Channel MOSFET On-Resistance	$R_{ON,ISO}$	Output current = 300mA, V_{GATE} = 5.6V, measured between OUT and V_{EE}		0.6	1.5	Ω
Isolation Switch n-Channel MOSFET Off-Threshold Voltage	V_{GSTH}	V_{GATE} - V_{EE}, OUT = V+, output current < 1µA	0.5			V
GATE Pulldown Switch Resistance	R_G	Power-off mode, V_{IN} = +12V		38	80	Ω
GATE Charging Current	I_{GATE}	V_{GATE} = 2V	4.5	10	16.5	µA
GATE High Voltage	V_{GATE}	I_{GATE} = 1µA	5.59	5.76	5.93	V
PGOOD Assertion V_{OUT} Threshold (Note 10)	V_{OUTEN}	V_{OUT} - V_{EE} decreasing, V_{GATE} = 5.75V	1.16	1.23	1.31	V
		Hysteresis		70		mV
PGOOD, $\overline{PGOOD}$ Assertion V_{GATE} Threshold	V_{GSEN}	V_{GATE} - V_{EE} increasing	4.62	4.76	4.91	V
		Hysteresis		80		mV
PGOOD, $\overline{PGOOD}$ Output Low Voltage	$V_{OL,PGOOD}$	I_{SINK} = 2mA, V_{OUT} ≤ (V+ - 5V) (Note 11)			0.2	V
PGOOD Leakage Current		GATE = high, V+ - V_{OUT} = 67V (Note 11)			1	µA
$\overline{PGOOD}$ Leakage Current		GATE = V_{EE}, $\overline{PGOOD}$ - V_{EE} = 67V (Note 11)			1	µA

IEEE 802.3af PD Interface and PWM Controllers with Integrated Power MOSFETs

ELECTRICAL CHARACTERISTICS (DC-DC Controller)

(All voltages referenced to GND, unless otherwise noted. V_{HVIN} = +48V, C_{INBIAS} = 1µF, C_{REGOUT} = 2.2µF, R_{RTCT} = 25kΩ, C_{RTCT} = 100pF, C_{BST} = 0.22µF, V_{CSS} = V_{CS} = 0V, V_{RAMP} = V_{DCUVLO} = 3V, T_J = 0°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Range	V_{HVIN}		11		76	V
OSCILLATOR (RTCT)						
PWM Frequency	f_S			250		kHz
Maximum PWM Duty Cycle	D_{MAX}			47		%
Maximum RTCT Frequency	$f_{RTCTMAX}$	(Note 12)		1		MHz
RTCT Peak Trip Level	$V_{TH,RTCT}$			0.51 x V_{REGOUT}		V
RTCT Valley Trip Level	$V_{TL,RTCT}$			1		V
RTCT Input Bias Current	$I_{IN,RTCT}$			±1		µA
RTCT Discharge MOSFET $R_{DS(ON)}$	$R_{DIS,RTCT}$	Sinking 50mA		35	85	Ω
RTCT Discharge Pulse Width				50		ns
LOOK-AHEAD LOGIC (PPWM)						
PPWM to Output Propagation Delay	t_{PPWM}	V_{PPWM} rising to V_{XFRMRL} falling		110		ns
PPWM Output High	$V_{OH,PPWM}$	Sourcing 2mA	7.0		11.0	V
PPWM Output Low	$V_{OL,PPWM}$	Sinking 2mA			0.2	V
PWM COMPARATOR (OPTO, RAMP, RCFF)						
Common-Mode Input Range	V_{CM_PWM}		0		5.5	V
Input Offset Voltage				10		mV
Input Bias Current			-2		+2	µA
RAMP to XFRMRL Propagation Delay	$t_{COMPARATOR}$	From V_{RAMP} (50mV overdrive) rising to V_{XFRMRL} rising		100		ns
Minimum OPTO Voltage		V_{CSS} = 0V, OPTO sinking 2mA		1.47		V
Minimum RCFF Voltage		RCFF sinking 2mA		2.18		V
REGOUT LDO (REGOUT)						
REGOUT Voltage Set Point	V_{REGOUT}	INBIAS unconnected, V_{HVIN} = 11V to 76V	8.3	8.75	9.2	V
		V_{INBIAS} = V_{HVIN} = 11V to 76V	9.5	10.6	11.0	
REGOUT Load Regulation		INBIAS unconnected, V_{HVIN} = 15V, I_{REGOUT} = 0 to 30mA			0.25	V
		V_{INBIAS} = V_{HVIN} = 15V, I_{REGOUT} = 0 to 30mA			0.25	
REGOUT Dropout Voltage		INBIAS unconnected, I_{REGOUT} = 30mA			1.25	V
		V_{INBIAS} = V_{HVIN}, I_{REGOUT} = 30mA			1.25	
REGOUT Undervoltage Lockout Threshold		REGOUT rising	6.6	7.0	7.4	V
REGOUT Undervoltage Lockout Threshold Hysteresis		REGOUT falling		0.7		V

ELECTRICAL CHARACTERISTICS (DC-DC Controller) (continued)

(All voltages referenced to GND, unless otherwise noted. V_{HVIN} = +48V, C_{INBIAS} = 1µF, C_{REGOUT} = 2.2µF, R_{RTCT} = 25kΩ, C_{RTCT} = 100pF, C_{BST} = 0.22µF, V_{CSS} = V_{CS} = 0V, V_{RAMP} = V_{DCUVLO} = 3V, T_J = 0°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SOFT-START (CSS)						
Soft-Start Current	I_{CSS}	V_{CSS} = 0V		33		µA
INTEGRATING FAULT PROTECTION						
FLTINT Source Current	I_{FLTINT}			80		µA
FLTINT Trip Point		V_{FLTINT} rising		2.7		V
FLTINT Hysteresis				0.75		V
INTERNAL POWER FETs						
On-Resistance	$R_{ON,POWER}$	V_{DRVIN} = V_{BST} = 9V, V_{XFRMRH} = V_{SRC} = 0V, I_{DS} = 50mA		0.4	0.8	Ω
Off-State Leakage Current			-5		+10	µA
Total Gate Charge Per Power FET				15		nC
HIGH-SIDE DRIVER						
Low to High Latency	t_{LH-HS}	Driver delay until FET V_{GS} reaches 0.9 x (V_{BST} - V_{XFRMRH}) and is fully on		80		ns
High to Low Latency	t_{HL-HS}	Driver delay until FET V_{GS} reaches 0.1 x (V_{BST} - V_{XFRMRH}) and is fully off		40		ns
Output Drive Voltage	V_{BST}	BST to XFRMRH with high side on		8		V
LOW-SIDE DRIVER						
Low to High Latency	t_{LH-LS}	Driver delay until FET V_{GS} reaches 0.9 x V_{DRVIN} and is fully on		80		ns
High to Low Latency	t_{HL-LS}	Driver delay until FET V_{GS} reaches 0.1 x V_{DRVIN} and is fully off		40		ns
CURRENT-LIMIT COMPARATOR (CS)						
Current-Limit Threshold Voltage	V_{ILIM}		140	156	172	mV
Current-Limit Input Bias Current	I_{BILIM}	0 < V_{CS} < 0.3V	-2		+2	µA
Propagation Delay to XFRMRL	t_{dILIM}	From V_{CS} rising (10mV overdrive) to V_{XFRMRL} rising		160		ns
BOOST VOLTAGE CIRCUIT (See Figure 9, QB)						
Driver Output Delay	t_{PPWMD}			200		ns
One-Shot Pulse Width	t_{PWQB}			300		ns
QB R_{DSON}		Sinking 20mA		30	60	Ω
THERMAL SHUTDOWN						
Shutdown Temperature	T_{SH}	Temperature rising		+160		°C
Thermal Hysteresis	T_H			20		°C

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ELECTRICAL CHARACTERISTICS (DC-DC Controller) (continued)

(All voltages referenced to GND, unless otherwise noted. V_{HVIN} = +48V, C_{INBIAS} = 1µF, C_{REGOUT} = 2.2µF, R_{RTCT} = 25kΩ, C_{RTCT} = 100pF, C_{BST} = 0.22µF, V_{CSS} = V_{CS} = 0V, V_{RAMP} = V_{DCUVLO} = 3V, T_J = 0°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UNDERVOLTAGE LOCKOUT (DCUVLO)						
Threshold Voltage	$V_{REF,DCUVLO}$	V_{DCUVLO} rising	1.14	1.26	1.38	V
Hysteresis	$V_{HYS,DCUVLO}$			140		mV
Input Bias Current	$I_{IN,DCUVLO}$	V_{DCUVLO} = 3V	-100		+100	nA
SUPPLY CURRENT						
Supply Current		From V_{HVIN} = 11V to 76V, V_{CSS} = 0V, V_{INBIAS} = 11V		0.7	1.5	mA
		From V_{INBIAS} = 11V to 76V, V_{CSS} = 0V, V_{HVIN} = 76V		4.4	6.4	
		From V_{HVIN} = 76V, V_{OPIO} = 4V		7		
Standby Supply Current		V_{DCUVLO} = 0V			1	mA

Note 1: Limits at 0°C are guaranteed by design, unless otherwise noted.
Note 2: The input offset current is illustrated in Figure 1.
Note 3: Effective differential input resistance is defined as the differential resistance between V+ and V_{EE} without any external resistance.
Note 4: Classification current is turned off whenever the IC is in power mode.
Note 5: See Table 2 in the *Classification Mode* section. R_{DISC} and R_{RCLASS} must be 1%, 100ppm or better. I_{CLASS} includes the IC bias current and the current drawn by R_{DISC}.
Note 6: See the *Thermal Dissipation* section.
Note 7: When UVLO is connected to the midpoint of an external resistor-divider with a series resistance of 25.5kΩ (±1%), the turn-on threshold set point for the power mode is defined by the external resistor-divider. Make sure the voltage on UVLO does not exceed its maximum rating of 8V when V_{IN} is at the maximum voltage.
Note 8: When V_{UVLO} is below $V_{TH,G,UVLO}$, the MAX5953A/MAX5953C set the turn-on voltage threshold internally ($V_{UVLO,ON}$).
Note 9: An input voltage or V_{UVLO} glitch below their respective thresholds shorter than or equal to t_{OFF_DLY} does not cause the MAX5953A/MAX5953B/MAX5953C/MAX5953D to exit power-on mode (as long as the input voltage remains above an operable voltage level of 12V).
Note 10: Guaranteed by design, not tested in production for MAX5953B/MAX5953D.
Note 11: PGOOD references to OUT while $\overline{PGOOD}$ references to V_{EE}.
Note 12: Output switching frequency is 1/2 oscillator frequency.

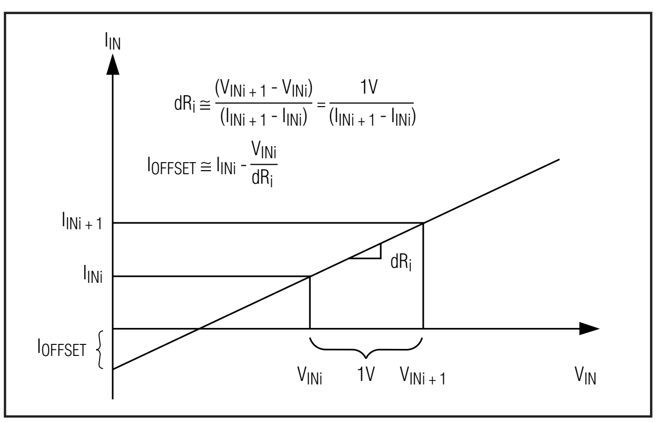

Figure 1. Effective Differential Input Resistance/Offset Current

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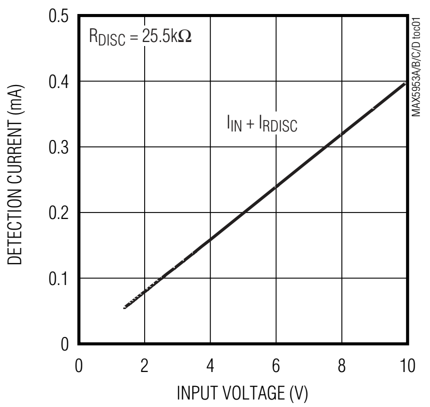
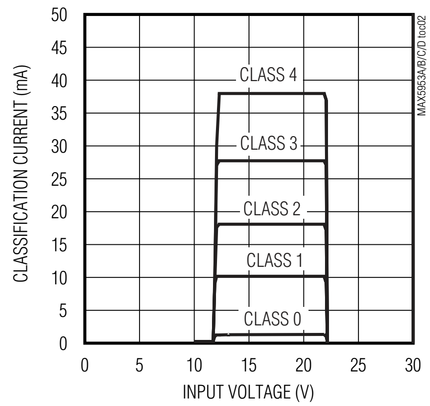
Typical Operating Characteristics

(V_{IN} = (V+ - V_{EE}) = 48V, GATE = PGOOD = unconnected, GND connected to OUT, HVIN connected to V+, UVLO = V_{EE}, C_{INBIAS} = 1µF, C_{REGOUT} = 2.2µF, R_{RTCT} = 25kΩ, C_{RTCT} = 100pF, C_{BST} = 0.22µF, T_J = 0°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C. All voltages are referenced to V_{EE}, unless otherwise noted.)

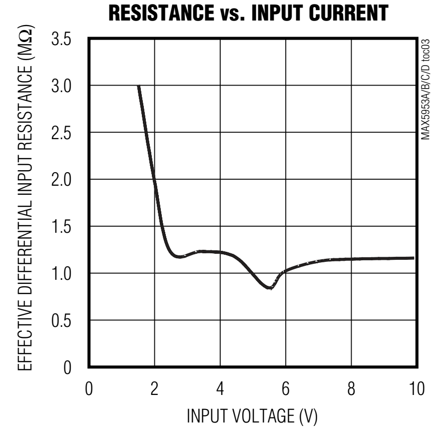
DETECTION CURRENT vs. INPUT VOLTAGE



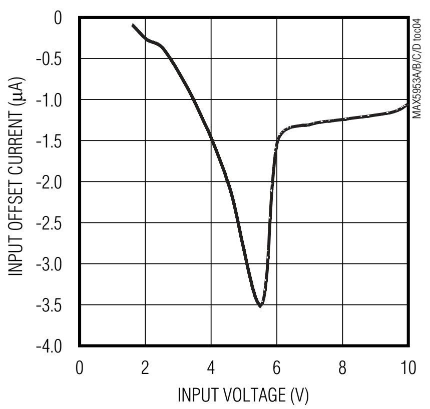
CLASSIFICATION CURRENT vs. INPUT VOLTAGE



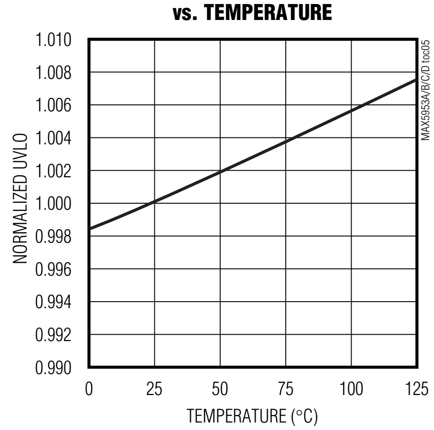
EFFECTIVE DIFFERENTIAL INPUT RESISTANCE vs. INPUT CURRENT



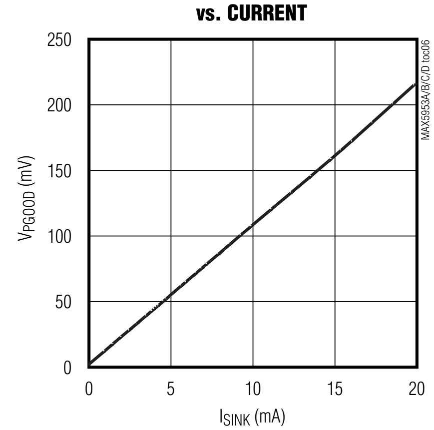
INPUT OFFSET CURRENT vs. INPUT VOLTAGE



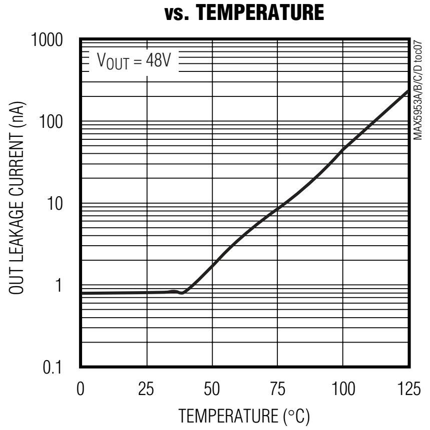
NORMALIZED UVLO vs. TEMPERATURE



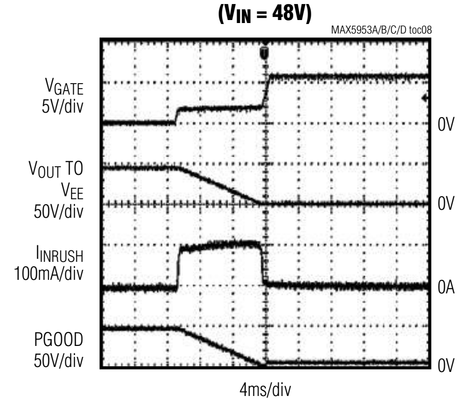
PGOOD OUTPUT LOW VOLTAGE vs. CURRENT



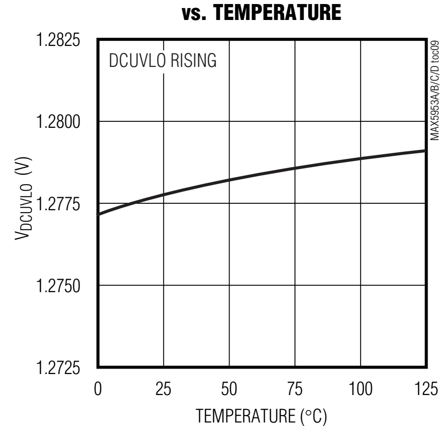
OUT LEAKAGE CURRENT vs. TEMPERATURE



INRUSH CURRENT CONTROL (V_{IN} = 48V)



DCUVLO THRESHOLD vs. TEMPERATURE

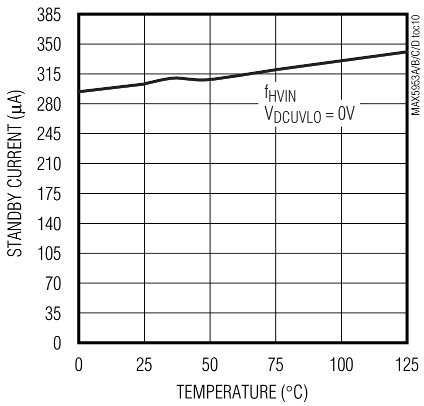


IEEE 802.3af PD Interface and PWM Controllers with Integrated Power MOSFETs

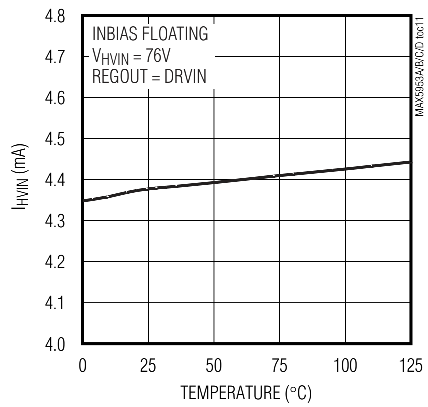
Typical Operating Characteristics (continued)

(V_{IN} = (V+ - V_{EE}) = 48V, GATE = PGOOD = unconnected, GND connected to OUT, HVIN connected to V+, UVLO = V_{EE}, C_{INBIAS} = 1µF, C_{REGOUT} = 2.2µF, R_{RTCT} = 25kΩ, C_{RTCT} = 100pF, C_{BST} = 0.22µF, T_J = 0°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C. All voltages are referenced to V_{EE}, unless otherwise noted.)

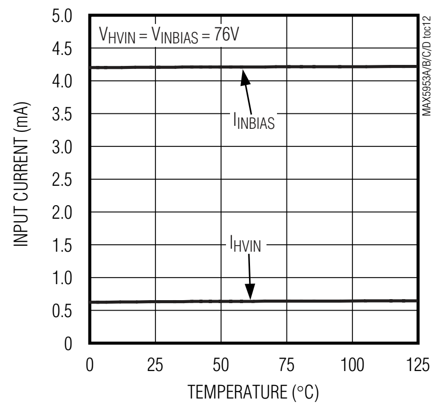
HVIN STANDBY CURRENT vs. TEMPERATURE



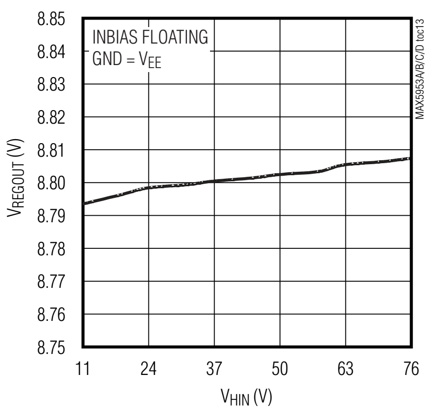
HVIN INPUT CURRENT vs. TEMPERATURE



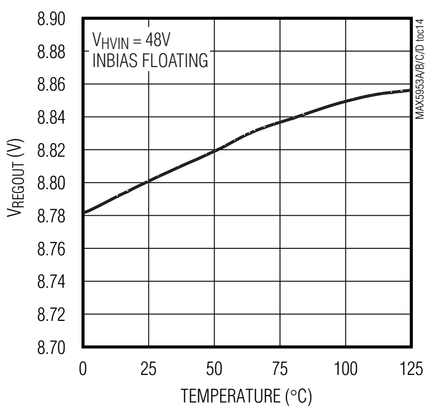
HVIN AND INBIAS INPUT CURRENT vs. TEMPERATURE



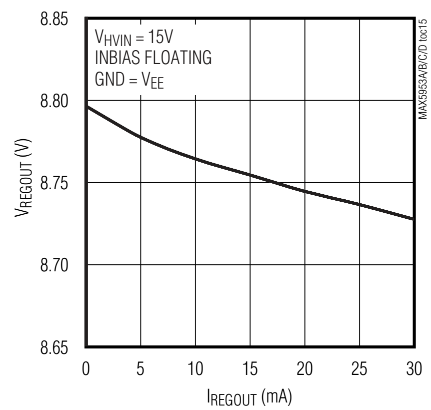
REGOUT VOLTAGE vs. INPUT VOLTAGE



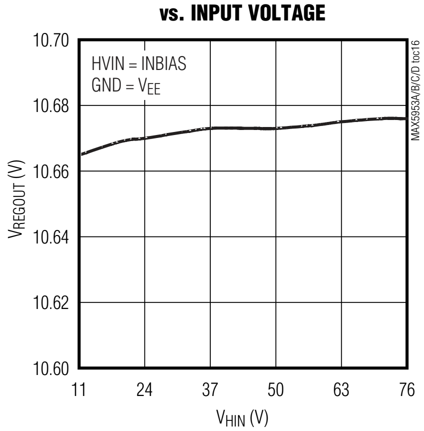
REGOUT VOLTAGE vs. TEMPERATURE



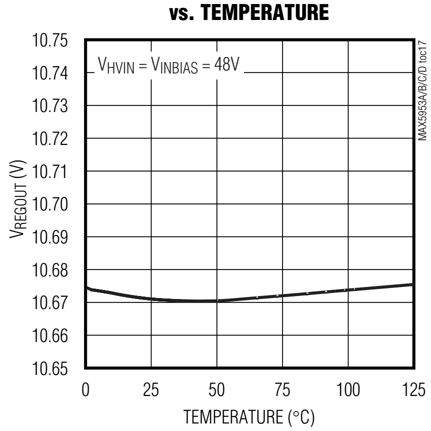
REGOUT VOLTAGE vs. LOAD CURRENT



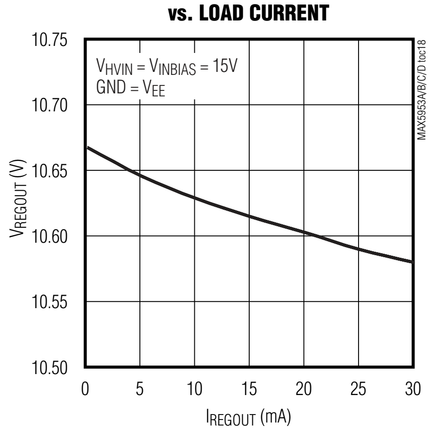
REGOUT VOLTAGE vs. INPUT VOLTAGE



REGOUT VOLTAGE vs. TEMPERATURE



REGOUT VOLTAGE vs. LOAD CURRENT

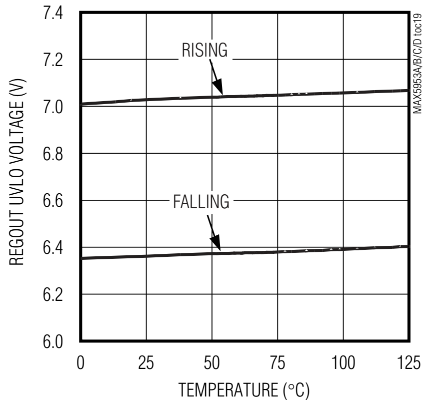


IEEE 802.3af PD Interface and PWM Controllers with Integrated Power MOSFETs

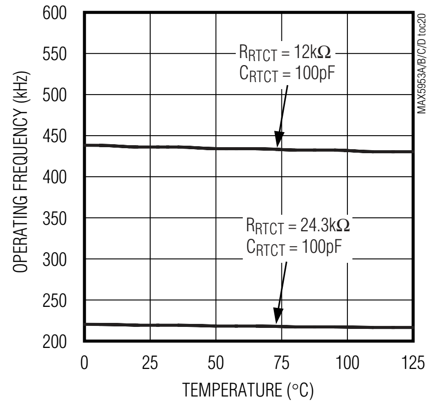
Typical Operating Characteristics (continued)

(V_{IN} = (V+ - V_{EE}) = 48V, GATE = PGOOD = unconnected, GND connected to OUT, HVIN connected to V+, UVLO = V_{EE}, C_{INBIAS} = 1µF, C_{REGOUT} = 2.2µF, R_{RTCT} = 25kΩ, C_{RTCT} = 100pF, C_{BST} = 0.22µF, T_J = 0°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C. All voltages are referenced to V_{EE}, unless otherwise noted.)

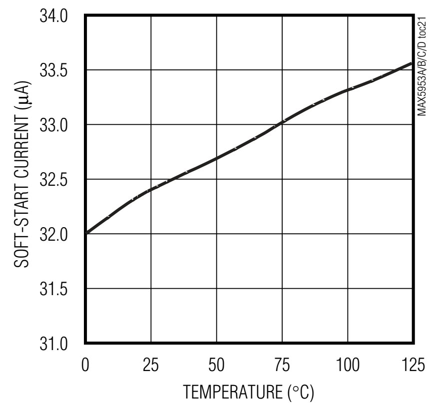
REGOUT UVLO VOLTAGE vs. TEMPERATURE



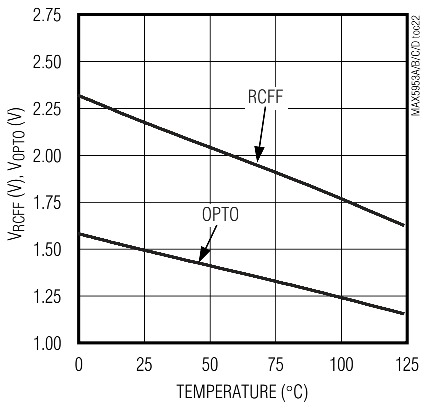
OPERATING FREQUENCY vs. TEMPERATURE



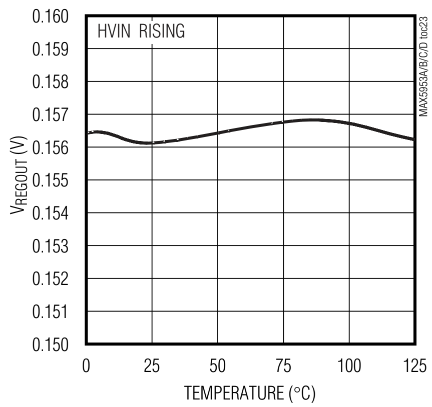
SOFT-START CURRENT vs. TEMPERATURE



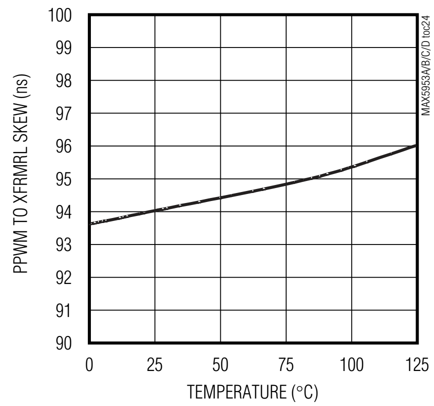
MINIMUM RCFF AND OPTO LEVELS vs. TEMPERATURE



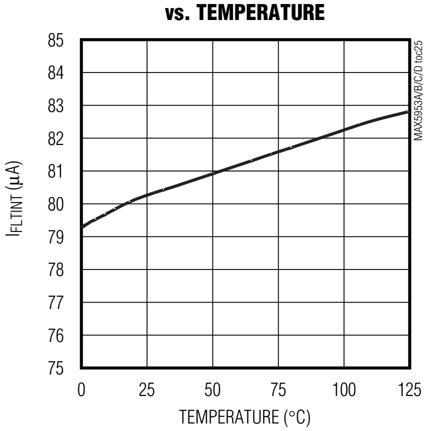
CURRENT-LIMIT COMPARATOR THRESHOLD vs. TEMPERATURE



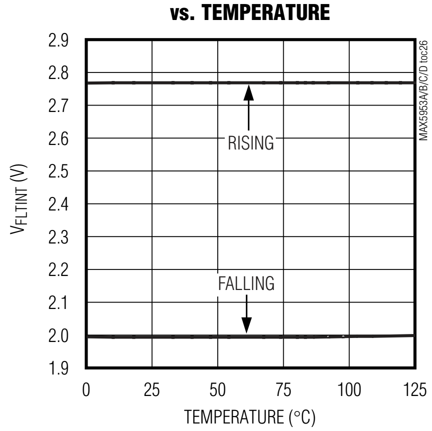
PPWM TO XFRMRL SKEW vs. TEMPERATURE



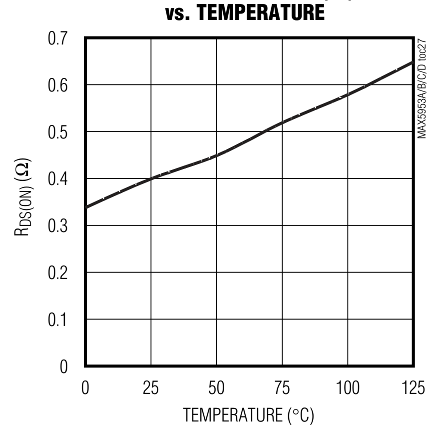
FLTINT CURRENT vs. TEMPERATURE



FLTINT SHUTDOWN VOLTAGE vs. TEMPERATURE



POWER MOSFETS $R_{DS(ON)}$ vs. TEMPERATURE



IEEE 802.3af PD Interface and PWM Controllers with Integrated Power MOSFETs

Pin Description

PIN	NAME	FUNCTION
1, 2, 3, 5, 7, 12, 13, 14, 17, 19, 35, 38, 46, 47, 48	N.C.	No Connection. Not internally connected. Make no electrical connection to these pins.
4	V+	Positive Input Power. Referenced to V_{EE}.
6 (MAX5953A/MAX5953C)	UVLO	Undervoltage Lockout Programming Input for PD Interface. UVLO is referenced to V_{EE}. When UVLO is above its threshold, the device enters the power mode. Connect UVLO to V_{EE} to use the default undervoltage lockout threshold. Connect UVLO to the center of an external resistor-divider between V+ and V_{EE} to define a threshold externally. The series resistance value of the external resistors must add to 25.5kΩ (±1%) and replaces the detection resistor. To keep the device in undervoltage lockout, drive UVLO between $V_{TH,G,UVLO}$ and $V_{REF,UVLO}$.
6 (MAX5953B/MAX5953D)	N.C.	No Connection. Not internally connected. Make no electrical connection to this pin.
8	RCLASS	Classification Setting for PD Interface. RCLASS is referenced to V_{EE}. Add a resistor from RCLASS to V_{EE} to set a PD class (see Tables 1 and 2).
9	GATE	Gate of Internal Isolation n-Channel Power MOSFET. GATE is referenced to V_{EE}. GATE sources 10µA when the device enters power mode. Connect an external 100V ceramic capacitor from GATE to OUT to program the inrush current. Drive GATE to V_{EE} to turn off the internal MOSFET. The detection and classification functions operate normally when GATE is driven to V_{EE}.
10, 11	V_{EE}	Negative Input Power. Source of the integrated isolation n-channel power MOSFET.
15, 16	OUT	Output Voltage. OUT is referenced to V_{EE}. OUT is connected to the drain of the integrated isolation n-channel power MOSFET. Connect OUT to GND.
18 (MAX5953A/MAX5953B)	PGOOD	Active-High, Open-Drain Power-Good Indicator Output for PD Interface. PGOOD is referenced to OUT. PGOOD goes high impedance when V_{OUT} is within 1.2V of V_{EE} and when V_{GATE} is 5V above V_{EE}. Otherwise, PGOOD is internally pulled to OUT (given that V_{OUT} is at least 5V below V+). PGOOD can be connected directly to CSS or DCUVLO to enable/disable the DC-DC converter.
18 (MAX5953C/MAX5953D)	$\overline{PGOOD}$	Active-Low, Open-Drain Power-Good Indicator Output for PD Interface. $\overline{PGOOD}$ is referenced to V_{EE}. $\overline{PGOOD}$ is pulled to V_{EE} when V_{OUT} is within 1.2V of V_{EE} and when V_{GATE} is 5V above V_{EE}. Otherwise, $\overline{PGOOD}$ goes high impedance.
20	CS	Current-Sense Input for PWM Controller. CS is referenced to PGND. The current-limit threshold is internally set to 156mV relative to PGND. The device has an internal noise filter. If necessary, connect an external RC filter from CS to PGND for additional filtering.
21	PPWM	PWM Pulse Output. Referenced to GND. PPWM leads the internal power MOSFET pulse by approximately 100ns.
22	GND	Signal Ground of PWM Controller. Connect GND to PGND.
23	PGND	Power Ground of the DC-DC Converter Power Stage. Connect PGND to GND.
24	CSS	Soft-Start Timing Capacitor Connection for PWM Controller. CSS is referenced to GND. Connect a 0.01µF or greater ceramic capacitor from CSS to GND. Connect to PGOOD to automatically enable the PWM controller from the PD interface.

Pin Description (continued)

PIN	NAME	FUNCTION
25	OPTO	PWM Comparator Inverting Input. OPTO is referenced to GND. Connect the collector of the optotransistor to OPTO and a pullup resistor to REGOUT.
26, 27	SRC	Source Connection of Low-Side Power MOSFET in the Two-Switch Power Stage of the DC-DC Converter. Connect SRC to PGND with a low-value resistor for current limiting.
28, 29	XFRMRL	Low-Side Connection for the Isolation Transformer. Drain terminal of low-side power MOSFET in the two-switch power stage of the DC-DC converter.
30	DRVIN	Supply Input for the Gate-Driver of Internal Power MOSFETs. DRVIN is referenced to PGND. Bypass DRVIN with at least 0.1µF to PGND. Connect DRVIN to REGOUT.
31, 32	XFRMRH	High-Side Connection for the Isolation Transformer. Source connection of high-side power MOSFET in the two-switch power stage of the DC-DC converter.
33, 34	DRNH	Drain Connection of High-Side MOSFET in the Two-Switch Power Stage of the DC-DC Converter. Connect DRNH to the most positive rail of the input supply. Bypass DRNH appropriately to handle the heavy switching current through the transformer.
36	BST	Boost Input for the DC-DC Converter. BST is the boost connection point for the high-side MOSFET driver. Connect a minimum 0.1µF capacitor from BST to XFRMRH with short and wide PC board traces.
37	DCUVLO	DC-DC Converter Undervoltage Lockout Input. DCUVLO is referenced to GND. Connect a resistor-divider from HVIN to DCUVLO to GND to set the UVLO threshold.
39	HVIN	DC-DC Converter Positive Input Power Supply. HVIN is referenced to GND. Connect HVIN to V+.
40	INBIAS	Input from the Rectified Bias Winding to the DC-DC Converter. INBIAS is referenced to GND. INBIAS is the input to the internal linear voltage regulator (REGOUT).
41	REGOUT	Internal Regulator Output. REGOUT is used for the DC-DC converter gate driver. REGOUT is referenced to GND. V_{REGOUT} is always present as long as HVIN is powered with a voltage above the DCUVLO threshold. Bypass REGOUT to GND with a minimum 2.2µF ceramic capacitor.
42	RTCT	Oscillator Frequency Set Input for the PWM Controller. RTCT is referenced to GND. Connect a resistor from RTCT to REGOUT and a ceramic capacitor from RTCT to GND to set the oscillator frequency.
43	FLTINT	Fault Integration Input for PWM Controller. FLTINT is referenced to GND. During persistent current-limit faults, a capacitor connected to FLTINT is charged with an internal 80µA current source. Switching is terminated when V_{FLTINT} reaches 2.7V. An external resistor connected in parallel discharges the capacitor. Switching resumes when V_{FLTINT} drops to 1.9V.
44	RCFF	Feed-Forward Input for PWM Controller. RCFF is referenced to GND. To generate the PWM ramp, connect a resistor from RCFF to HVIN and a capacitor from RCFF to GND.
45	RAMP	Ramp Sense Input for PWM Controller. Connect RAMP to RCFF.
—	EP	Exposed Paddle. EP is internally unconnected and must be connected to V_{EE} externally. To improve power dissipation, solder the exposed paddle to a copper pad on the PC board.

Typical Application Circuit

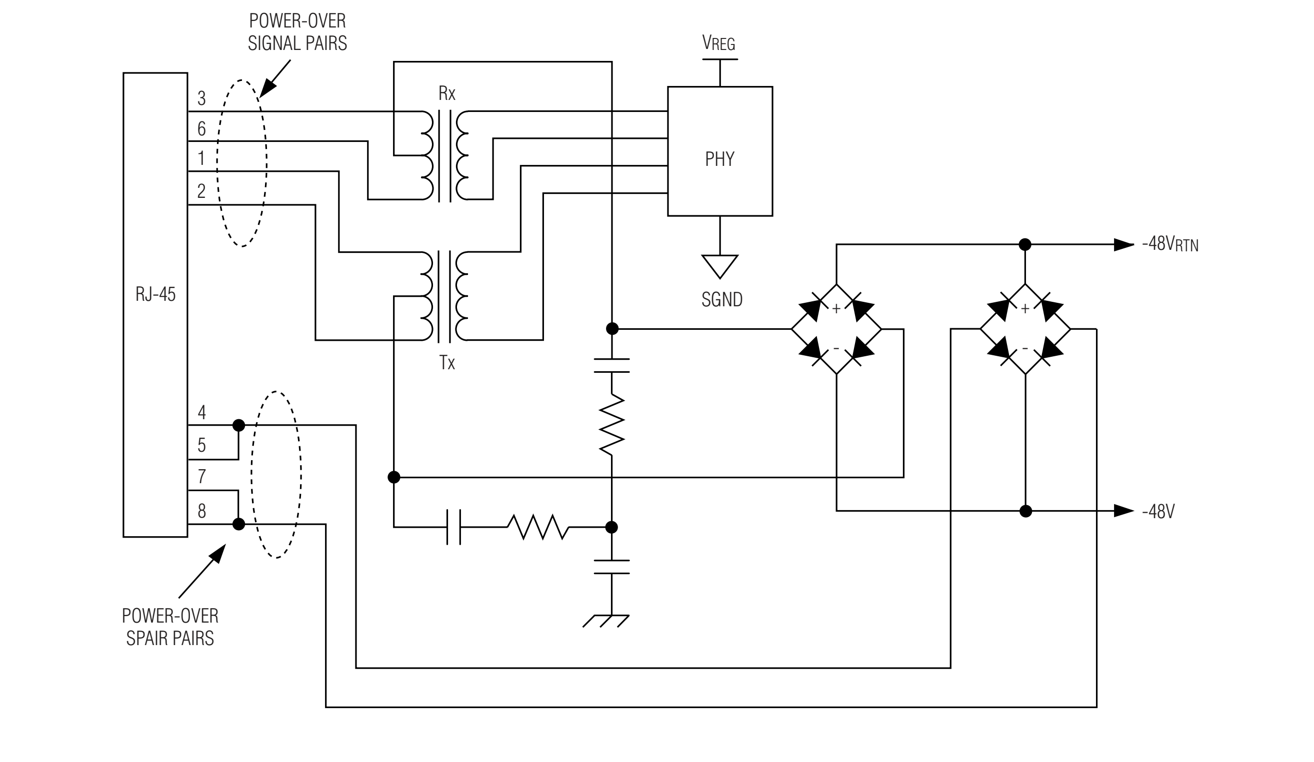


Figure 2. RJ-45 Connector, PoE Magnetic, and Input Diode Bridges

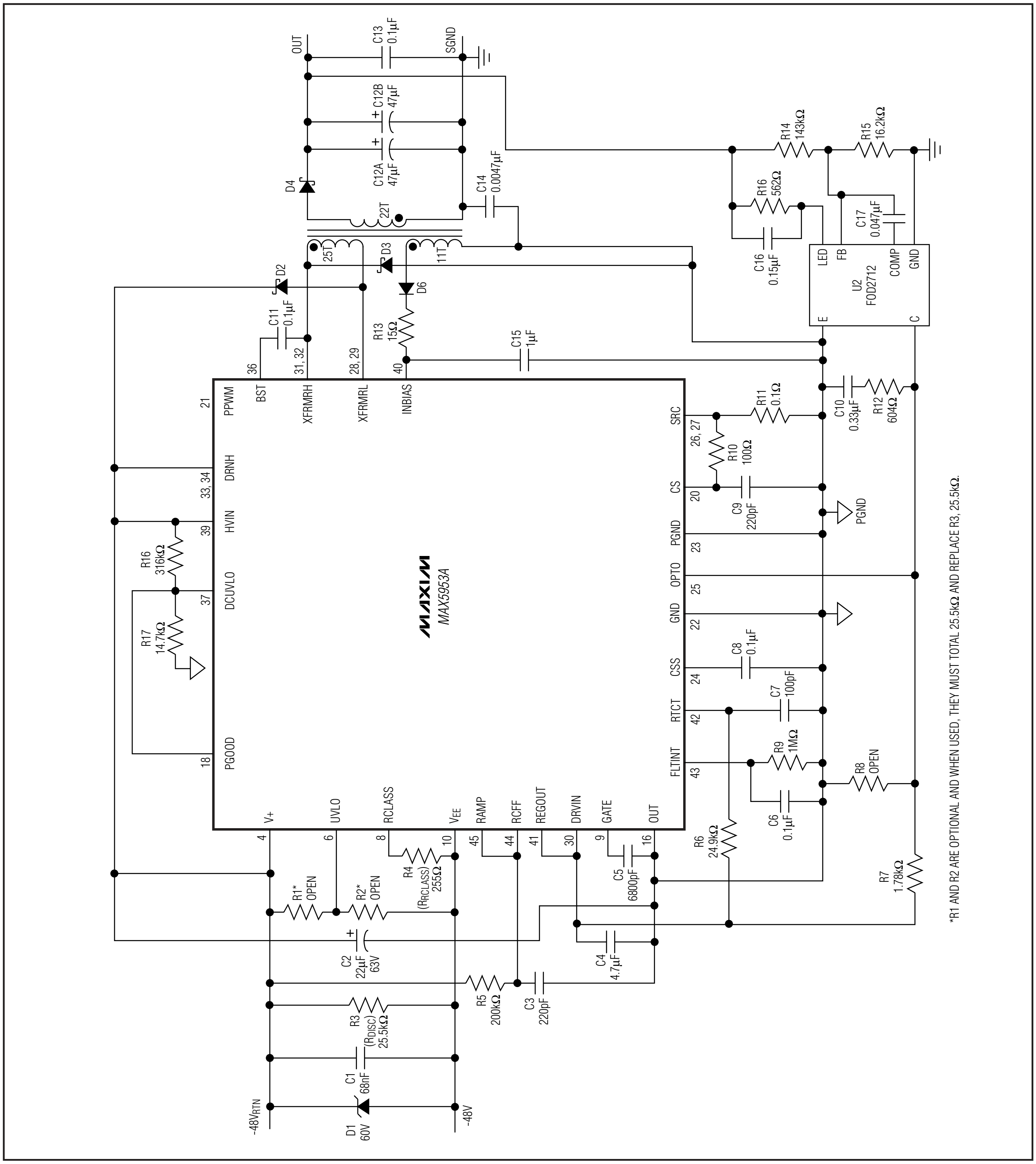


Figure 3. Typical Application Circuit

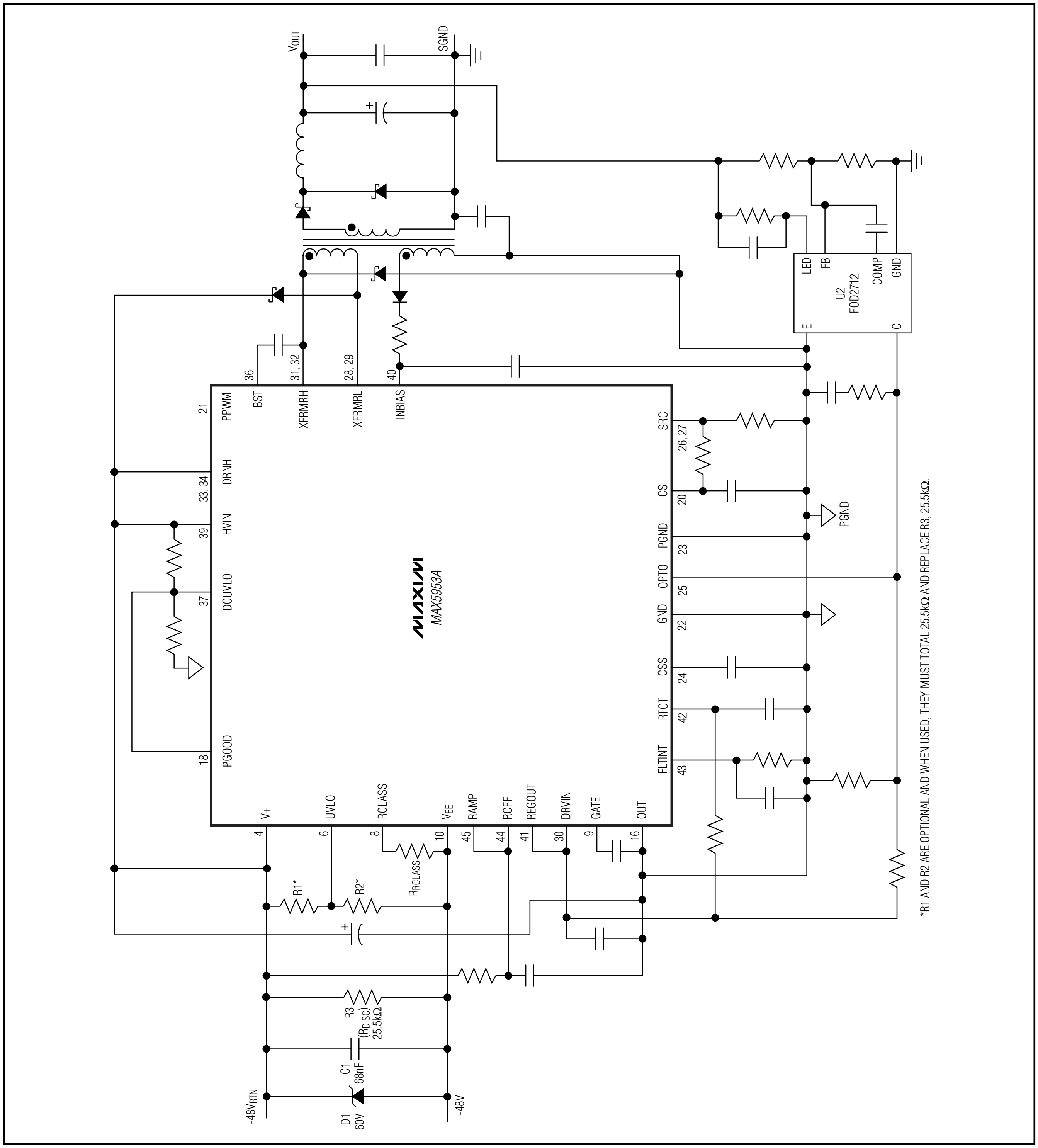


Figure 4. For higher power applications, the MAX5953A/MAX5953B/MAX5953C/MAX5953D can be used in a two-switch forward converter configuration

Detailed Description

PD Interface

The MAX5953A/MAX5953B/MAX5953C/MAX5953D include complete interface function for a PD to comply with the IEEE 802.3af standard in a PoE system. They provide the PD with a detection signature, a classification signature, and an integrated isolation switch with programmable inrush current control. An integrated MOSFET provides PD isolation during detection and classification. All devices guarantee a leakage current offset of less than 10µA during the detection phase. A programmable current limit prevents high inrush current during power-on. The device features power-mode UVLO with wide hysteresis and long deglitch time to compensate for twisted-pair-cable resistive drop and to assure glitch-free transition between detection, classification, and power-on/-off phases. The MAX5953A/MAX5953C have an adjustable UVLO threshold with the default value compliant to the 802.3af standard, while the MAX5953B/MAX5953D have a lower and fixed UVLO threshold compatible with some legacy pre-802.3af PSE.

Table 1. PD Power Classification/ R_{RCLASS} Selection

CLASS	USAGE	R_{RCLASS} (Ω)	MAXIMUM POWER USED BY PD (W)
0	Default	10k	0.44 to 12.95
1	Optional	732	0.44 to 3.84
2	Optional	392	3.84 to 6.49
3	Optional	255	6.49 to 12.95
4	Not Allowed	178	Reserved*

Class 4 reserved for future use.

Operating Modes

Depending on the input voltage ($V_{IN} = V_+ - V_{EE}$), the PD front-end section of the MAX5953A/MAX5953B/MAX5953C/MAX5953D operate in three different modes: PD detection signature, PD classification, and PD power. All voltage thresholds are designed to operate with or without the optional diode bridge while still complying with the IEEE 802.3af standard (see Figure 2).

Detection Mode (1.4V ≤ V_{IN} ≤ 10.1V)

In detection mode, the power source equipment (PSE) applies two voltages on V_{IN} in the range of 1.4V to 10.1V (1V step minimum), and records the corresponding current measurements at those two points. The PSE then computes $\Delta V/\Delta I$ to ensure the presence of the 25.5kΩ signature resistor. In this mode, most interface circuitry of the MAX5953A/MAX5953B/MAX5953C/MAX5953D is off and the offset current is less than 10µA.

Classification Mode (12.6V ≤ V_{IN} ≤ 20V)

In the classification mode, the PSE classifies the PD based on the power consumption required by the PD. This allows the PSE to efficiently manage power distribution. The IEEE 802.3af standard defines five different classes as shown in Table 1. An external resistor (R_{RCLASS}) connected from RCLASS to V_{EE} sets the classification current.

The PSE determines the class of a PD by applying a voltage at the PD input and measuring the current sourced out of the PSE. When the PSE applies a voltage between 12.6V and 20V, the IC exhibits a current characteristic with values indicated in Table 2. The PSE uses the classification current information to classify the power requirement of the PD. The classification current includes the current drawn by the 25.5kΩ detection signature resistor and the supply current of the IC so the total current drawn by the PD is within the IEEE 802.3af standard figures. The classification current is turned off whenever the device is in power mode.

Table 2. Setting Classification Current

CLASS	R_{RCLASS} (Ω)	V_{IN}* (V)	CLASS CURRENT SEEN AT V_{IN} (mA)		IEEE 802.3af PD CLASSIFICATION CURRENT SPECIFICATION (mA)	
			MIN	MAX	MIN	MAX
0	10k	12.6 to 20	0	2.00	0	4
1	732	12.6 to 20	9.17	11.83	9	12
2	392	12.6 to 20	17.29	19.71	17	20
3	255	12.6 to 20	26.45	29.55	26	30
4	178	12.6 to 20	36.60	41.40	36	44

V_{IN} is measured across the MAX5953A/MAX5953B/MAX5953C/MAX5953D input pins ($V_+ - V_{EE}$), which do not include the diode bridge voltage drop.

Power Mode

During power mode, when V_{IN} rises above the undervoltage lockout threshold ($V_{UVLO,ON}$), the IC gradually turns on the internal n-channel MOSFET Q1 (see Figure 8). The IC charges the gate of Q1 with a constant current source (10µA, typ). The drain-to-gate capacitance of Q1 limits the voltage rise rate at the drain of the MOSFET, thereby limiting the inrush current. To further reduce the inrush current, add external drain-to-gate capacitance (see the *Inrush Current Limit* section). When the drain of Q1 is within 1.2V of its source voltage and its gate-to-source voltage is above 5V, the MAX5953A/MAX5953B assert the PGOOD output (MAX5953C/MAX5953D assert the $\overline{\text{PGOOD}}$ output). The IC has a wide UVLO hysteresis and turn-off deglitch time to compensate for the high impedance of the twisted-pair cable.

Undervoltage Lockout for PD Interface

The IC operates up to a 67V supply voltage with a default UVLO turn-on ($V_{UVLO,ON}$) set at 38.6V (MAX5953A/MAX5953C) or 35.4V (MAX5953B/MAX5953D) and a UVLO turn-off ($V_{UVLO,OFF}$) set at 30V. The MAX5953A/MAX5953C have an adjustable UVLO threshold using a resistor-divider connected to UVLO (see Figure 3). When the input voltage goes below the UVLO threshold for more than t_{OFF_DLY}, the MOSFET turns off.

To adjust the UVLO threshold, connect an external resistor-divider from V+ to UVLO to V_{EE}. Use the following equations to calculate R1 and R2 for a desired UVLO threshold:

$$R2 = 25.5k\Omega \times \frac{V_{REF,UVLO}}{V_{IN,EX}}$$

$$R1 = 25.5k\Omega - R2$$

where $V_{IN,EX}$ is the desired UVLO threshold. Since the resistor-divider replaces the 25.5kΩ PD detection resistor, ensure that the sum of R1 and R2 equals 25.5kΩ ±1%. When using the external resistor-divider, MAX5953A/MAX5953C have an external reference voltage hysteresis of 20% (typ). In other words, when UVLO is programmed externally, the turn-off threshold is 80% (typ) of the new UVLO threshold.

Inrush Current Limit

The IC charges the gate of the internal MOSFET with a constant current source (10µA, typ). The drain-to-gate capacitance of the MOSFET limits the voltage rise rate at the drain, thereby limiting the inrush current. Add an external capacitor from GATE to OUT to further reduce the inrush current. Use the following equation to calculate the inrush current:

$$I_{INRUSH} = I_G \times \frac{C_{OUT}}{C_{GATE}}$$

The recommended typical inrush current for a PoE application is 100mA.

PGOOD/$\overline{\text{PGOOD}}$ Output

PGOOD is an open-drain, active-high logic output. PGOOD goes high impedance when V_{OUT} is within 1.2V of V_{EE} and when GATE is 5V above V_{EE}. Otherwise, PGOOD is pulled to V_{OUT} (given that V_{OUT} is at least 5V below V+). Connect PGOOD directly to CSS to enable/disable the DC-DC converter. $\overline{\text{PGOOD}}$ is an open-drain, active-low logic output. $\overline{\text{PGOOD}}$ is pulled to V_{EE} when V_{OUT} is within 1.2V of V_{EE} and when GATE is 5V above V_{EE}. Otherwise, $\overline{\text{PGOOD}}$ goes high impedance. Connect a 100kΩ pullup resistor from $\overline{\text{PGOOD}}$ to V+ if needed.

Thermal Dissipation

Thermal shutdown limits total power dissipation in the IC. If the junction temperature exceeds +160°C, thermal shutdown is enabled to turn off the MAX5953A/MAX5953B/MAX5953C/MAX5953D, allowing the IC to cool. The IC turns on after the junction temperature cools by 20°C.

DC-DC Converter

The MAX5953A/MAX5953B/MAX5953C/MAX5953D isolated PWM power ICs feature integrated switching power MOSFETs connected in a voltage-clamped, two-transistor, power-circuit configuration. These devices can be used in both forward and flyback configurations with a wide 11V to 76V input voltage range. The voltage-clamped power topology enables full recovery of stored magnetizing and leakage inductive energy for enhanced efficiency and reliability. A look-ahead signal for driving secondary-side synchronous rectifiers can be used to increase efficiency. A wide array of protection features include UVLO, overtemperature shutdown, and short-circuit protection with hiccup current-limit for enhanced performance and reliability. Operation up to 500kHz allows smaller external magnetics and capacitors.

Power Topology

The two-switch forward-converter topology offers outstanding robustness against faults and transformer saturation while affording efficient use of 0.4Ω power MOSFETs. Voltage-mode control with feed-forward compensation allows the rejection of input supply disturbances within a single cycle similar to that of current-mode controlled topologies.

The two-switch power topology recovers energy stored in both the magnetizing and the parasitic leakage inductances of the transformer. The *Typical Application Circuit*, Figure 3, shows the schematic diagram of a -48V input flyback converter using the MAX5953A. Figure 4 shows the schematic diagram of a -48V input forward converter and a 5V, 3A output isolated power supply.

Voltage-Mode Control and the PWM Ramp

For voltage-mode control, the feed-forward PWM ramp is generated at RCFF. From RCFF, connect a capacitor to GND and a resistor to HVIN. The ramp generated is applied to the noninverting input of the PWM comparator at RAMP and has a minimum voltage of approximately 2V. The slope of the ramp is determined by the voltage at HVIN and affects the overall loop gain. The ramp peak must remain below the 5.5V dynamic range of RCFF. Assuming the maximum duty cycle approaches 50% at a minimum input voltage (PWM UVLO turn-on threshold), use the following formula to calculate the minimum value of either the ramp capacitor or resistor:

$$R_{RCFF} \times C_{RCFF} \geq \frac{V_{IN,EX}}{2 \times f_S \times V_{R(P-P)}}$$

where f_S is the switching frequency, $V_{R(P-P)}$ is the peak-to-peak ramp voltage (2V, typ). Select R_{RCFF} resistance value between 200kΩ and 600kΩ.

Maximize the signal-to-noise ratio by setting the ramp peak as high as possible. Calculate the low-frequency, small-signal gain of the power stage (the gain from the inverting input of the PWM comparator to the output) using the following formula:

$$G_{PS} = N_{SP} \times R_{RCFF} \times C_{RCFF} \times f_S$$

where N_{SP} is the secondary to primary power transformer turns ratio.

Secondary-Side Synchronization

The MAX5953A/MAX5953B/MAX5953C/MAX5953D provide convenient synchronization for optional secondary-side synchronous rectifiers. Figure 5 shows the connection diagram with a high-speed optocoupler. Choose an optocoupler with a propagation delay of less than 80ns. The synchronizing pulse is generated approximately 110ns ahead of the main pulse that drives the two power MOSFETs.

Undervoltage Lockout for DC-DC Converter

Connect PGOOD to DCUVLO to ensure the PD interface is ready prior to the DC-DC converter. The DCUVLO block monitors the input voltage at HVIN through an external resistive divider (R16 and R17) connected to DCUVLO (see Figure 3). Use the following equation to calculate R16 and R17:

$$V_{DCUVLOIN} = V_{DCUVLO} \times \left(1 + \frac{R16}{R17}\right)$$

where $V_{DCUVLOIN}$ is the desired input voltage lockout level and V_{DCUVLO} is the undervoltage lockout threshold (1.25V, typ). Select the R17 resistance value between 100kΩ and 500kΩ.

Optocoupled Feedback

Isolated voltage feedback is achieved by using an optocoupler as shown in Figure 3. Connect the collector of the optotransistor to OPTO and a pullup resistor between OPTO and REGOUT.

Internal Regulators

As soon as power is provided to HVIN, internal power supplies power the DCUVLO detection circuitry. REGOUT is used to drive the internal power MOSFETs. Bypass REGOUT to GND with a minimum 2.2µF ceramic capacitor. The HVIN LDO steps down V_{HVIN} to a nominal output voltage (V_{REGOUT}) of 8.75V. A second parallel LDO powers REGOUT from INBIAS. A tertiary winding connected through a diode to INBIAS powers up REGOUT once switching commences. This powers REGOUT to 10.5V (typ) and shuts off the current flowing from HVIN to REGOUT. This results in a lower on-chip power dissipation and higher efficiency.

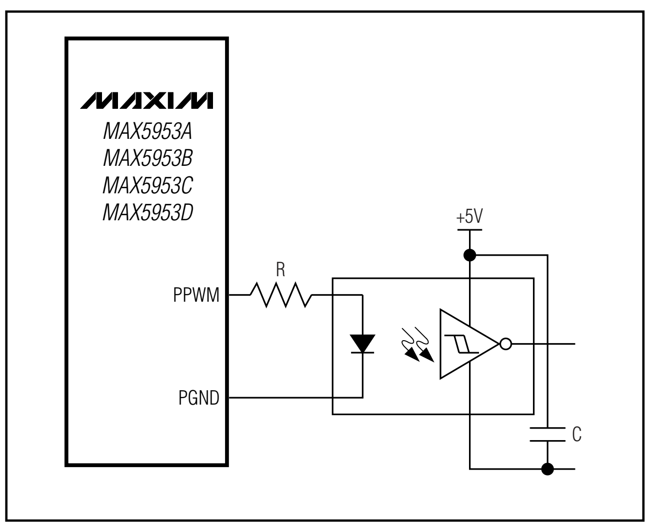


Figure 5. Secondary-Side Synchronous Rectifier Driver Using a High-Speed Optocoupler

IEEE 802.3af PD Interface and PWM Controllers with Integrated Power MOSFETs

Soft-Start

Program the MAX5953A/MAX5953B/MAX5953C/MAX5953D soft-start with an external capacitor (C_{CSS}) connected between CSS and GND. When the device turns on, C_{CSS} charges with a constant current of 33µA, ramping up to 7.3V. During this time, the feedback input (OPTO) is clamped to V_{CSS} + 0.6V. This initially holds the duty cycle lower than the value the regulator imposes, thus preventing voltage overshoot at the output. When the IC turns off, the soft-start capacitor internally discharges to GND.

Oscillator

The oscillator is externally programmable through a resistor connected from RTCT to REGOUT and a capacitor connected from RTCT to GND. The PWM frequency is one-half the frequency seen at RTCT with a 50% duty cycle. Use the following formula to calculate the oscillator components:

$$R_{RTCT} \cong \frac{1}{2f_S(C_{RTCT} + C_{PCB})\ln\left(\frac{V_{REGOUT}}{V_{REGOUT} - V_{TH,RTCT}}\right)}$$

where C_{PCB} is the stray capacitance on the PC board (14pF, typ), $V_{TH,RTCT}$ is the RTCT peak trip level, and f_S is the switching frequency.

Integrating Fault Protection

The integrating fault protection feature allows the IC to ignore transient overcurrent conditions for a programmable amount of time, giving the power-supply time to behave like a current source to the load. This can happen, for example, under load-current transients when the control loop requests maximum current to keep the output voltage from going out of regulation. The ignore time is programmed externally by connecting a capacitor from FLTINT to GND. Under sustained overcurrent faults, the voltage across this capacitor ramps up toward the FLTINT shutdown threshold (2.7V, typ). When V_{FLTINT} reaches the shutdown threshold, the power supply shuts down. A high-value bleed resistor connected in parallel with the FLTINT capacitor allows the capacitor to discharge toward the restart threshold (1.9V, typ). FLTINT drops to the restart threshold allowing for soft-starting the supply again.

The fault integration circuit works by forcing an 80µA current into FLTINT for one clock cycle every time the current-limit comparator ILIM (Figure 9) trips. Use the following formula to calculate the approximate capacitor needed for the desired shutdown time:

$$C_{FLTINT} \cong \frac{I_{FLTINT} \times t_{SH}}{1.4}$$

where I_{FLTINT} is typically 80µA, and t_{SH} is the desired ignore time during which current-limit events from the current-limit comparator are ignored.

This is an approximate formula; some testing may be required to fine tune the actual value of the capacitor.

Calculate the approximate bleed resistor needed for the desired recovery time using the following formula:

$$R_{FLTINT} \cong \frac{t_{RT}}{C_{FLTINT} \times 0.3514}$$

where t_{RT} is the desired recovery time.

Choose $t_{RT} \geq 10 \times t_{SH}$. Typical values for t_{SH} can range from a few hundred microseconds to a few milliseconds.

Shutdown

Shut down the controller section of the IC by driving DCUVLO to GND using an open-collector or open-drain transistor connected to GND. The DC-DC converter section shuts down if REGOUT is below its DCUVLO level.

Current-Sense Comparator

The current-sense (CS) comparator and its associated logic limit the peak current through the internal MOSFET. Current is sensed at CS as a voltage across a sense resistor between the source of the MOSFET and GND. The power MOSFET switches off when the voltage at CS reaches 156mV. Select the current-sense resistor, R_{SENSE}, according to the following equation:

$$R_{SENSE} = 0.156V / I_{LimPrimary}$$

where $I_{LimPrimary}$ is the maximum peak primary-side current.

To reduce switching noise, connect CS to an external RC lowpass filter for additional filtering (Figure 3).

Applications Information

Design Example

Design Example 1: PD with three-output flyback DC-DC converter

Figure 6 shows an isolated three-output flyback DC-DC converter. It provides output voltages of 10V at 30mA, 5.1V at 1.8A, and 2.55V at 5.4A.

Design Example 2: PD with nonisolated step-down (buck) converter

Figure 7 shows a buck converter with 12V, 0.75A output. **Caution:** this converter does not have active current limit.

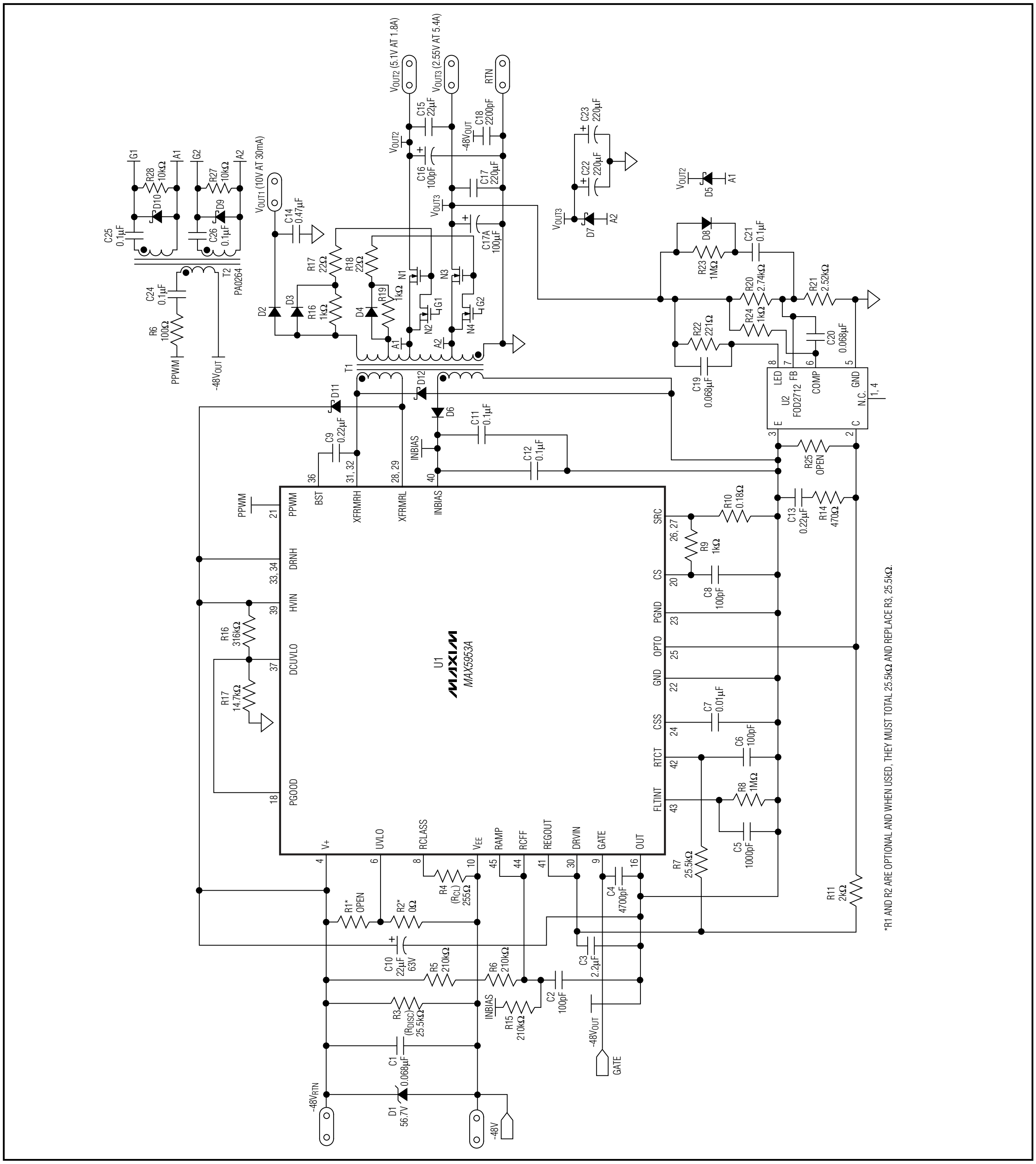


Figure 6. PD with Three-Output Flyback DC-DC Converter

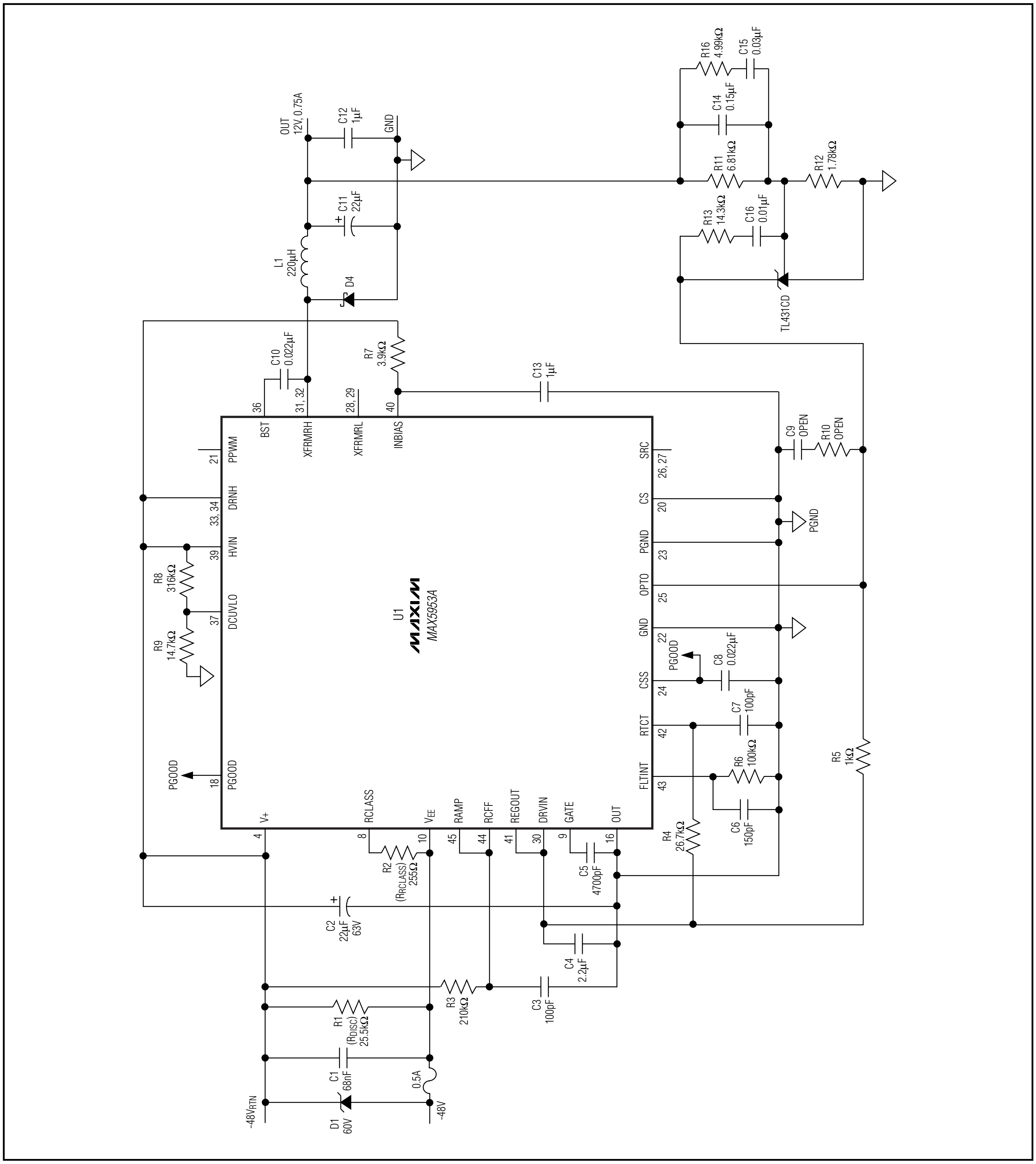


Figure 7. PD with Nonisolated Step-Down (Buck) Converter

Table 3. Component Suppliers

COMPONENT	SUPPLIERS	WEBSITE
Power FETS	International Rectifier	www.irf.com
	Fairchild	www.fairchildsemi.com
	Vishay-Siliconix	www.vishay.com/brands/siliconix/main.html
Current-Sense Resistors	Dale-Vishay	www.vishay.com/brands/dale/main.html
	IRC	www.irctt.com/pages/index.cfm
Diodes	ON Semi	www.onsemi.com
	General Semiconductor	www.gensemi.com
	Central Semiconductor	www.centralsemi.com
Capacitors	Sanyo	www.sanyo.com
	Taiyo Yuden	www.t-yuden.com
	AVX	www.avxcorp.com
Magnetics	Coiltronics	www.cooperet.com
	Coilcraft	www.coilcraft.com
	Pulse Engineering	www.pulseeng.com

Layout Recommendations

All connections carrying pulsed currents must be very short, as wide as possible, and have a ground plane as a return path. The inductance of these connections must be kept to a minimum due to the high di/dt of the currents in high-frequency-switching power converters.

Current loops must be analyzed in any layout proposed, and the internal area kept to a minimum to reduce radiated EMI. Ground planes must be kept as intact as possible.

Block Diagrams

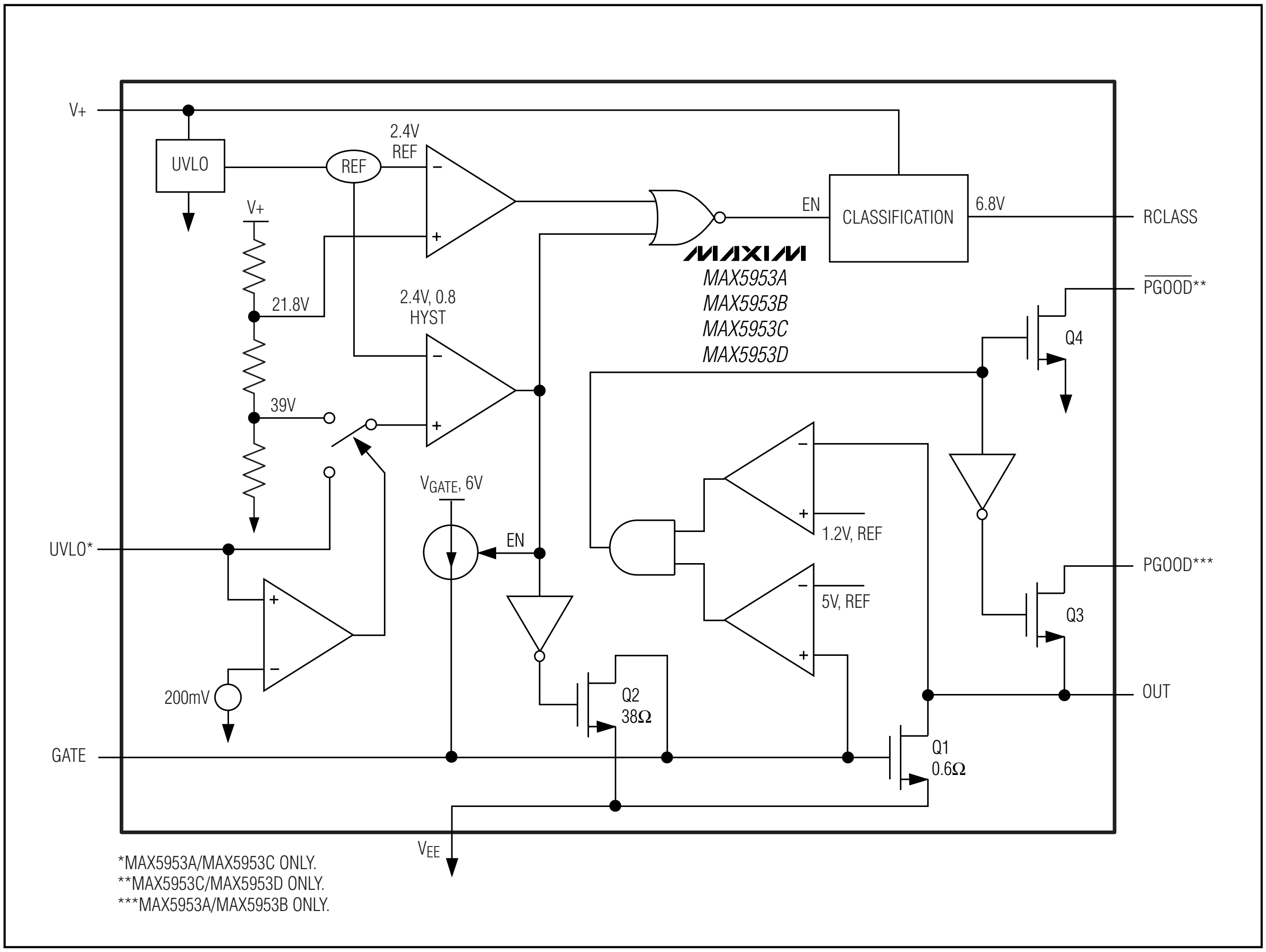


Figure 8. Powered Device Interface Block Diagram

Block Diagrams (continued)

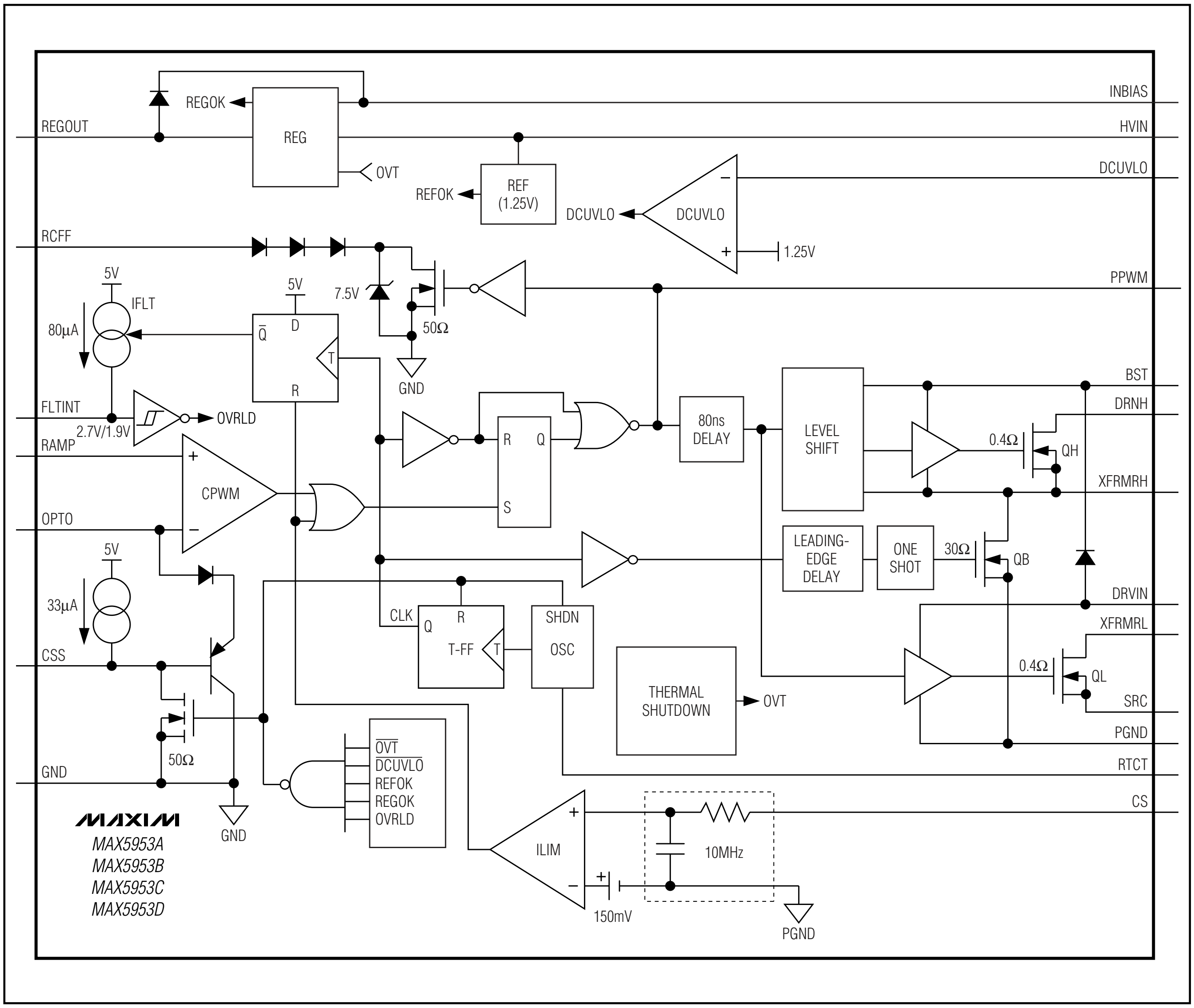
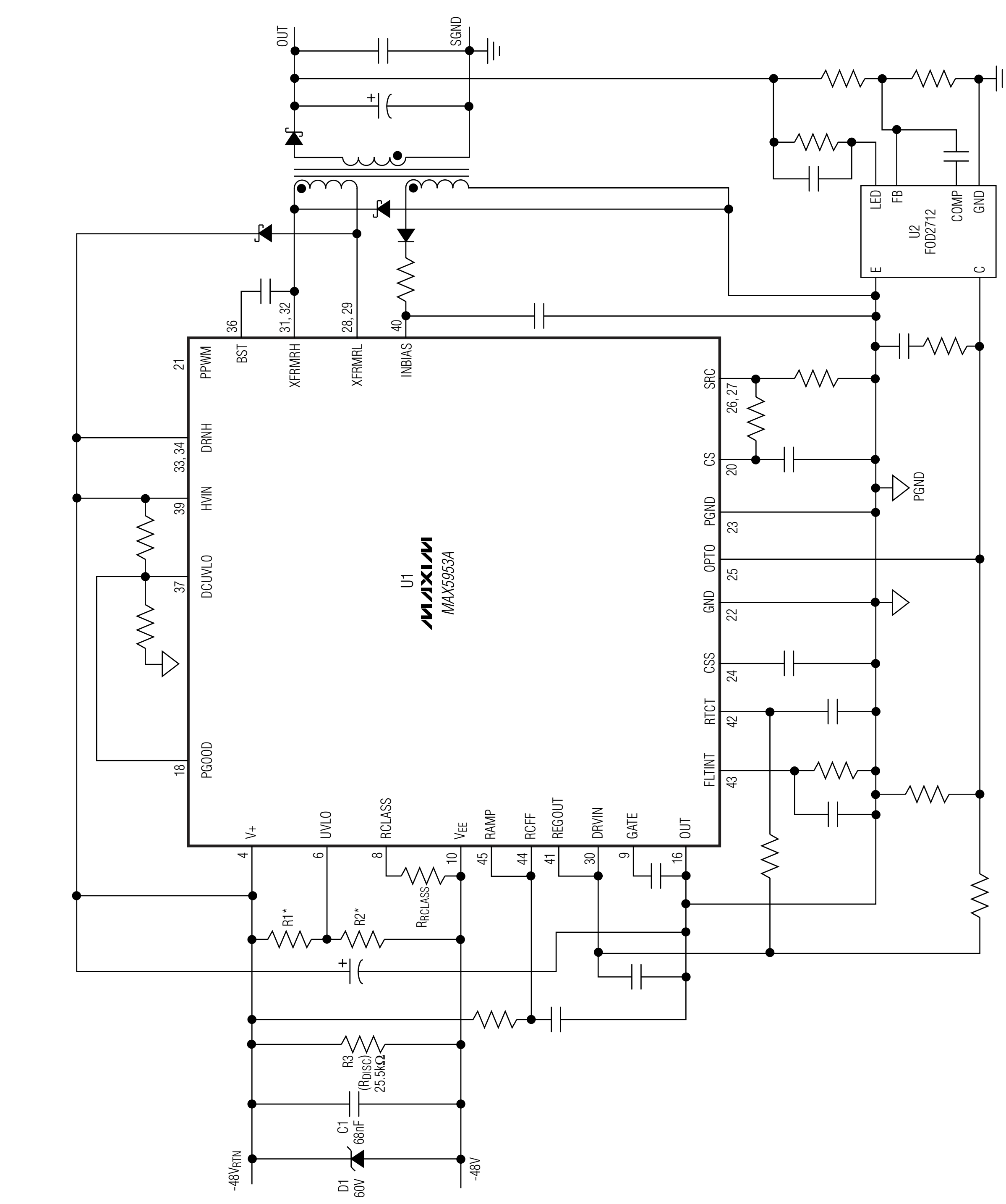


Figure 9. DC-DC Converter Block Diagram (Voltage-Mode PWM Controller and Two-Switch Power Stage)

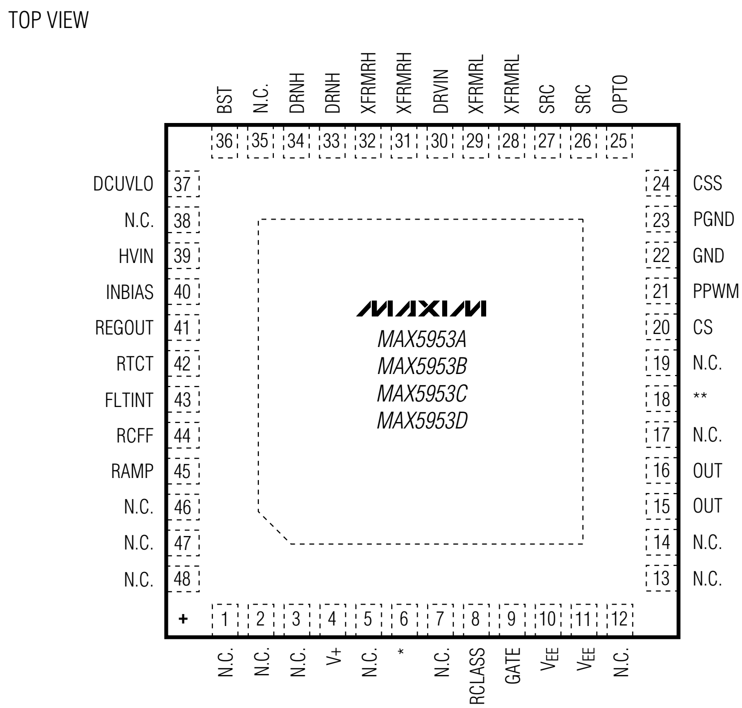
IEEE 802.3af PD Interface and PWM Controllers with Integrated Power MOSFETs

Typical Operating Circuit



*R1 AND R2 ARE OPTIONAL AND WHEN USED, THEY MUST TOTAL 25.5kΩ AND REPLACE R3, 25.5kΩ.

Pin Configuration



THIN QFN
7mm x 7mm

*UVLO FOR MAX5953A/MAX5953C
N.C. FOR MAX5953B/MAX5953D
** PGOOD FOR MAX5953A/MAX5953B
$\overline{\text{PGOOD}}$ FOR MAX5953C/MAX5953D

Selector Guide

PART	PGOOD or $\overline{\text{PGOOD}}$	UVLO
MAX5953A	PGOOD	Adjustable
MAX5953B	PGOOD	Fixed
MAX5953C	$\overline{\text{PGOOD}}$	Adjustable
MAX5953D	$\overline{\text{PGOOD}}$	Fixed

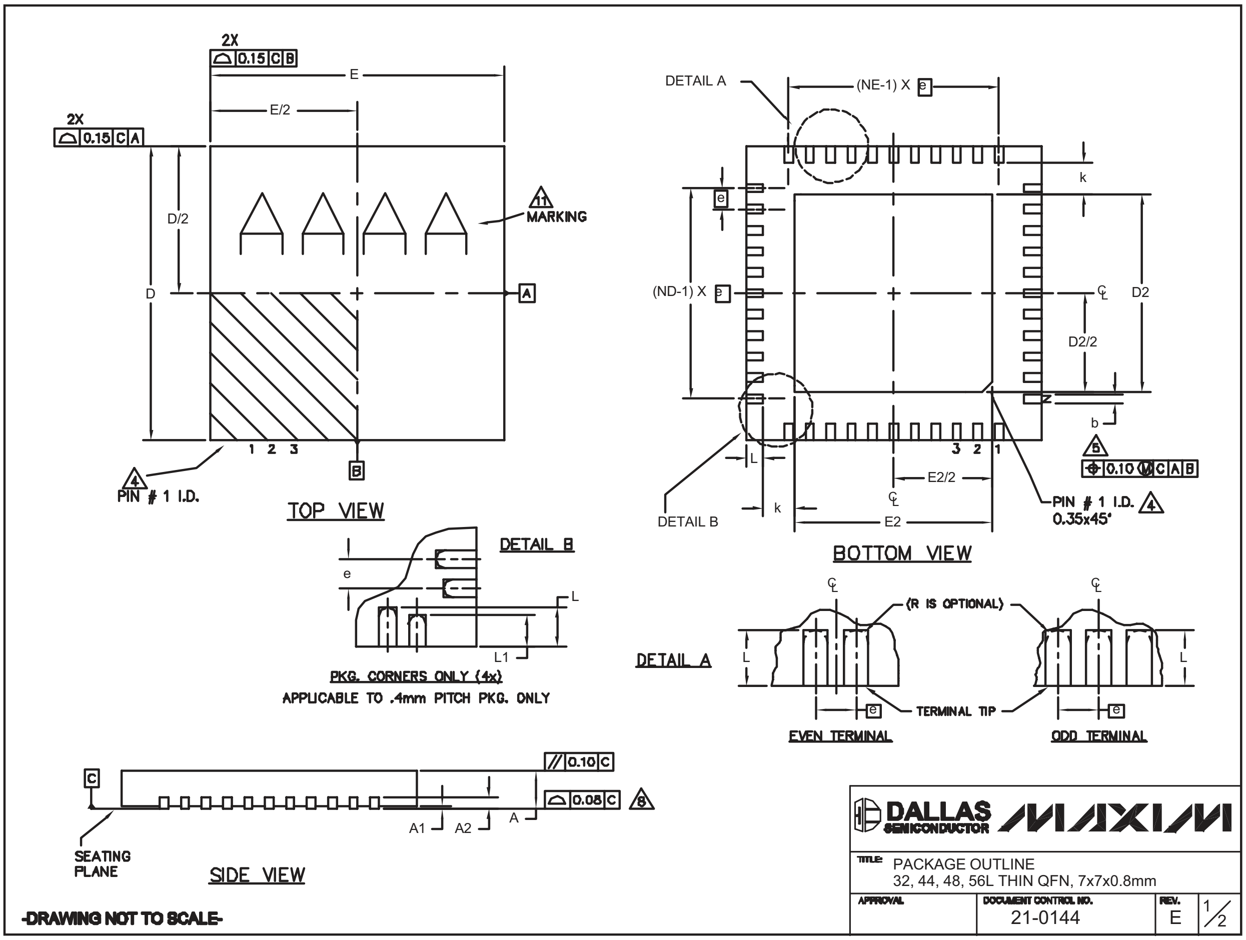
Chip Information

PROCESS: BiCMOS

IEEE 802.3af PD Interface and PWM Controllers with Integrated Power MOSFETs

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7			56L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	0.35	0.45
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65	0.40	0.50	0.60
L1	–	–	–	–	–	–	–	–	–	–	–	–	0.30	0.40	0.50
N	32			44			48			44			56		
ND	8			11			12			10			14		
NE	8			11			12			12			14		

EXPOSED PAD VARIATIONS									
PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C	DOWN BONDS ALLOWED
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T3277-2	–	4.55	4.70	4.85	4.55	4.70	4.85	–	YES
T3277-3	–	4.55	4.70	4.85	4.55	4.70	4.85	–	NO
T4477-2	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1	YES
T4477-3	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1	YES
T4877-1**	13,24,37,48	4.20	4.30	4.40	4.20	4.30	4.40	–	NO
T4877-3	–	4.95	5.10	5.25	4.95	5.10	5.25	–	YES
T4877-4	–	5.45	5.60	5.63	5.45	5.60	5.63	–	YES
T4877-5	–	2.40	2.50	2.60	2.40	2.50	2.60	–	NO
T4877-6	–	5.45	5.60	5.63	5.45	5.60	5.63	–	NO
T4877-7	–	4.95	5.10	5.25	4.95	5.10	5.25	–	YES
T5677-1	–	5.20	5.30	5.40	5.20	5.30	5.40	–	YES

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED. TOTAL NUMBER OF LEADS ARE 44.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 EXCEPT THE EXPOSED PAD DIMENSIONS OF T4877-1/-3/-4/-5/-6 & T5677-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE
32, 44, 48, 56L THIN QFN, 7x7x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0144	E	2/2

Revision History

Pages changed at Rev 1: 1, 27