



MPEG Clock Generator with VCXO

Features

- Integrated phase-locked loop (PLL)
- Low-jitter, high-accuracy outputs
- VCXO with analog adjust
- 3.3V operation

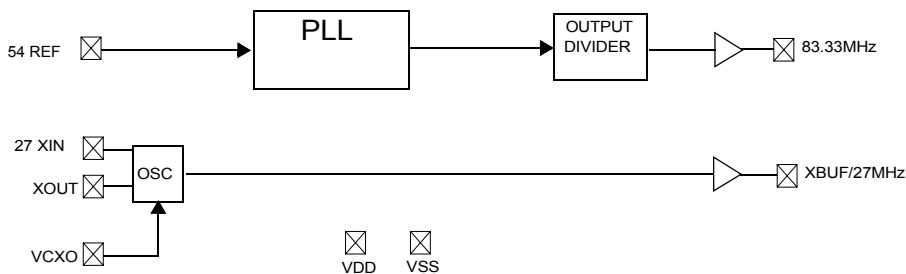
Benefits

- Highest-performance PLL tailored for multimedia applications
- Meets critical timing requirements in complex system designs
- Application compatibility for a wide variety of designs

Frequency Table

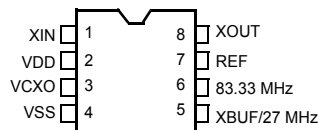
Part Number	Outputs	Input Frequency Range	Output Frequencies	VCXO Control Curve	Other Features
CY241V08A-41	1	27-MHz pullable crystal input per Cypress specification	One copy of 27 MHz One copy of 83.33 MHz (non-pullable)	linear	Pinout-compatible with MK3741

Block Diagram



Pin Configuration

CY241V08A-41
8-pin SOIC



Pin Descriptions

Name	Pin Number	Description
XIN	1	Reference crystal input.
VDD	2	Voltage supply.
VCXO	3	Input analog control for VCXO.
VSS	4	Ground.
XBUF/27 MHz	5	27-MHz buffered crystal output.
83.33 MHz	6	83.33-MHz clock output.
REF	7	54-MHz reference input.
XOUT	8	Reference crystal output.

Absolute Maximum Conditions

Supply Voltage (V_{DD}) -0.5 to +7.0V
 DC Input Voltage -0.5V to $V_{DD} + 0.5$
 Storage Temperature (Non-condensing) -55°C to +125°C
 Junction Temperature -40°C to +125°C

Data Retention @ $T_j = 125^\circ\text{C}$ > 10 years
 Package Power Dissipation 350 mW
 ESD (Human Body Model) MIL-STD-883 > 2000V
 (Above which the useful life may be impaired. For user guidelines, not tested.)

Pullable Crystal Specifications^[1]

Parameter	Description	Comments	Min.	Typ.	Max.	Unit
F_{NOM}	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut	-	27	-	MHz
C_{LNOM}	Nominal load capacitance		-	14	-	pF
R_1	Equivalent series resistance (ESR)	Fundamental mode	-	-	25	Ω
R_3/R_1	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R_1 values are much less than the maximum spec	3	-	-	-
DL	Crystal drive level	No external series resistor assumed	150	-	-	μW
F_{3SEPHI}	Third overtone separation from $3 \cdot F_{NOM}$	High side	300	-	-	ppm
F_{3SEPLO}	Third overtone separation from $3 \cdot F_{NOM}$	Low side	-	-	-150	ppm
C_0	Crystal shunt capacitance		-	-	7	pF
C_0/C_1	Ratio of shunt to motional capacitance		180	-	250	-
C_1	Crystal motional capacitance		14.4	18	21.6	fF

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	3.135	3.3	3.465	V
T_A	Ambient Temperature	0	-	70	$^\circ\text{C}$
C_{LOAD}	Max. Load Capacitance	-	-	15	pF
t_{PU}	Power-up time for all V_{DD} pins to reach minimum specified voltage (power ramps must be monotonic)	0.05	-	500	ms

DC Electrical Specifications

Parameter	Name	Description	Min.	Typ.	Max.	Unit
I_{OH}	Output HIGH Current	$V_{OH} = V_{DD} - 0.5\text{V}$, $V_{DD} = 3.3\text{V}$	12	24	-	mA
I_{OL}	Output LOW Current	$V_{OL} = 0.5\text{V}$, $V_{DD} = 3.3\text{V}$	12	24	-	mA
C_{IN}	Input Capacitance	Except XIN, XOUT pins	-	-	7	pF
V_{VCXO}	VCXO Input Range		0	-	V_{DD}	V
$f_{\Delta XO}$ ^[2]	VCXO Pullability Range	Low Side	-	-	-115	ppm
		High Side	115	-	-	ppm
I_{VDD}	Supply Current		-	-	40	mA

AC Electrical Specifications ($V_{DD} = 3.3\text{V}$)^[3]

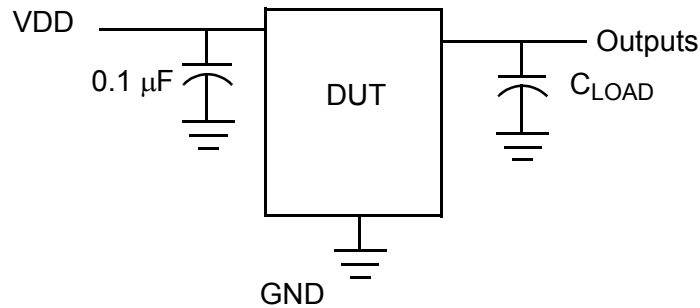
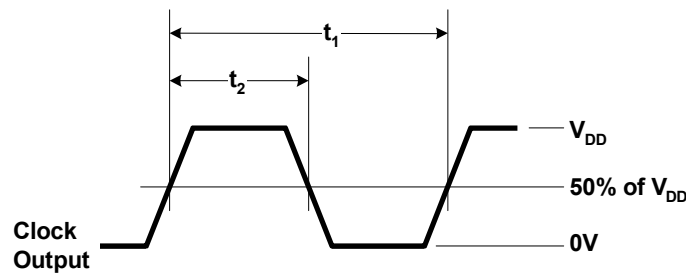
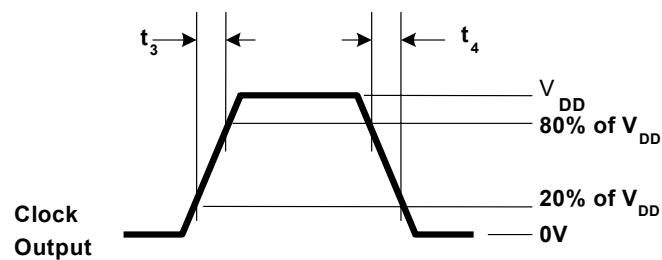
Parameter ^[3]	Name	Description	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in <i>Figure 1</i> , 50% of V_{DD}	45	50	55	%
ER	Rising Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD} . $C_{LOAD} = 15\text{ pF}$. See <i>Figure 2</i> .	0.8	1.4	-	V/ns
EF	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of V_{DD} . $C_{LOAD} = 15\text{ pF}$. See <i>Figure 2</i> .	0.8	1.4	-	V/ns

Notes:

- Crystals that meet this specification includes: Ecliptek ECX-5808-27.000M
- 115/+115 ppm assumes 2.5 pF of additional board level load capacitance. This range will be shifted down with more board capacitance or shifted up with less board capacitance.
- Not 100% tested.

AC Electrical Specifications ($V_{DD} = 3.3V$) (continued)^[3]

Parameter ^[3]	Name	Description	Min.	Typ.	Max.	Unit
t_9	Clock Jitter 83.33 MHz	Peak-to-peak period jitter	–	–	500	ps
t_9	Clock Jitter XBUF/27 MHz	Peak-to-peak period jitter	–	–	375	ps
t_{10}	PLL Lock Time		–	–	3	ms

Test and Measurement Set-up

Voltage and Timing Definitions

Figure 1. Duty Cycle Definition

Figure 2. $ER = (0.6 \times V_{DD}) / t_3$, $EF = (0.6 \times V_{DD}) / t_4$
Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage	Features
CY241V08ASC-41	S8	8-pin SOIC	Commercial	3.3V	Linear VCXO control curve
CY241V08ASC-41T	S8	8-pin SOIC – Tape and Reel	Commercial	3.3V	Linear VCXO control curve

Document History Page

Document Title: CY241V08A-41 MPEG Clock Generator with VCXO Document Number: 38-07655				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	213686	See ECN	RGL	New Data Sheet
*A	220421	See ECN	RGL	Minor Change: To post on web