International
IOR Rectifier

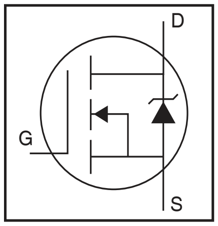
AUTOMOTIVE GRADE

AUIRLS4030
AUIRLSL4030

HEXFET® Power MOSFET

Features

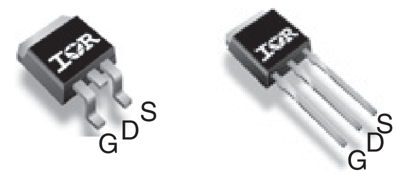
- Optimized for Logic Level Drive
- Advanced Process Technology
- Ultra Low On-Resistance
- Logic Level Gate Drive
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *



V_{DSS}		100V
$R_{DS(on)}$	typ.	3.4mΩ
	max.	4.3mΩ
I_D		180A

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating . These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



D^2Pak
AUIRLS4030

TO-262
AUIRLSL4030

G	D	S
Gate	Drain	Source

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRLS4030	D2-Pak	Tube	50	AUIRLS4030
		Tape and Reel Left	800	AUIRLS4030TRL
		Tape and Reel Right	800	AUIRLS4030TRR
AUIRLSL4030	TO-262 Pak	Tube	50	AUIRLSL4030

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	180	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	130	
I_{DM}	Pulsed Drain Current ①	730	
P_D @T_C = 25°C	Maximum Power Dissipation	370	W
	Linear Derating Factor	2.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy (Thermally limited) ②	305	mJ
I_{AR}	Avalanche Current ①	See Fig. 14, 15, 22a, 22b,	A
E_{AR}	Repetitive Avalanche Energy ①		mJ
dv/dt	Peak Diode Recovery ③	21	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑦⑨	——	0.40	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) , D^2Pak ⑧	——	40	

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*Qualification standards can be found at http://www.irf.com/

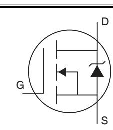
Static Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	–––	–––	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.10	–––	V/°C	Reference to 25°C, I_D = 5mA ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	3.4	4.3	mΩ	V_{GS} = 10V, I_D = 110A ④
		–––	3.6	4.5		V_{GS} = 4.5V, I_D = 92A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	–––	2.5	V	V_{DS} = V_{GS}, I_D = 250μA
gfs	Forward Transconductance	320	–––	–––	S	V_{DS} = 25V, I_D = 110A
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	20	μA	V_{DS} = 100V, V_{GS} = 0V
		–––	–––	250		V_{DS} = 100V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	100	nA	V_{GS} = 16V
	Gate-to-Source Reverse Leakage	–––	–––	-100		V_{GS} = -16V
$R_{G(int)}$	Internal Gate Resistance	–––	2.1	–––	Ω	

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	–––	87	130	nC	I_D = 110A
Q_{gs}	Gate-to-Source Charge	–––	27	–––		V_{DS} = 50V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	45	–––		V_{GS} = 4.5V ④
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})	–––	42	–––		I_D = 110A, V_{DS} =0V, V_{GS} = 4.5V
$t_{d(on)}$	Turn-On Delay Time	–––	74	–––	ns	V_{DD} = 65V
t_r	Rise Time	–––	330	–––		I_D = 110A
$t_{d(off)}$	Turn-Off Delay Time	–––	110	–––		R_G = 2.7Ω
t_f	Fall Time	–––	170	–––		V_{GS} = 4.5V ④
C_{iss}	Input Capacitance	–––	11360	–––	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	–––	670	–––		V_{DS} = 50V
C_{rss}	Reverse Transfer Capacitance	–––	290	–––		f = 1.0MHz
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	–––	760	–––		V_{GS} = 0V, V_{DS} = 0V to 80V ⑥
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)	–––	1140	–––		V_{GS} = 0[redacted]

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	180	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	730		
V_{SD}	Diode Forward Voltage	–––	–––	1.3	V	T_J = 25°C, I_S = 110A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	–––	50	–––	ns	T_J = 25°C V_R = 85V,
		–––	60	–––		T_J = 125°C I_F = 110A
Q_{rr}	Reverse Recovery Charge	–––	88	–––	nC	T_J = 25°C di/dt = 100A/μs ④
		–––	130	–––		T_J = 125°C
I_{RRM}	Reverse Recovery Current	–––	3.3	–––	A	T_J = 25°C
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.05mH, R_G = 25Ω, I_{AS} = 110A, V_{GS} =10V. Part not recommended for use above this value .

③ I_{SD} ≤ 110A, di/dt ≤ 1330A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

④ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ R_θ is measured at T_J approximately 90°C.

⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniquea refer to applocation note # AN- 994 echniques refer to application note #AN-994.

⑨ $R_{\theta JC}$ value shown is at time zero.

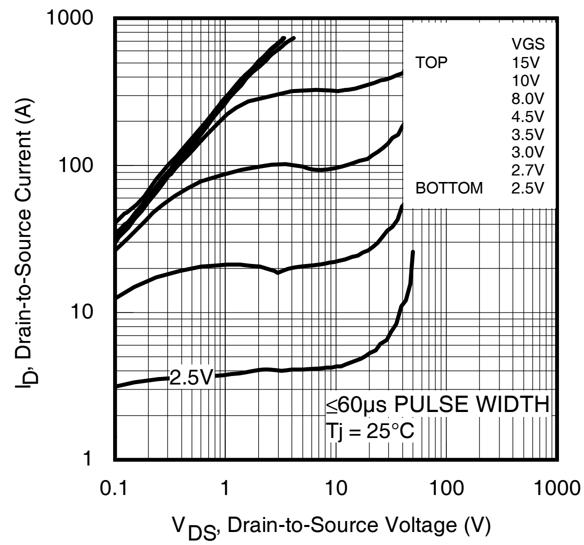


Fig 1. Typical Output Characteristics

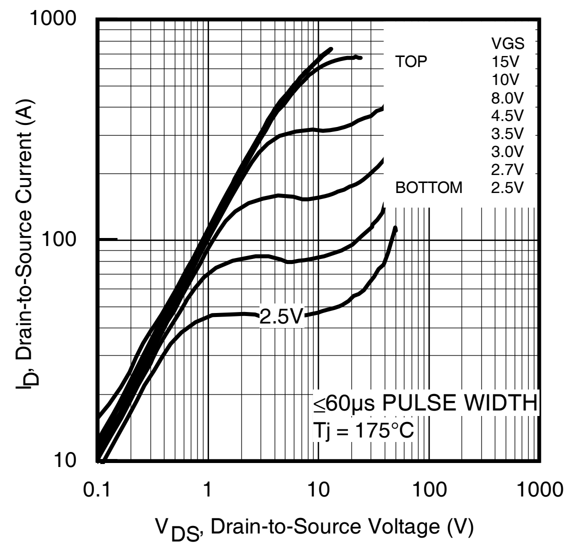


Fig 2. Typical Output Characteristics

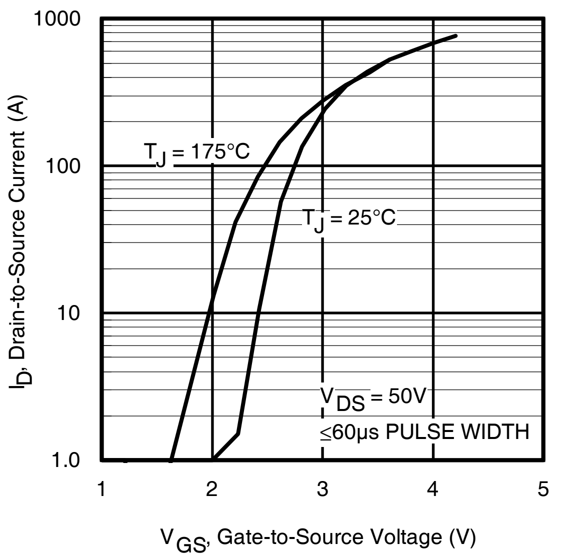


Fig 3. Typical Transfer Characteristics

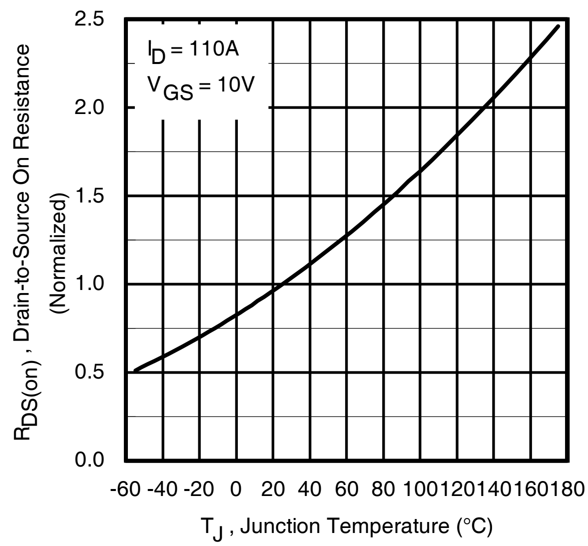


Fig 4. Normalized On-Resistance vs. Temperature

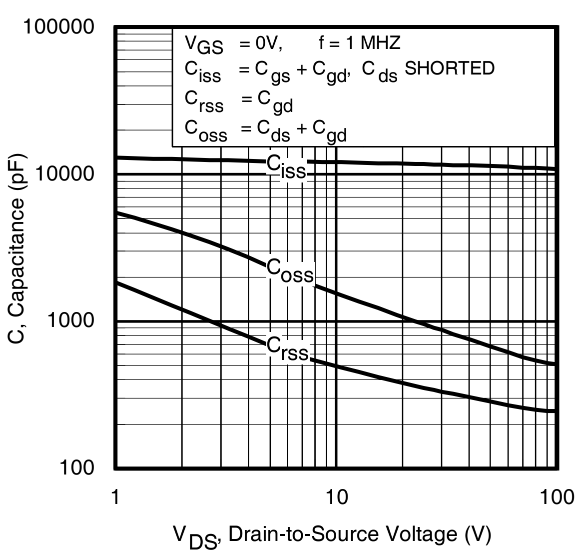


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

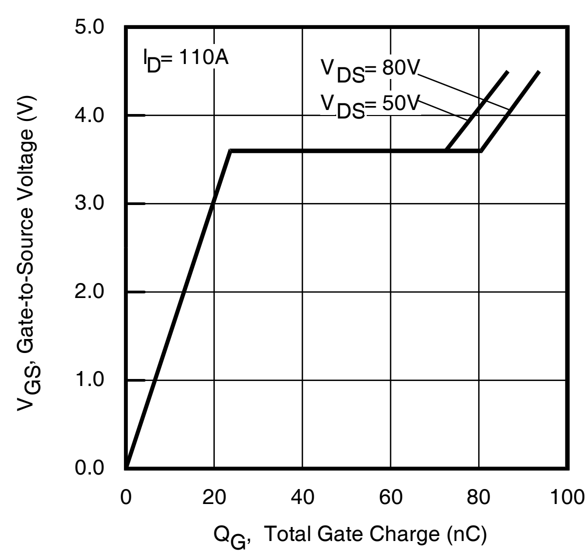


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

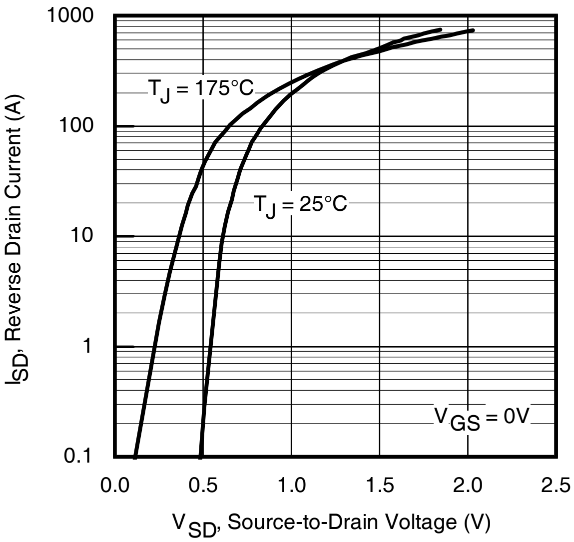


Fig 7. Typical Source-Drain Diode Forward Voltage

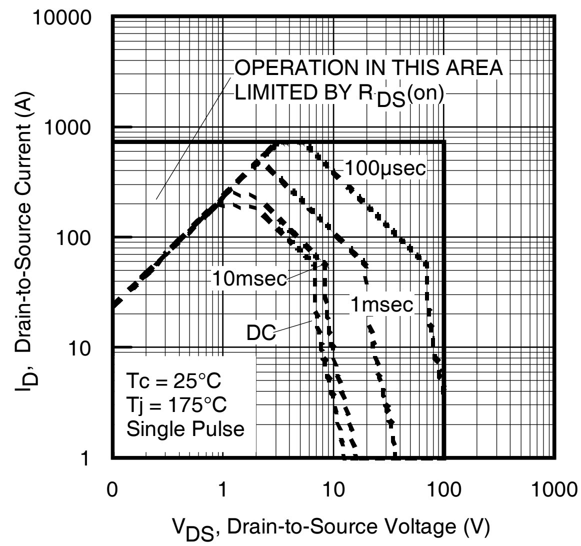


Fig 8. Maximum Safe Operating Area

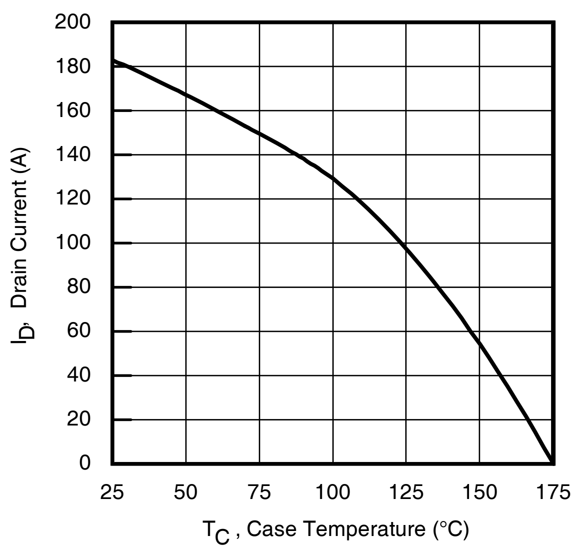


Fig 9. Maximum Drain Current vs. Case Temperature

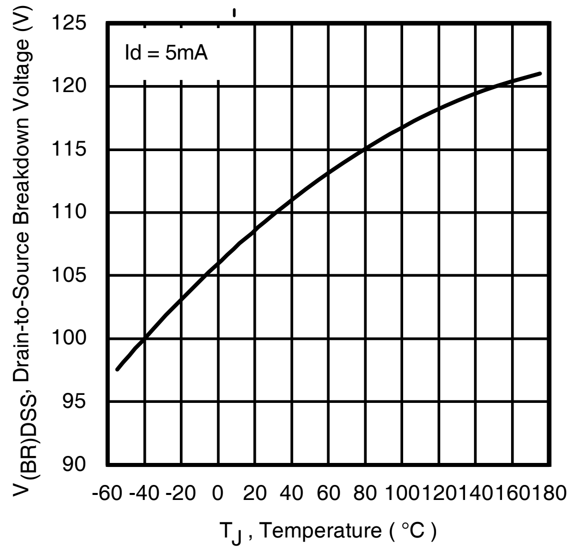


Fig 10. Drain-to-Source Breakdown Voltage

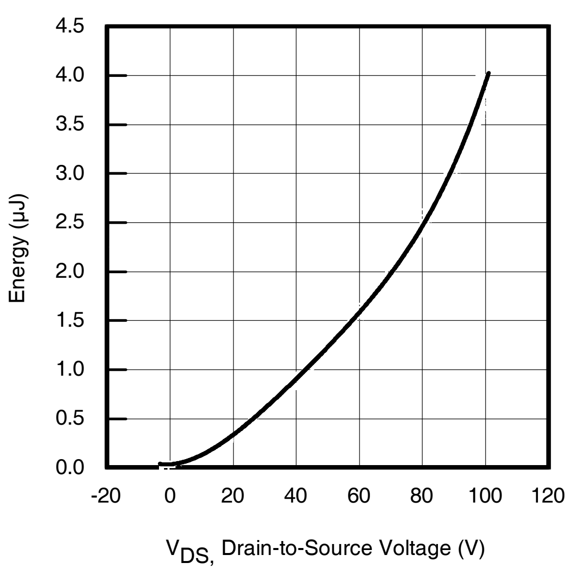


Fig 11. Typical C_{OSS} Stored Energy

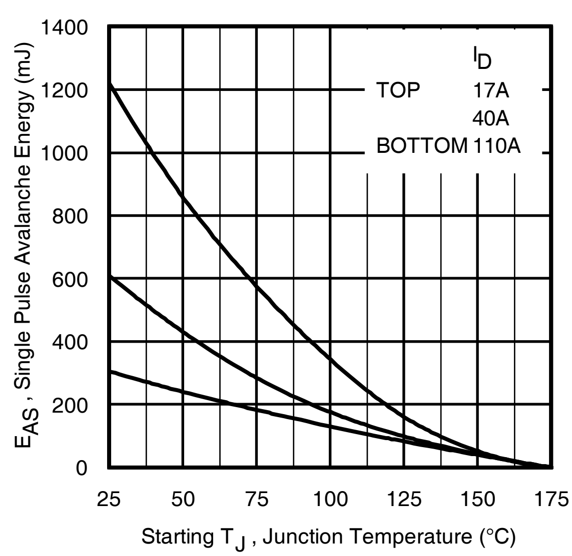


Fig 12. Maximum Avalanche Energy vs. DrainCurrent

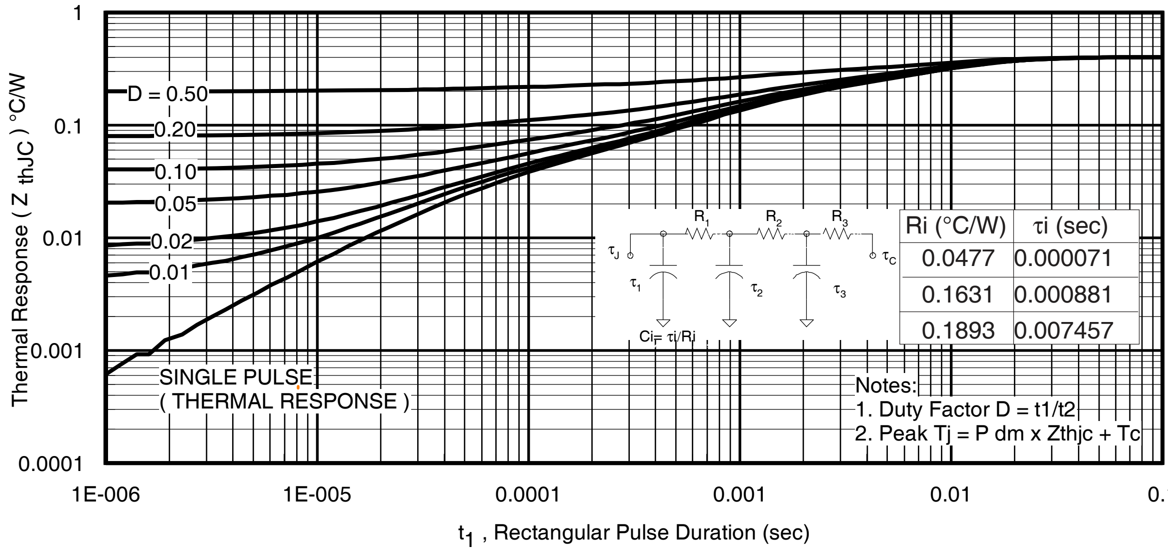


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

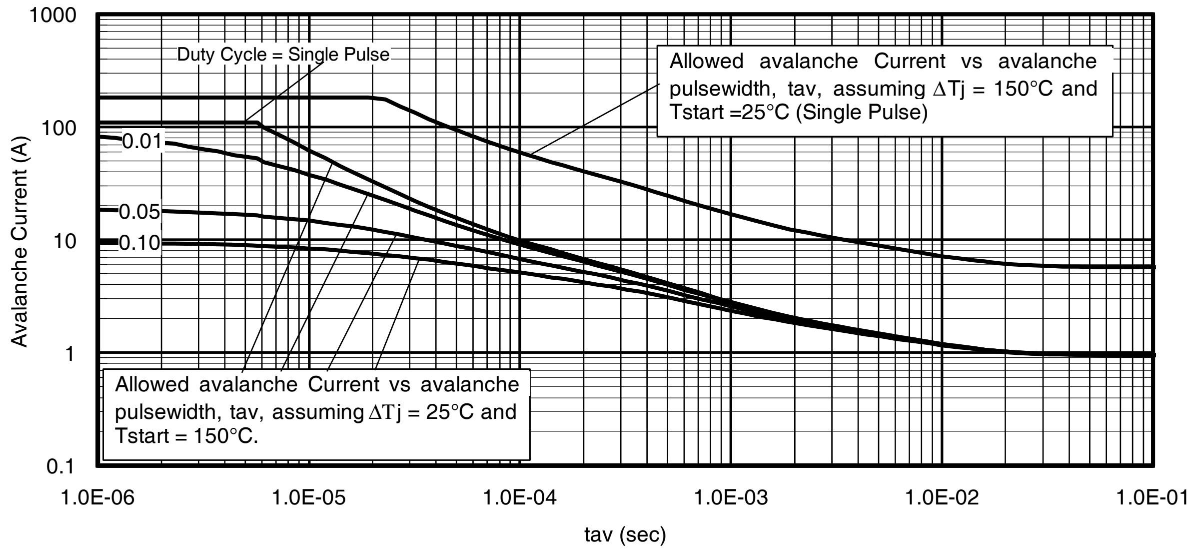


Fig 14. Typical Avalanche Current vs.Pulsewidth

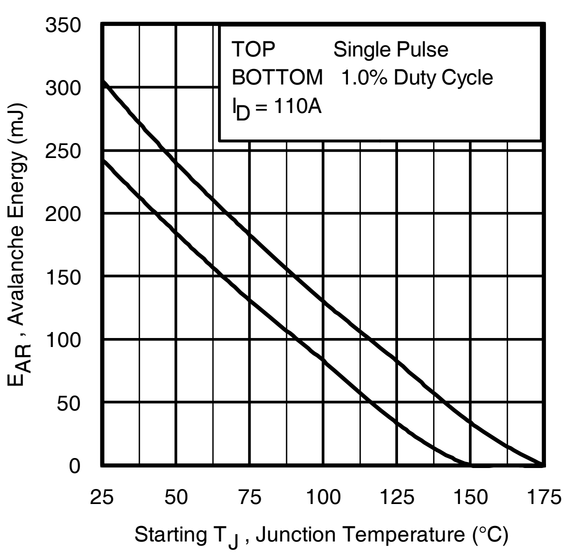


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

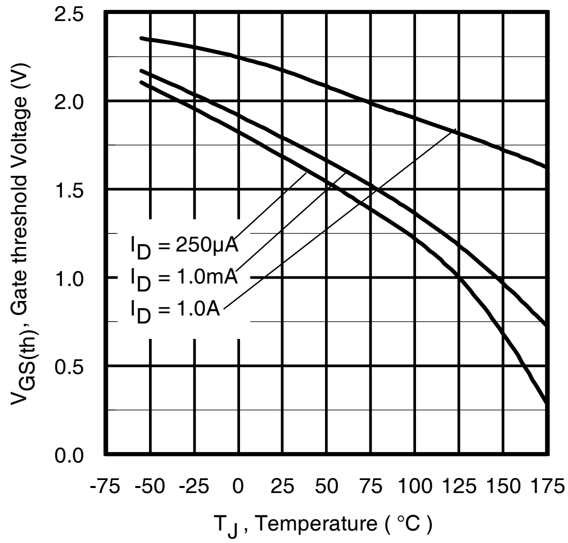


Fig 16. Threshold Voltage vs. Temperature

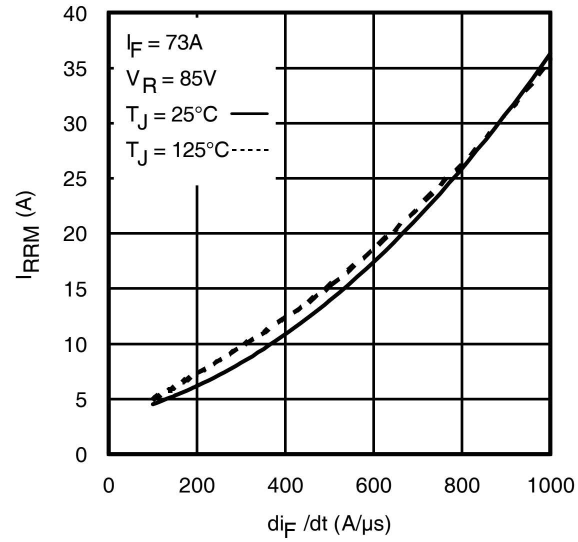


Fig. 17 - Typical Recovery Current vs. di_f/dt

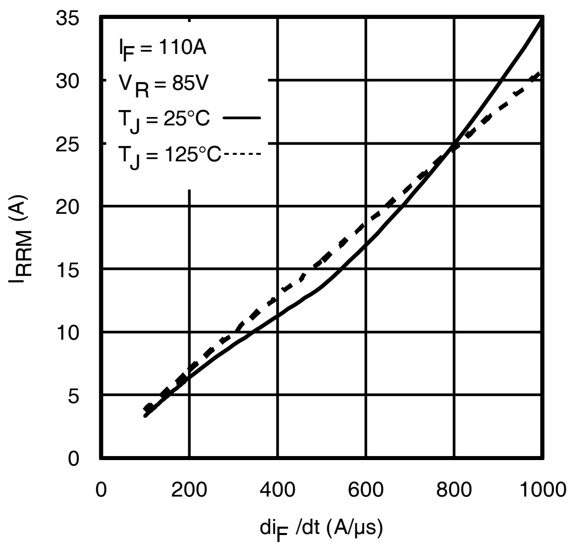


Fig. 18 - Typical Recovery Current vs. di_f/dt

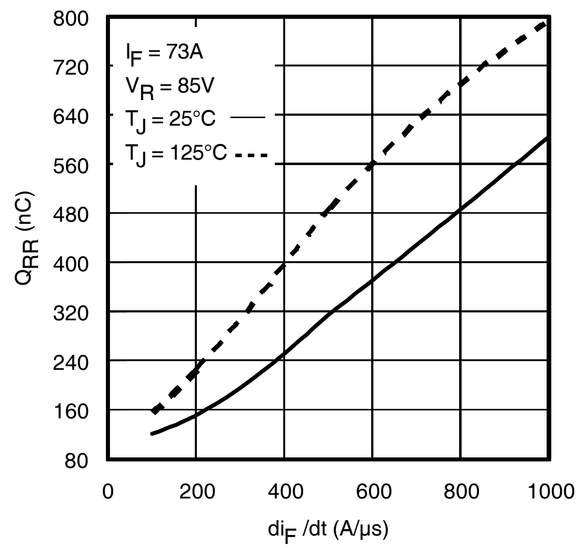


Fig. 19 - Typical Stored Charge vs. di_f/dt

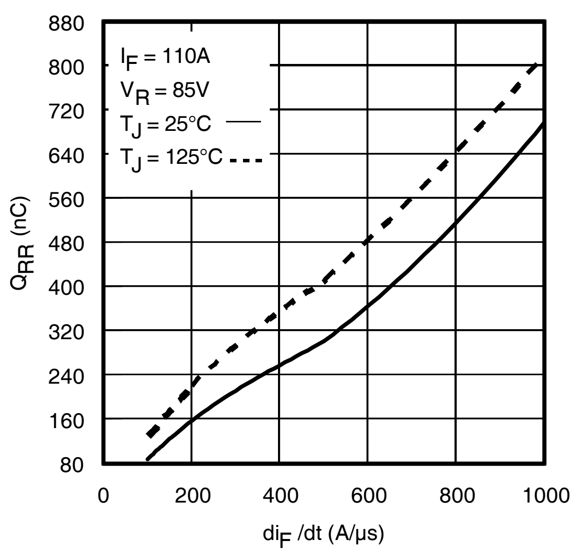
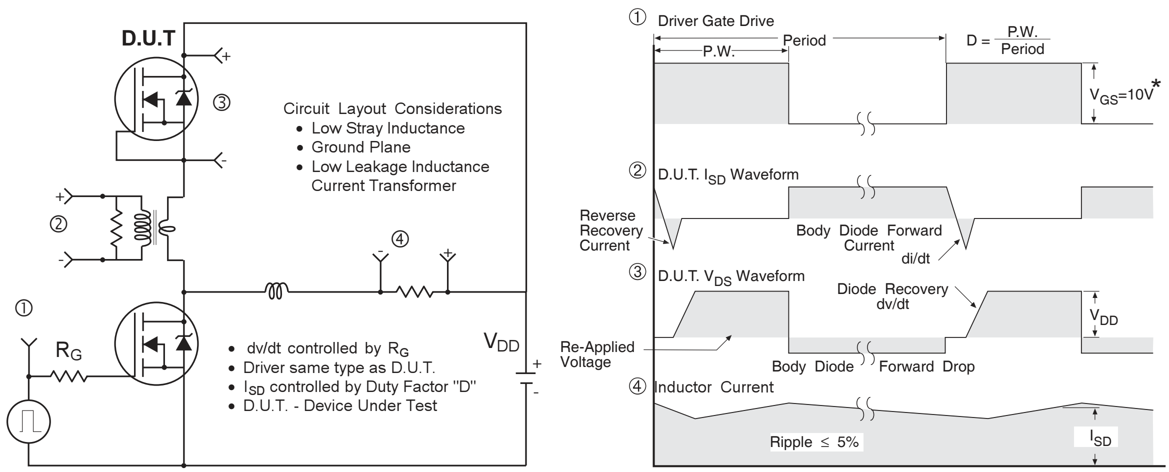


Fig. 20 - Typical Stored Charge vs. di_f/dt



* V_{GS} = 5V for Logic Level Devices

Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

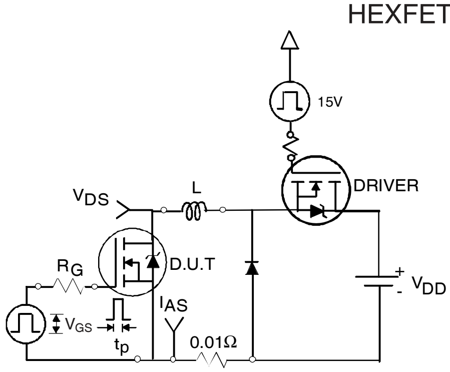


Fig 22a. Unclamped Inductive Test Circuit

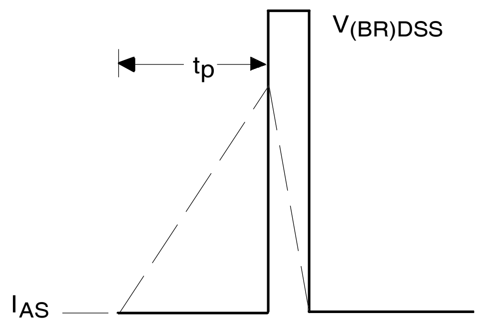


Fig 22b. Unclamped Inductive Waveforms

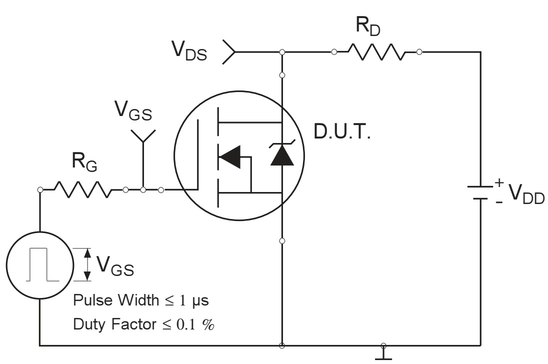


Fig 23a. Switching Time Test Circuit

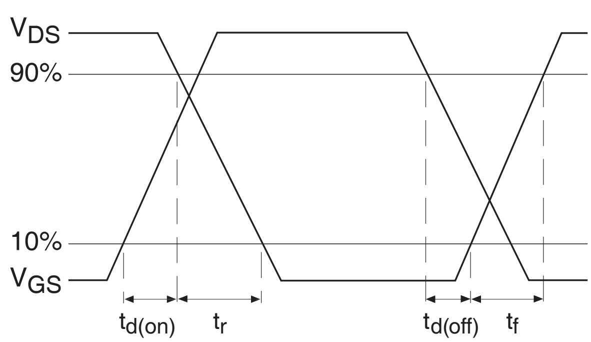


Fig 23b. Switching Time Waveforms

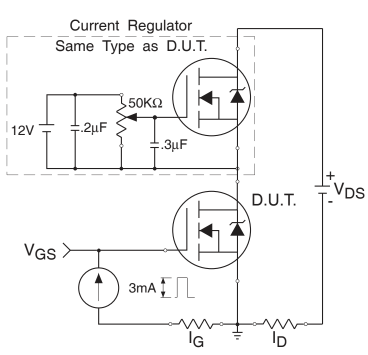


Fig 24a. Gate Charge Test Circuit

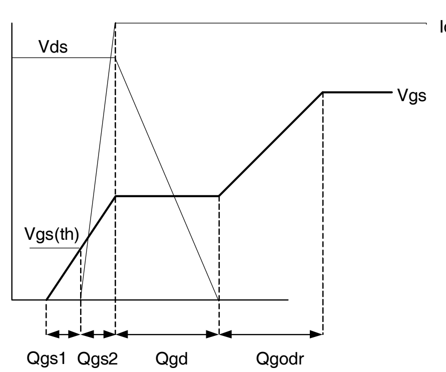
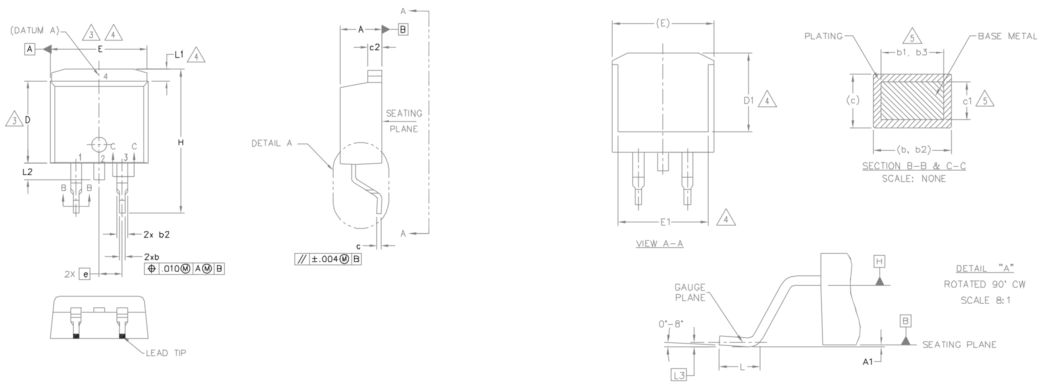


Fig 24b. Gate Charge Waveform

D²Pak Package Outline (Dimensions are shown in millimeters (inches))



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270	–	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245	–	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.68	–	.066	4
L2	–	1.78	–	.070	
L3	0.25 BSC		.010 BSC		

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

LEAD ASSIGNMENTS

DIODES

1.- ANODE (TWO DIE) / OPEN (ONE DIE)
2, 4.- CATHODE
3.- ANODE

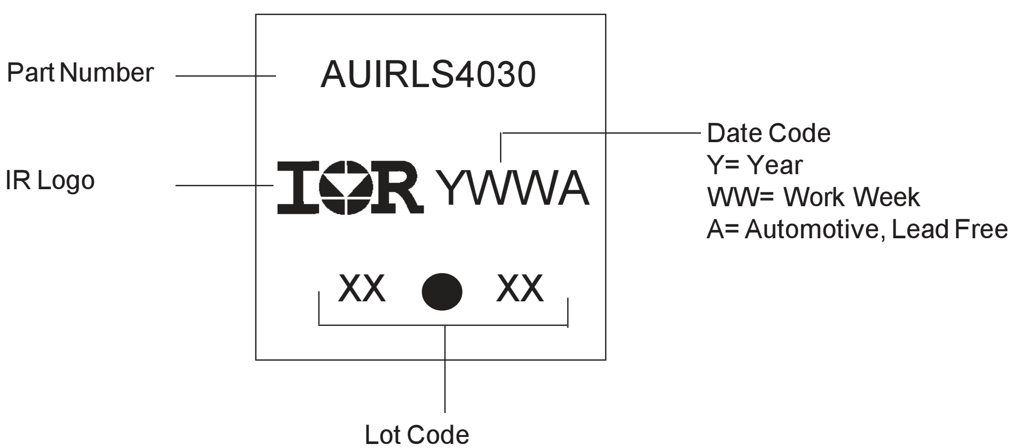
HEXFET

1.- GATE
2, 4.- DRAIN
3.- SOURCE

IGBTs, CoPACK

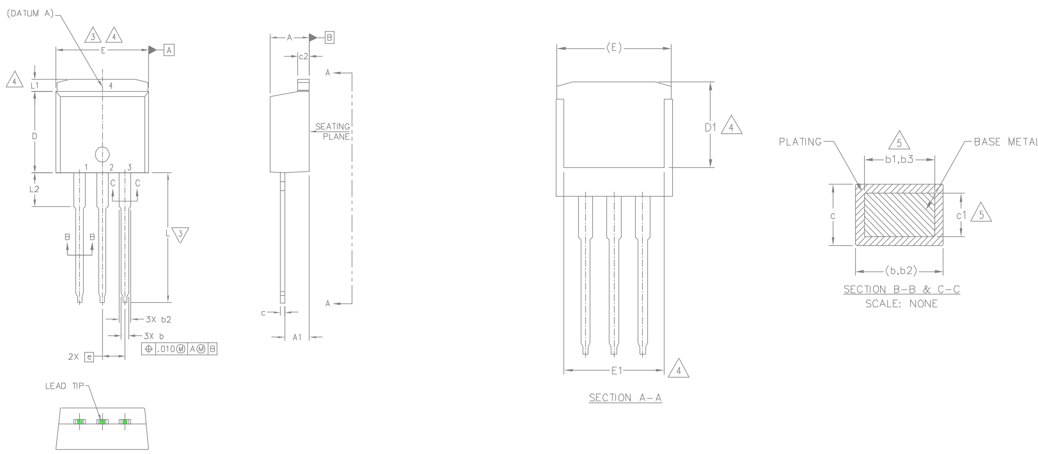
1.- GATE
2, 4.- COLLECTOR
3.- EMITTER

D²Pak Part Marking Information



Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

TO-262 Package Outline (Dimensions are shown in millimeters (inches))



SYMBOL	DIMENSIONS MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.	NOTES
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270	–	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245		4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	–	1.65	–	.065	4
L2	3.56	3.71	.140	.146	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. (△3) DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. (△4) THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. (△5) DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS

IGBTs, CoPACK

1.- GATE
2.- COLLECTOR
3.- EMITTER
4.- COLLECTOR

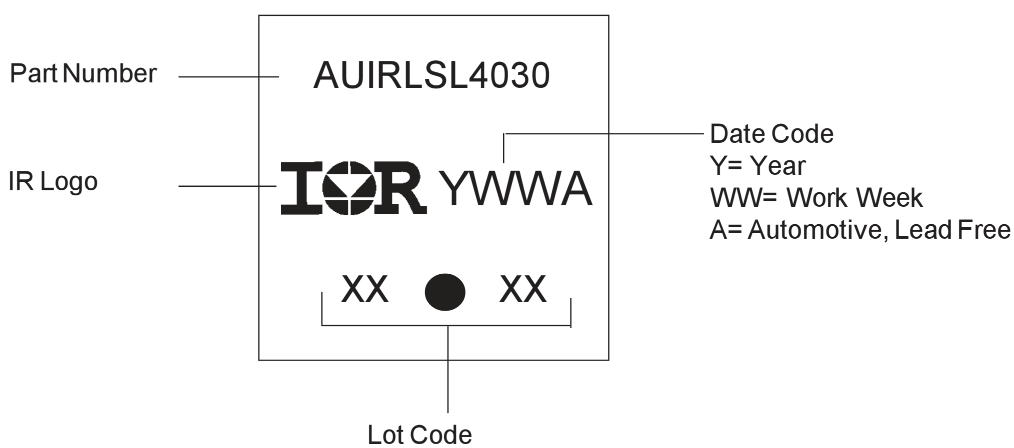
HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

DIODES

1.- ANODE (TWO DIE) / OPEN (ONE DIE)
2, 4.- CATHODE
3.- ANODE

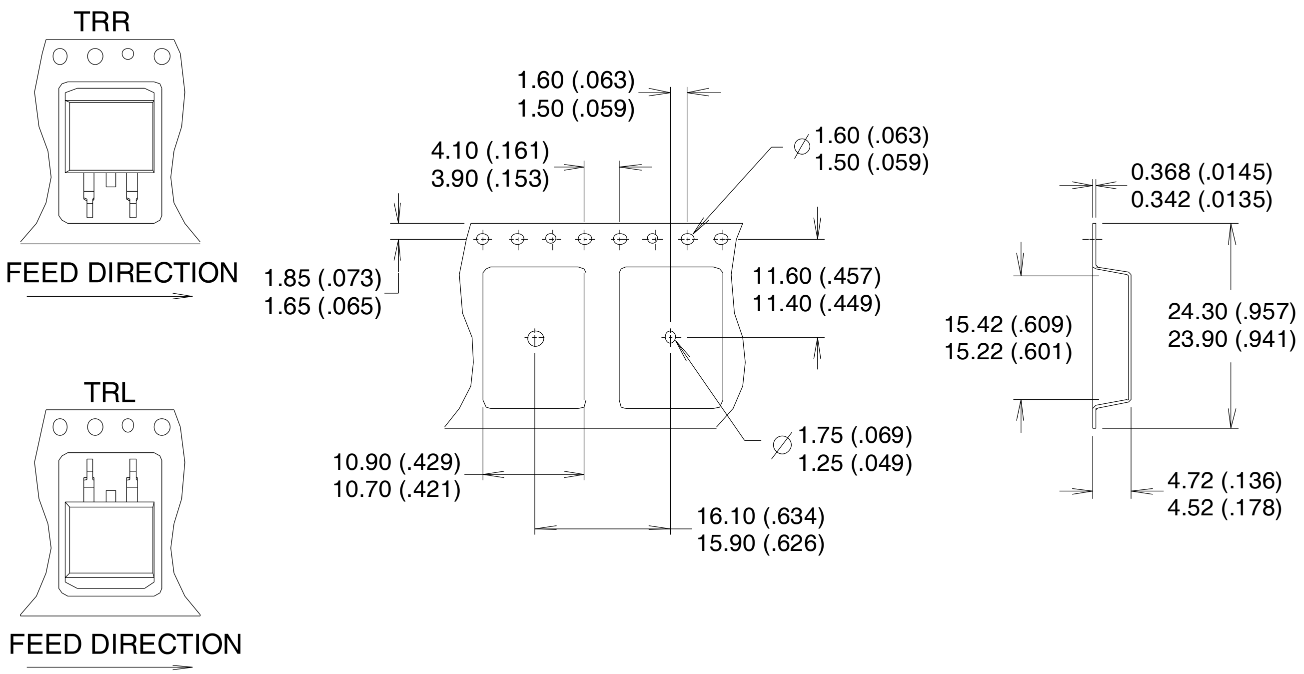
TO-262 Part Marking Information

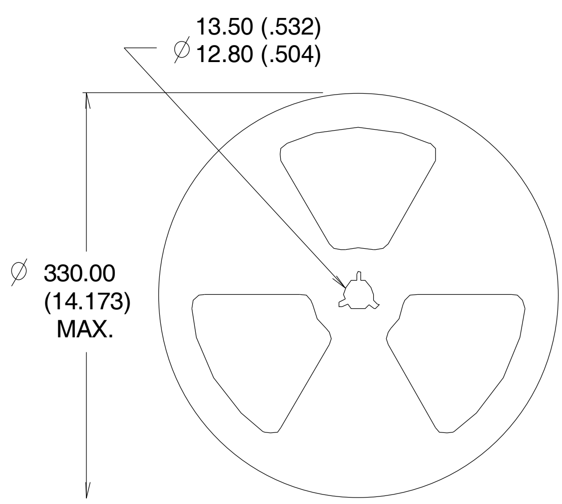


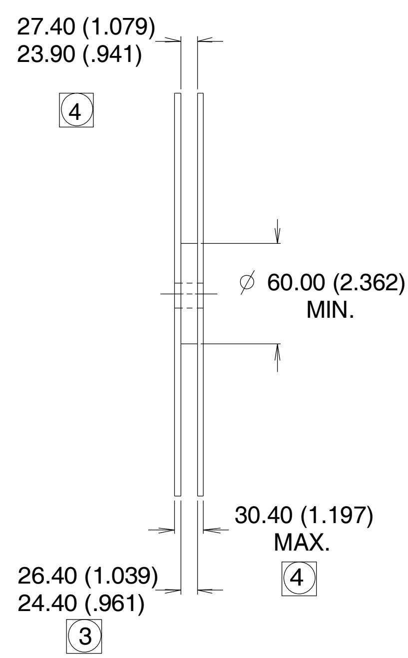
Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

D²Pak (TO-263AB) Tape & Reel Information

Dimensions are shown in millimeters (inches)







NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information†

<table>
<tr><td rowspan="2">Qualification Level</td><td colspan="3">Automotive
(per AEC-Q101) ††</td></tr>
<tr><td colspan="3">Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.</td></tr>
<tr><td rowspan="2">Moisture Sensitivity Level</td><td colspan="2">3L-D2 PAK</td><td rowspan="2">MSL1</td></tr>
<tr><td colspan="2">3L-TO-262</td></tr>
<tr><td rowspan="3">ESD</td><td>Machine Model</td><td colspan="2">Class M4(+/- 800V)†††
(per AEC-Q101-002)</td></tr>
<tr><td>Human Body Model</td><td colspan="2">Class H3A(+/- 6000V)†††
(per AEC-Q101-001)</td></tr>
<tr><td>Charged Device Model</td><td colspan="2">Class C5(+/- 2000V)†††
(per AEC-Q101-005)</td></tr>
<tr><td>RoHS Compliant</td><td colspan="3">Yes</td></tr>
</table>

† Qualification standards can be found at International Rectifier's web site: http//www.irf.com/

†† Exceptions (if any) to AEC-Q101 requirements are noted in the qualification report.

††† Highest passing voltage

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http://www.irf.com/technical-info/

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Revision History

Date	Comments
3/3/2014	• Added "Logic Level Gate Drive" bullet in the features section on page 1 • Updated data sheet with new IR corporate template
4/9/2014	• Updated package outline and part marking on page 8 & 9. • Updated Qualification table -TO262 Pak from "N/A" to "MSL1" on page 11. • Updated typo on the fig.19 and fig.20, unit of y-axis from "A" to "nC" on page 6.

