

## FEATURES

### • High Performance Non-Blocking Switch Architecture

- 48-lane 12-port PCIe switch
- Integrated SerDes supports 8.0 GT/s Gen3, 5.0 GT/s Gen2 and 2.5 GT/s Gen1 operation
- Delivers up to 96 GBps (768 Gbps) of switching capacity
- Low latency cut-through architecture
- Multicast compliant to Spec
- Supports up to 2 KB maximum payload size
- Request metering for maximum system throughput

### • Standards and Compatibility

- PCI Express Base Specification 3.0 compliant
- Implements the following optional PCI Express features:
  - Advanced Error Reporting (AER) on all ports
  - Access Control Services (ACS)
  - Alternative Routing ID (ARI) ECN
  - Internal Error Reporting (IER) ECN
  - Atomic operations ECN
  - TLP processing hints (TPH) ECN
  - Latency Tolerance Reporting (LTR) ECN
  - Optimized Buffer Flush/Fill (OBFF) ECN
- PCI Power Management Spec
  - Supports D0, D3hot and D3 power management states
- Active State Power Management (ASPM)

### • Switch Initialization/Configurability

- Supports x8, x4, x2 and x1 ports
- Automatic per port link width negotiation
- Automatic lane reversal
- Autonomous and software managed link width and speed control
- Per lane SerDes configuration
- Supports Global and Local reference port clock input
- Crosslink support
- 9 General Purpose I/O
- Supports Root (BIOS, DS, or driver), Serial EEPROM, pin strapping, or SMBus switch initialization
- No power sequencing requirements

### • Multi-Root Support

- Supports up to 12 fully independent switch partitions
- Configurable downstream port device numbering
- Supports dynamic reconfiguration of switch partitions
- Movable upstream port within and between switch partitions

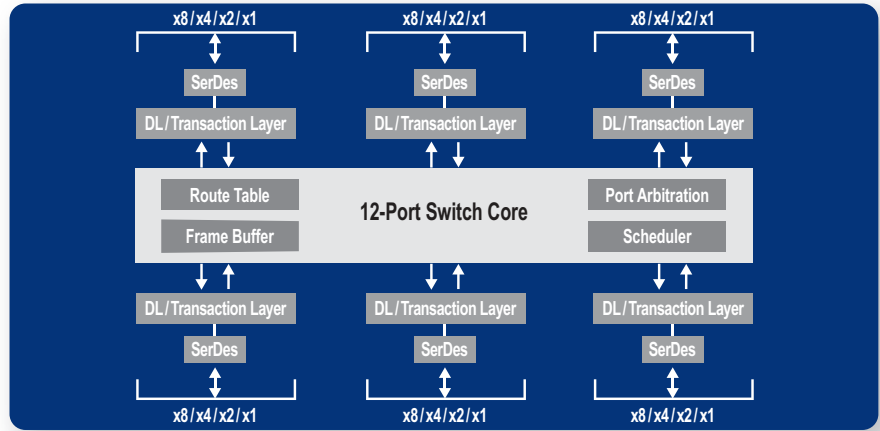
### • Reliability, Availability and Serviceability (RAS)

- ECRC support
- AER on all ports
- SECCED ECC protection on all internal RAMs
- End-to-end data path parity protection
- Ability to generate an interrupt (INTx or MSI) on link up/down transitions
- Hot-plug supported on all downstream switch ports
- On-chip link activity and status outputs available including the upstream ports
- Supports IEEE 1149.6 AC JTAG and IEEE 1149.1 JTAG

### • Development Tools

- 89KTPES48H12G3 Evaluation Board
- PCIe Browser Software
- Provides ODS (On-Die Scope)
- Built-in PRBS generator and checker
- Documentation and support at: [www.IDT.com](http://www.IDT.com)

### • Packaged in a 27mm x 27mm 676-ball FCBGA

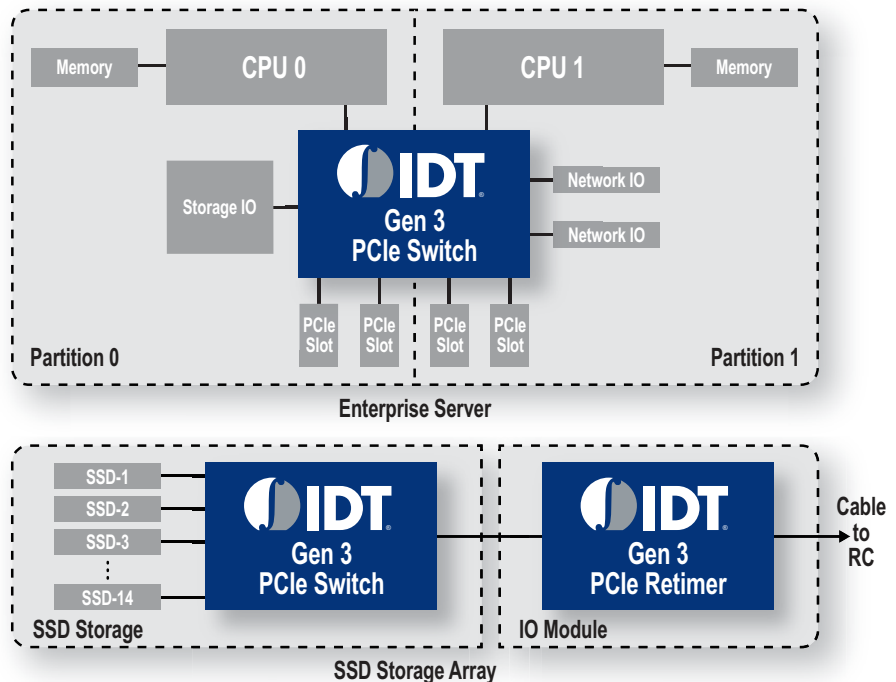


48 PCI Express Lanes - Up to 6 x8 ports or 12 x4 ports

## Device Overview

The 89H48H12G3 is a 48-lane, 12-port system interconnect switch optimized for PCI Express® Gen3 packet switching in high-performance applications, supporting multiple simultaneous peer-to-peer traffic flows. Target applications include servers, storage, communications, embedded systems, and multi-host or intelligent I/O based systems with inter-domain communication.

Utilizing standard PCI Express Gen3 interconnect, the 89H48H12G3 provides the most efficient system interconnect switching solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides 96 GBps (768 Gbps) of aggregated, full-duplex switching capacity through 48 integrated serial lanes, using proven and robust IDT technology. Each lane is capable of 8 GT/s of bandwidth in both directions and is fully compliant with PCI Express Base Specification 3.0.



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