

## 1.7MHz, 50μA/ch, Excellent EMI Immunity, Rail-to-Rail Input/Output, Operational Amplifier

### ■ FEATURES ( $V^+ = 5V$ , Typical value)

- High Efficiency:
  - GBW 1.7MHz
  - Supply Current 50μA/ch
- Rail-to-Rail Input and Output
- Supply Voltage 1.8V to 5.5V
- Integrated EMI filter EMIRR = 75dB @f = 900MHz
- Input Tolerant
- Unity-Gain stable
- Input Offset Voltage 5mV max.
- Slew Rate 0.8V/μs
- Operating Temperature -55°C to 125°C
- Package
  - NJU77550 / NJU77551 SOT-23-5, SC-88A
  - NJU77552 SOP8, MSOP8 (TVSP8)\*
  - \* meet JEDEC MO-187-DA / thin type
  - DFN8-U1 (ESON8-U1)
  - NJU77554 SSOP14

### ■ APPLICATIONS

- Battery-Powered Equipment
  - Audio, Healthcare, Security, etc.
- Gas / Smoke Sensors
- Smart Meter
- Sensor Interface
- Active Filters
- Photodiode Amplifier

### ■ DESCRIPTION

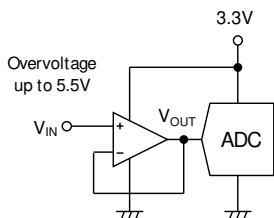
The NJU77550/NJU77551/NJU77552/NJU77554 are single, dual and quad rail-to-rail input and output single supply OpAmp, featuring low supply current of 50μA typical per amplifier, wide gain bandwidth product of 1.7MHz and a slew rate of 0.8V/μs. Furthermore, operating voltage from 1.8V single supply can contribute to energy saving design, it is most suitable for battery equipment required low power.

Low input bias current makes NJU7755x series suitable for photodiode amplifiers, piezoelectric sensors, smoke detector and other applications with high-impedance applications. A rail-to-rail input and output allows the device to be used in wide variety of applications, such as audio amplifier, high-side current sensing, active filter, buffering and others. And also, High EMI immunity that can reduced malfunctions caused by RF-noises from mobile phones and other electronic devices, and input tolerant that allows the input voltage (Recommended:  $V^+ = 5.5V$ ) that exceed positive supply voltage is ideal for robust industrial applications.

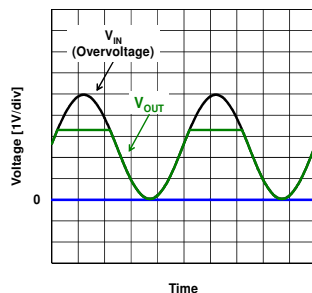
The NJU7755x series guarantees the specifications from 1.8V to 5.5V single supply, making it ideal for low voltage applications. In addition, the operating temperature is expanded to -55°C to 125°C, which can be used in harsh environments with large temperature changes.

The NJU77550/NJU77551 is available in 5-pin SC-88A and SOT-23-5 package. The NJU77552 is available in 8-pin SOP8, MSOP8 (TVSP): meet JEDEC MO-187-DA / thin type package and DFN that is thin and 2mm square small package. The NJU77554 is available in SSOP14 package.

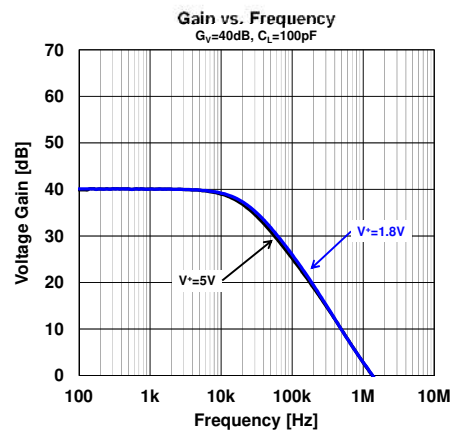
### TYPICAL APPLICATION



ADCbuffer with input tolerant



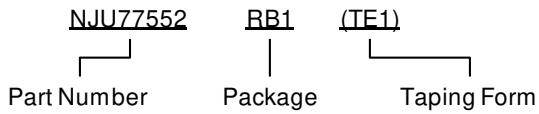
High Efficiency  
GBW=1.7MHz ( $I_{SUPPLY} = 50\mu A / ch$ )



## ■ PIN CONFIGURATIONS

PRODUCT NAME	NJU77550F3	NJU77550F	NJU77551F3	NJU77551F
Package	SC88A	SOT-23-5	SC88A	SOT-23-5
Pin Functions				
PRODUCT NAME	NJU77552G	NJU77552RB1	NJU77552KU1	
Package	SOP8	MSOP8 (TVSP8)	DFN8-U1 (ESON8-U1)	
Pin Functions			<p>(Connect to exposed pad to V<sup>-</sup>)</p>	
PRODUCT NAME	NJU77554V			
Package	SSOP14			
Pin Functions				

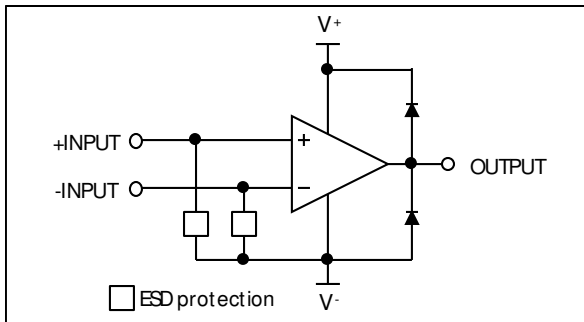
## ■ PRODUCT NAME INFORMATION



## ■ ORDERING INFORMATION

PRODUCT NAME	PACKAGE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJU77550F (TE1)	SOT-23-5	Yes	Yes	Sn2Bi	11P	15	3000
NJU77550F3 (TE1)	SC-88A	Yes	Yes	Sn2Bi	AU	7.5	3000
NJU77551F (TE1)	SOT-23-5	Yes	Yes	Sn2Bi	11R	15	3000
NJU77551F3 (TE1)	SC-88A	Yes	Yes	Sn2Bi	AV	7.5	3000
NJU77552G (TE2)	SOP8	Yes	Yes	Pure Sn	77552	88	2500
NJU77552RB1 (TE1)	MSOP8 (TVSP8)	Yes	Yes	Sn2Bi	77552	18	2000
NJU77552KU1 (TE3)	DFN8-U1 (ESON8-U1)	Yes	Yes	Sn2Bi	77552	5.3	3000
NJU77554V (TE1)	SSOP14	Yes	Yes	Sn2Bi	77554	65	2000

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS

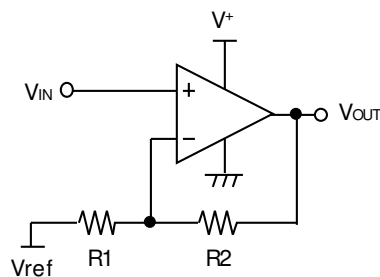
PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	$V^+ - V^-$	7	V
Input Voltage <sup>(1)</sup>	$V_{IN}$	$V^- - 0.3$ to $V^- + 7$	V
Input Current <sup>(2)</sup>	$I_{IN}$	10	mA
Output Terminal Input Voltage <sup>(3)</sup>	$V_O$	$V^- - 0.3$ to $V^+ + 0.3$	V
Differential Input Voltage <sup>(4)</sup>	$V_{ID}$	$\pm 7$	V
Output Short-Circuit Duration <sup>(5)</sup>		Continuous	
Power Dissipation ( $T_a = 25^\circ\text{C}$ )		2-Layer / 4-Layer <sup>(6)</sup>	
SOT-23-5 SC-88A SOP8 MSOP8 (TVSP8) DFN8-U1 (ESON8-U1) SSOP14	$P_D$	480 / 650 360 / 490 690 / 1000 510 / 680 450 / 1200 <sup>(7)</sup> 500 / 620	mW
Storage Temperature	$T_{stg}$	-65 to 150	$^\circ\text{C}$
Junction Temperature	$T_j$	150	$^\circ\text{C}$

- (1) Input voltage is the voltage should be allowed to apply to the input terminal independent of the magnitude of  $V^+$ .  
The normal operation will establish when any input is within the "Common-Mode Input Voltage Range" of electrical characteristics.
- (2) Input voltages below the negative supply voltage will be clamped by ESD protection diodes. If the input voltage lower than  $V^- - 0.3\text{V}$ , the input current must be limited 10 mA or less by using a restriction resistance.
- (3) The output terminal input voltage is limited at 7V.
- (4) Differential voltage is the voltage difference between +INPUT and -INPUT.
- (5) Short-circuit can cause excessive heating and destructive dissipation.
- (6) 2-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4).  
4-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4), internal Cu area: 74.2 mm × 74.2 mm.
- (7) 2-Layer: Mounted on glass epoxy board (101.5 mm × 114.5 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4) with exposed pad.  
4-Layer: Mounted on glass epoxy board (101.5 mm × 114.5 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4) with exposed pad.  
(For 4-layer: Applying 99.5 mm × 99.5 mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5.)

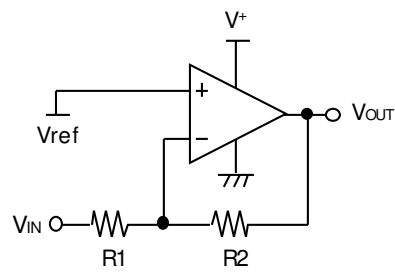
## ■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNIT
Supply Voltage	$V^+ - V^-$	-40 $^\circ\text{C}$ to 125 $^\circ\text{C}$	1.8 to 5.5	V
		-55 $^\circ\text{C}$ to 125 $^\circ\text{C}$	2.0 to 5.5	V
Input Voltage	$V_{IN}$	Closed-loop Gain $\geq 1$	$V^- - 0.3$ to $V^- + 5.5$	V
Operating Temperature	$T_{opr}$		-55 to 125	$^\circ\text{C}$

## ■ TYPICAL APPLICATIONS



Non-inverting amplifier



Inverting amplifier

## ■ ELECTRICAL CHARACTERISTICS

( $V^+ = 1.8$  to  $5.5V$ ,  $V^- = 0V$ ,  $V_{COM} = V^+ / 2$ ,  $R_L = 10k\Omega$  to  $V_{COM}$ ,  $T_a = 25^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT CHARACTERISTICS</b>						
Input Offset Voltage	$V_{IO}$	$V_{COM} = 0V$ to $V^+$	-	1	5	mV
Input Bias Current	$I_B$		-	1	-	pA
Input Offset Current	$I_{IO}$		-	1	-	pA
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	$T_a = -40^\circ C$ to $125^\circ C$	-	1	-	$\mu V/^\circ C$
Common-Mode Input Resistance	$R_{IC}$		-	1	-	$T\Omega$
Differential Input Resistance	$R_{ID}$		-	1	-	$T\Omega$
Input Capacitance	$C_{IN}$		-	5	-	pF
Open-Loop Voltage Gain	$A_V$	$V^+ = 5V$ , $R_L = 10k\Omega$ to $V^+ / 2$	68	90	-	dB
Common-Mode Rejection Ratio	CMR	$V^+ = 5.5V$ , $V_{COM} = V^- - 0.2V$ to $V^+ - 1.5V$	70	90	-	dB
		$V^+ = 5.5V$ , $V_{COM} = V^- - 0.2V$ to $V^+$	55	70	-	dB
		$V^+ = 1.8V$ , $V_{COM} = V^- - 0.2V$ to $V^+ + 0.2V$	50	65	-	dB
Common-Mode Input Voltage Range	$V_{ICM}$	CMR $\geq 50$ dB	$V^- - 0.2$	-	$V^+ + 0.2^{(8)}$	V
<b>OUTPUT CHARACTERISTICS</b>						
High-level Output Voltage	$V_{OH}$	$R_L = 10k\Omega$ to $V^+ / 2$	$V^+ - 0.025$	$V^+ - 0.010$	-	V
		$R_L = 2k\Omega$ to $V^+ / 2$	$V^+ - 0.100$	$V^+ - 0.050$	-	V
Low-level Output Voltage	$V_{OL}$	$R_L = 10k\Omega$ to $V^+ / 2$	-	6	25	mV
		$R_L = 2k\Omega$ to $V^+ / 2$	-	30	60	mV
		$R_L = 10k\Omega$ to $V^-$	-	0	5	mV
		$R_L = 2k\Omega$ to $V^-$	-	0	5	mV
Capacitive Load Drive	$C_L$		-	100	-	pF
Output Short-Circuit Current	$I_{SC}$	Sourcing, $V^+ = 5V$	-	40	-	mA
		Sinking, $V^+ = 5V$	-	60	-	mA
<b>POWER SUPPLY</b>						
Supply Current per Amplifier	$I_{SUPPLY}$	No signal, $V_{COM} = 0V$	-	55	76	$\mu A$
		NJU77550, NJU77551	-	50	70	$\mu A$
		NJU77552, NJU77554	-	50	70	$\mu A$
Supply Voltage Rejection Ratio	SVR	$V^+ = 1.8V$ to $5.5V$ , $V_{COM} = 0V$ or $V^+$	70	90	-	dB

(8)  $V^+ + 0.2V$  value is limited at  $5.5V$ .

## ■ ELECTRICAL CHARACTERISTICS [Continued]

( $V^+ = 1.8$  to  $5.5V$ ,  $V^- = 0V$ ,  $V_{COM} = V^+ / 2$ ,  $R_L = 10k\Omega$  to  $V_{COM}$ ,  $T_a = 25^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>AC CHARACTERISTICS (<math>V^+ = 5V</math>)</b>						
Slew Rate	SR	$C_L = 100pF$	-	0.8	-	V/ $\mu s$
Gain Bandwidth Product	GBW	$C_L = 100pF$	-	1.7	-	MHz
Settling Time	$t_s$	0.1%, $V^+ = 5V$ , $C_L = 100pF$	-	6.5	-	$\mu s$
Phase Margin	$\Phi_M$	$C_L = 10pF$	-	60	-	Deg
Total Harmonic Distortion + Noise	THD+N	Gain = +2, $f = 1kHz$ , $V_O = 1.5V_{rms}$	-	0.005	-	%
Equivalent Input Noise Voltage	$V_{NI}$	$f = 0.1Hz$ to $10Hz$	-	1.6	-	$\mu V_{PP}$
	$e_n$	$f = 1kHz$	-	24	-	$nV/\sqrt{Hz}$
Channel Separation	CS	$f = 1kHz$	-	120	-	dB

## ■ THERMAL CHARACTERISTICS

PACKAGE	SYMBOL	VALUE	UNIT
Junction-to-Ambient Thermal Resistance			
SOT-23-5	$\theta_{ja}$	260 / 192	°C/W
SC-88A		347 / 255	
SOP8		181 / 125	
MSOP8 (TVSP8)		245 / 184	
DFN8-U1 (ESON8-U1)		278 / 104 <sup>(7)</sup>	
SSOP14		250 / 202	
Junction-to-Top of Package Characterization Parameter			
SOT-23-5	$\psi_{jt}$	67 / 58	°C/W
SC-88A		91 / 73	
SOP8		49 / 43	
MSOP8 (TVSP8)		51 / 45	
DFN8-U1 (ESON8-U1)		42 / 25 <sup>(7)</sup>	
SSOP14		53 / 52	

(6) 2-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4).

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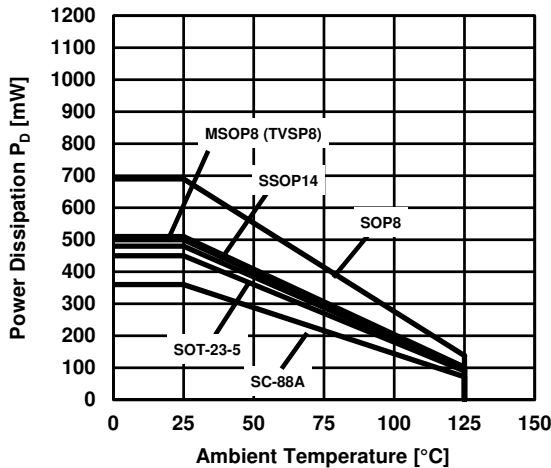
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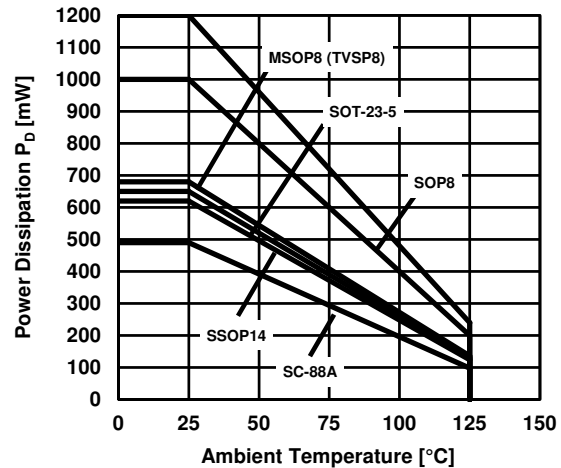
(For 4-layer: Applying 99.5 mm × 99.5 mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5.)

## ■ POWER DISSIPATION vs. AMBIENT TEMPERATURE

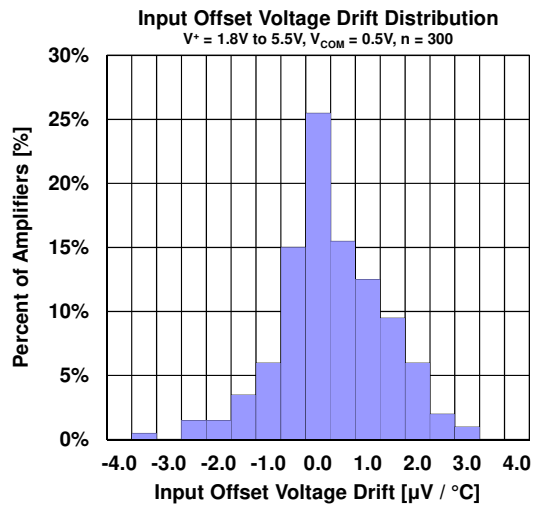
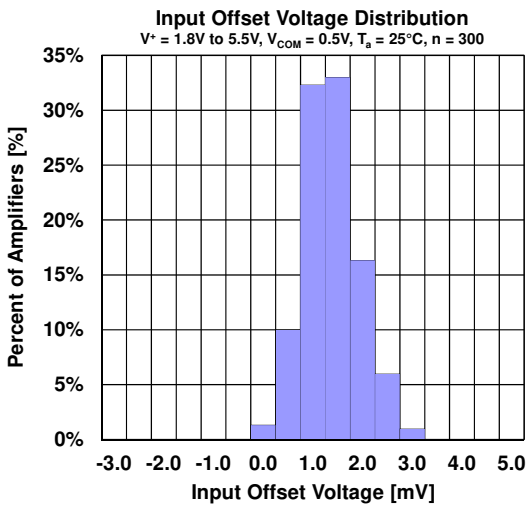
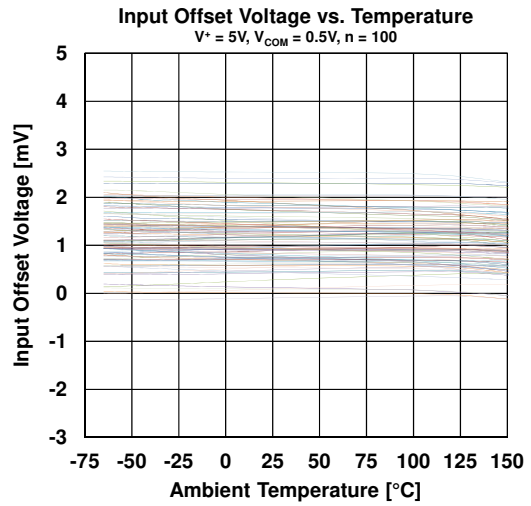
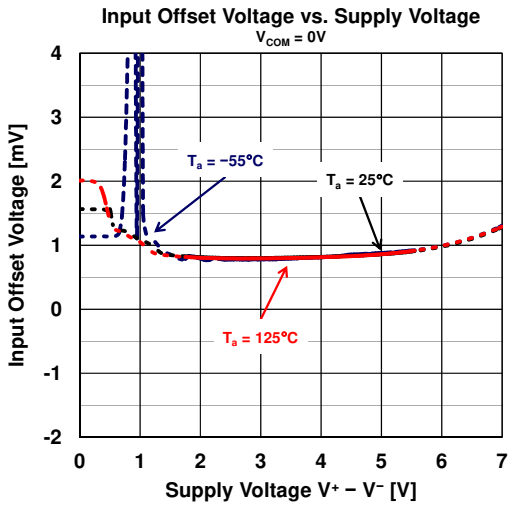
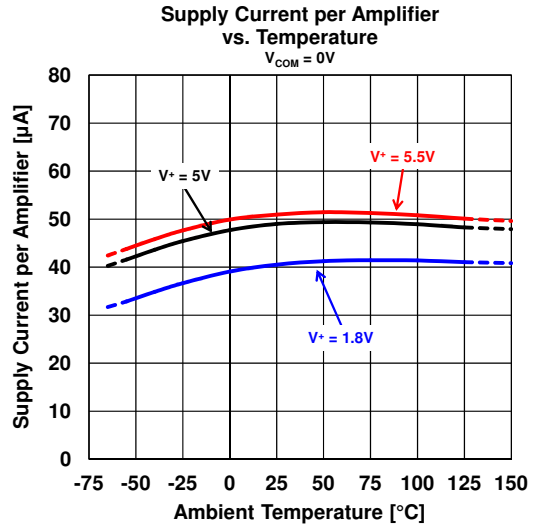
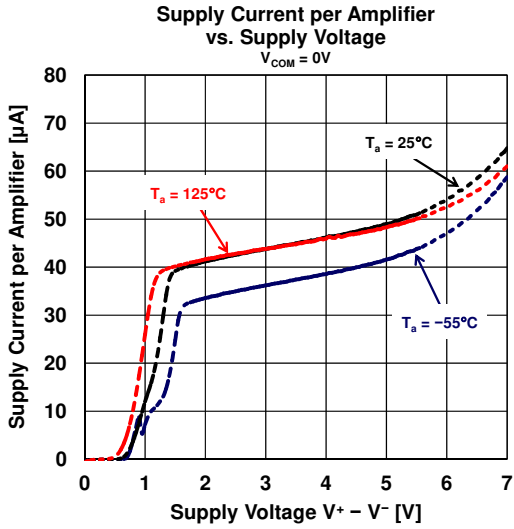
Power Dissipation vs. Temperature  
2-Layer



Power Dissipation vs. Temperature  
4-Layer

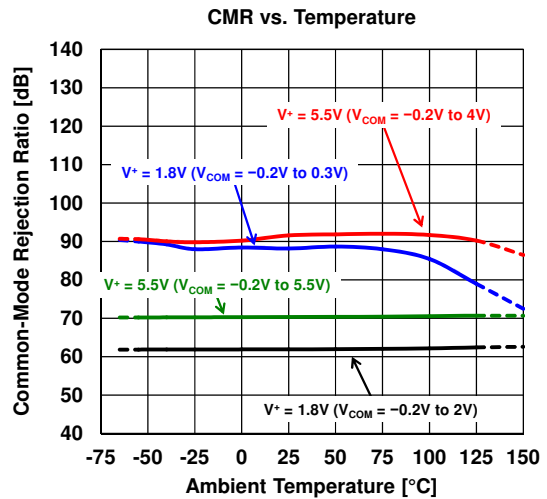
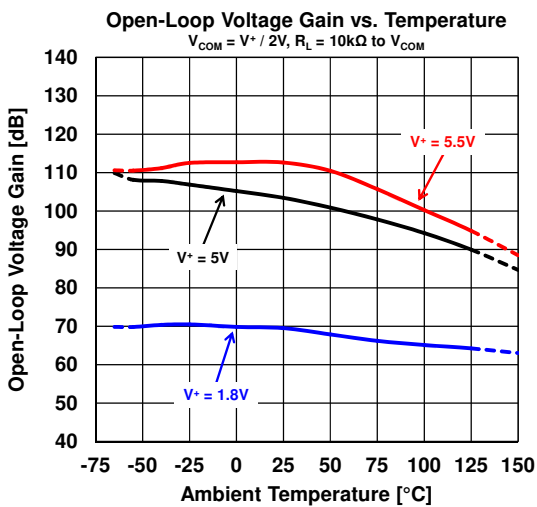
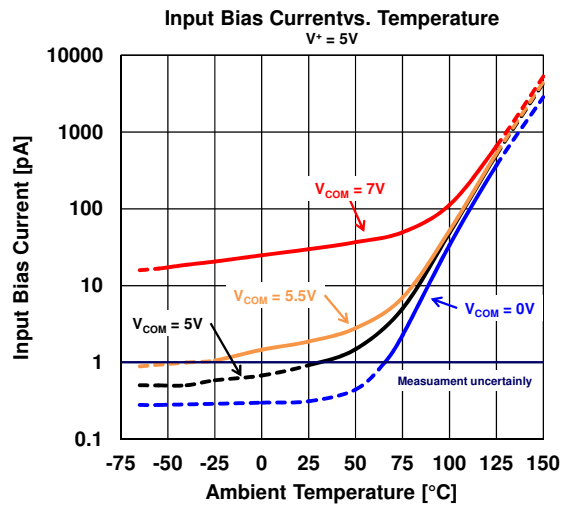
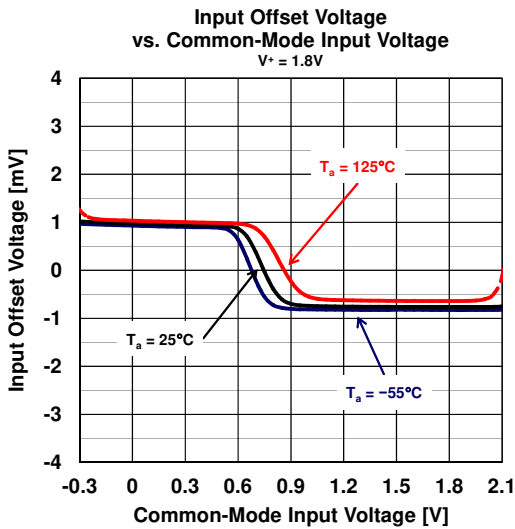
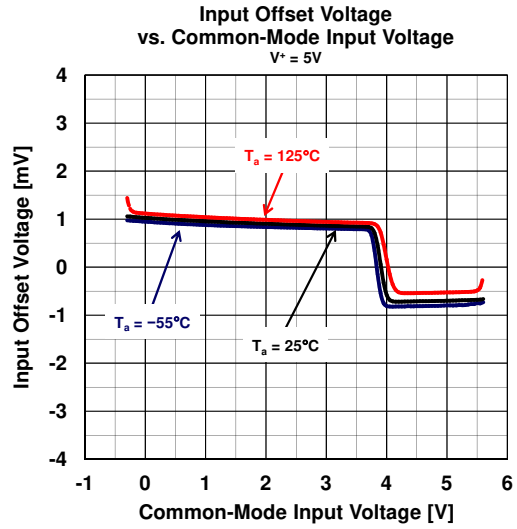
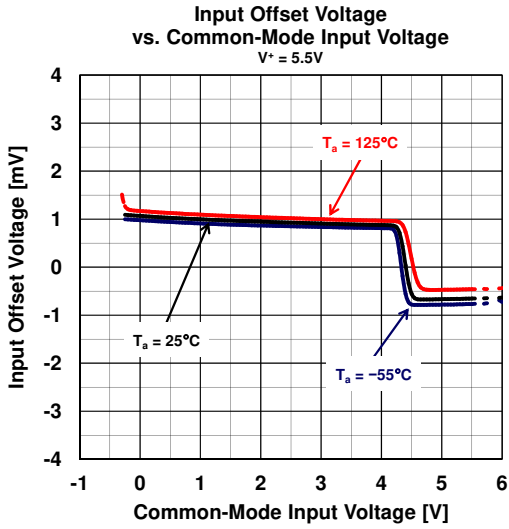


## ■ TYPICAL CHARACTERISTICS

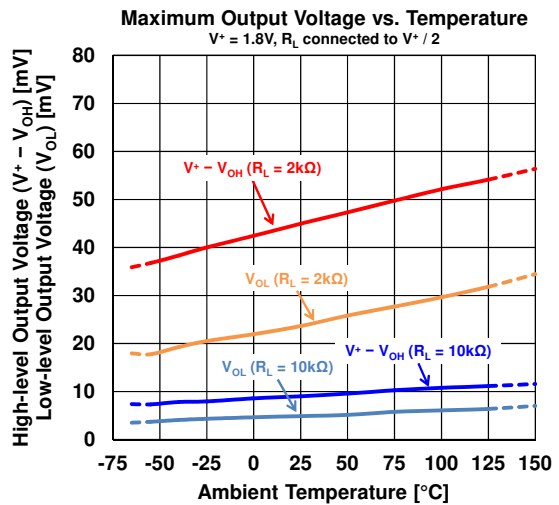
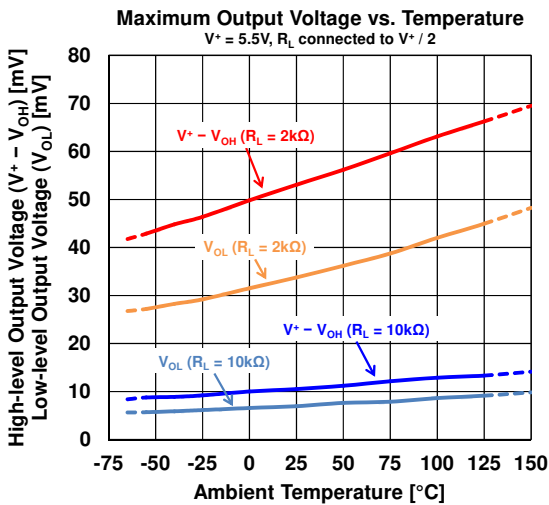
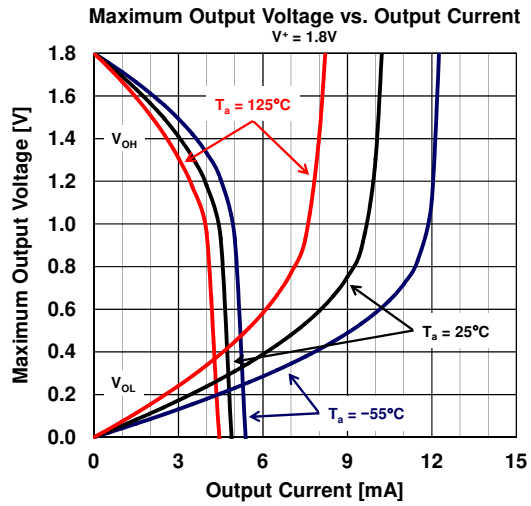
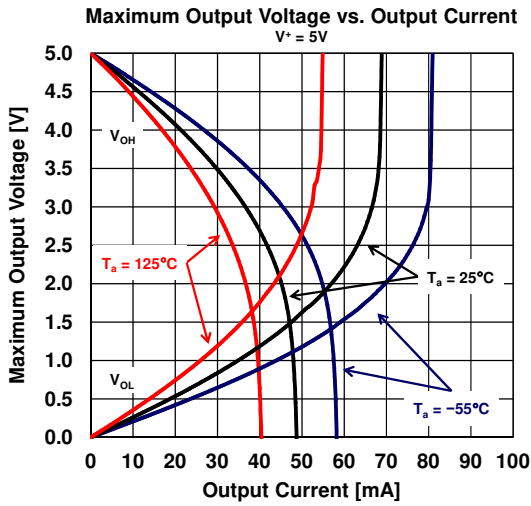
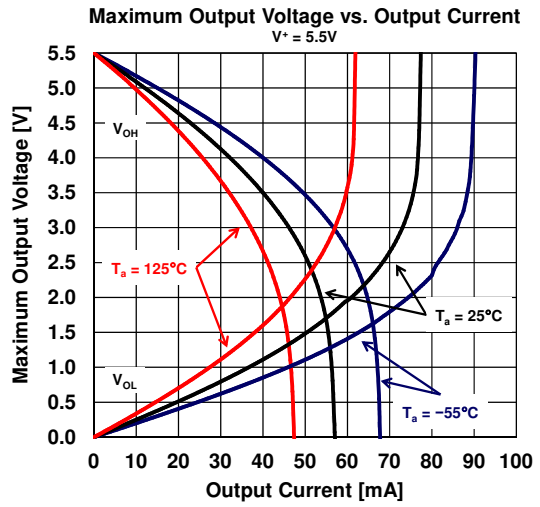
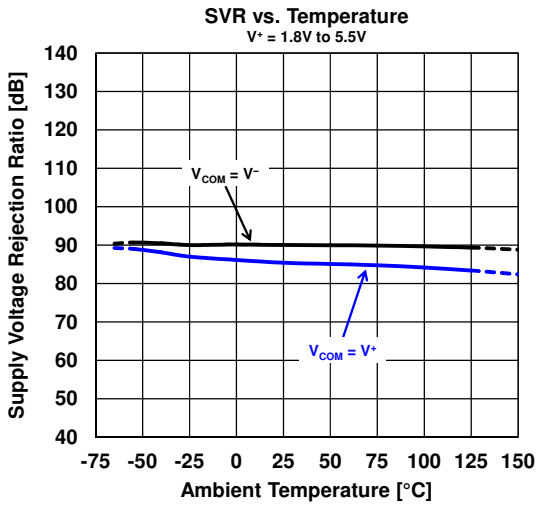




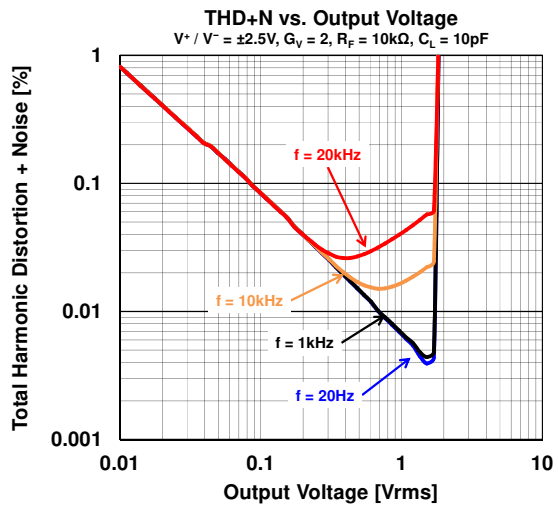
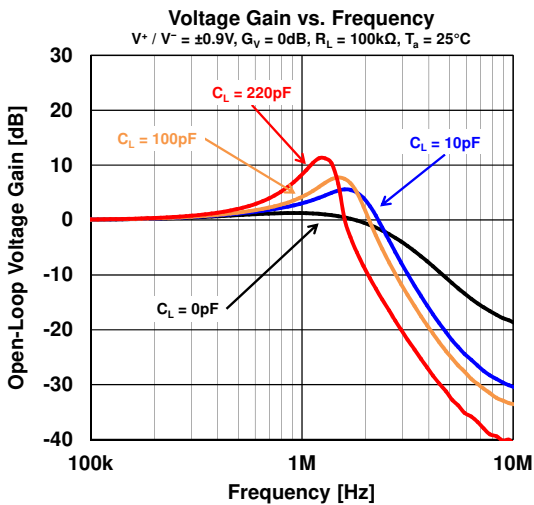
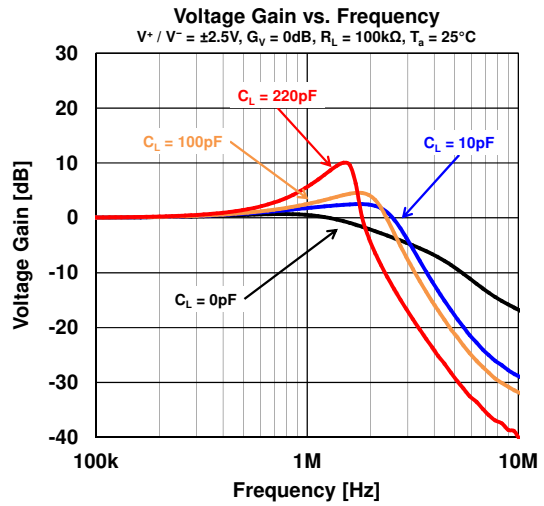
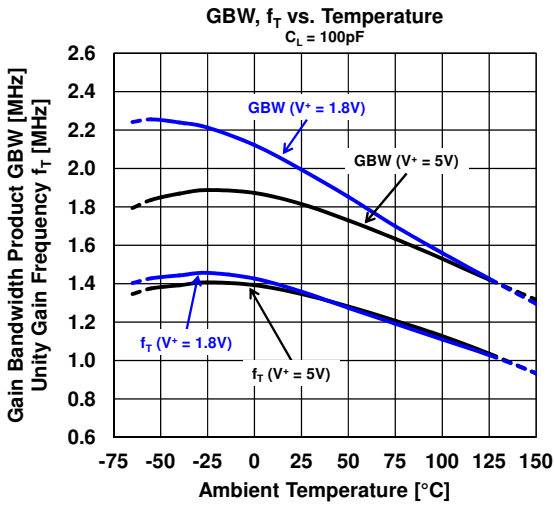
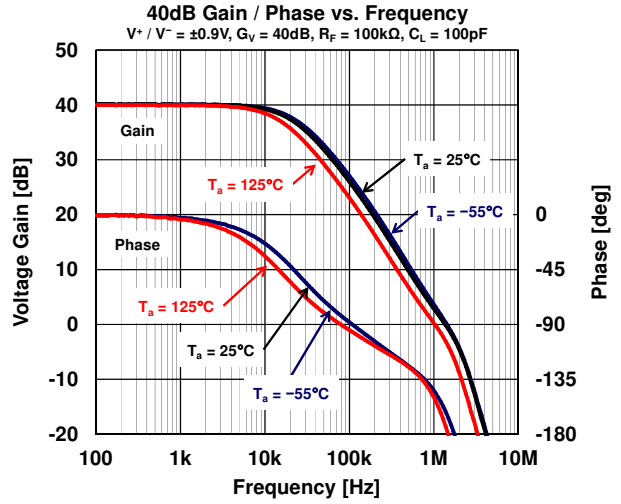
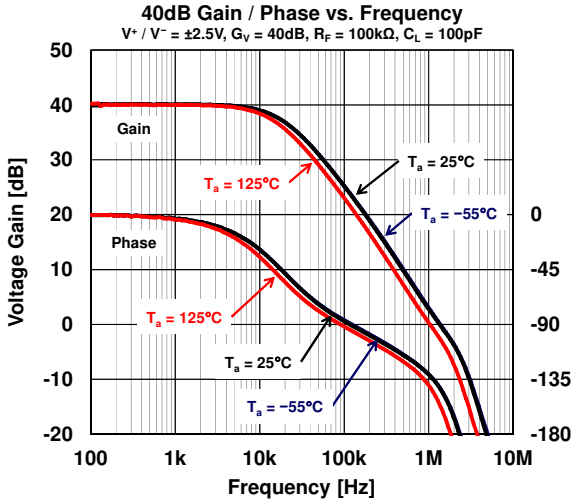
## ■ TYPICAL CHARACTERISTICS



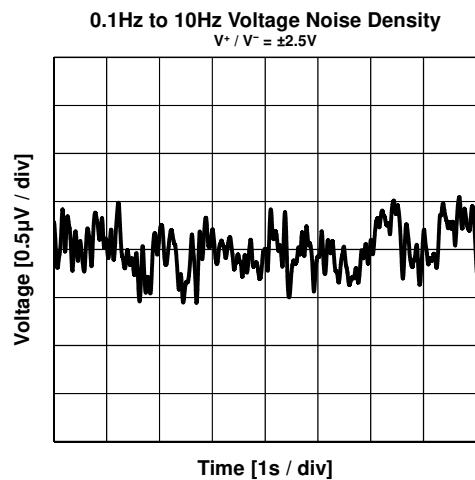
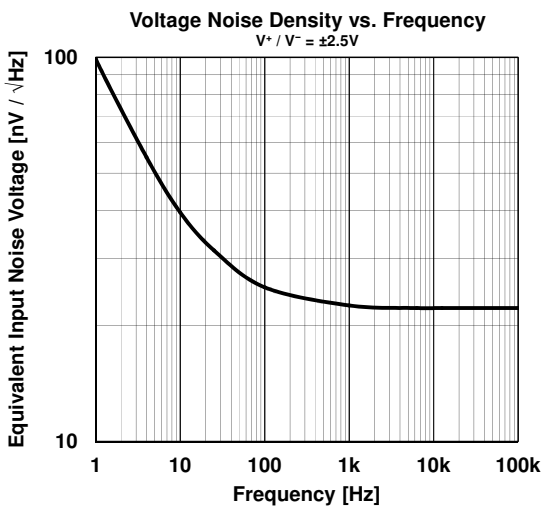
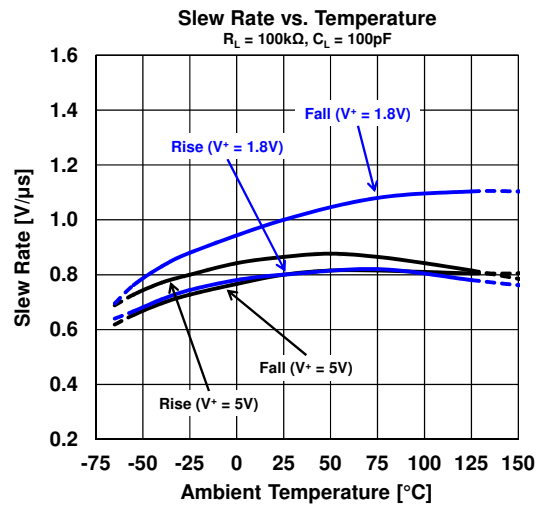
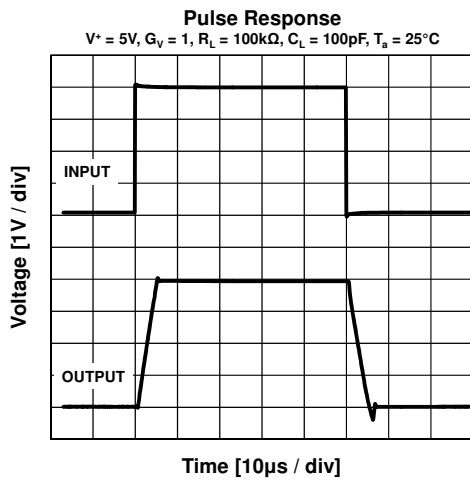
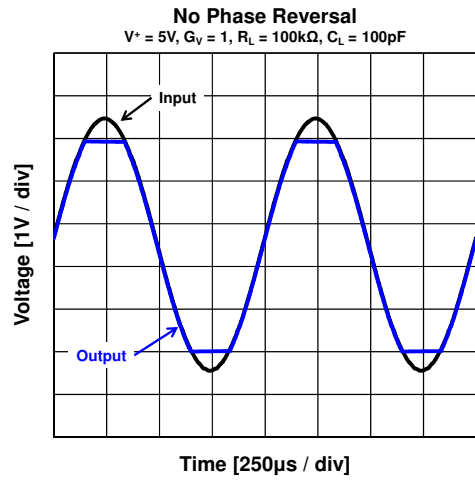
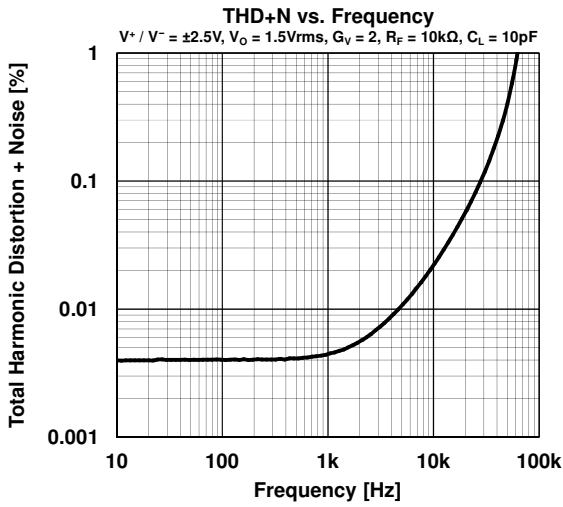
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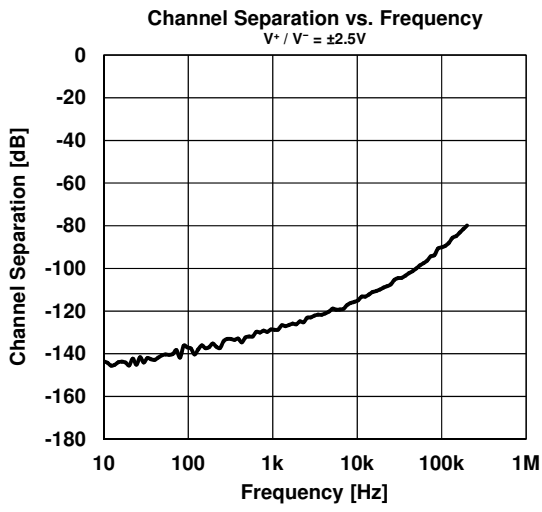
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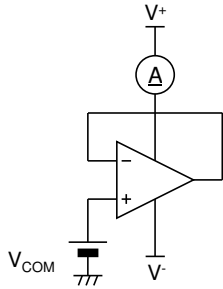


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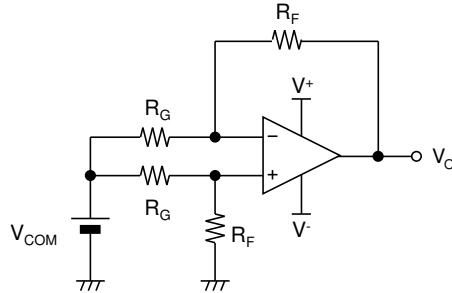
## ■ TEST CIRCUITS

- $I_{SUPPLY}$



- $V_{IO}, CMR, SVR$

$R_G = 50\Omega, R_F = 50k\Omega$



$$V_{IO} = \frac{R_G}{(R_G + R_F)} \times (V_O - V_{COM})$$

$$CMR = 20 \log \frac{\Delta V_{COM} \left(1 + \frac{R_F}{R_G}\right)}{\Delta V_O}$$

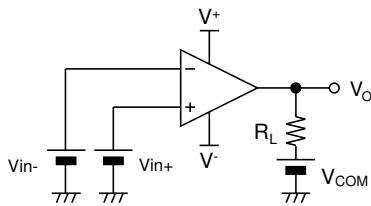
$$SVR = 20 \log \frac{\Delta V_s \left(1 + \frac{R_F}{R_G}\right)}{\Delta V_O}$$

$V_s = V^+ - V^-$

- $V_{OH}, V_{OL}$

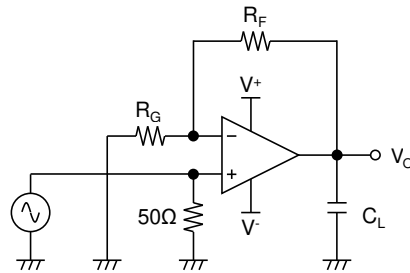
$V_{OH}: V_{in+} = 1V, V_{in-} = 0V, V_{COM} = V^+ / 2$

$V_{OL}: V_{in+} = 0V, V_{in-} = 1V, V_{COM} = V^+ / 2, V^-$



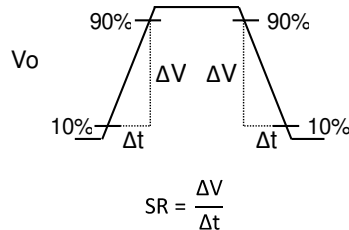
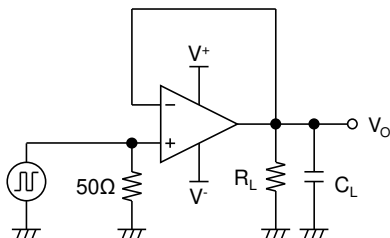
- GBW

$R_G = 1k\Omega, R_F = 100k\Omega$



- SR

$R_L = 100k\Omega$



## APPLICATION NOTE

### Single and Dual Supply Voltage Operation

The NJU7755x series works with both single supply and dual supply when the voltage supplied is between  $V^+$  and  $V^-$ . These amplifiers operate from single 1.8V to 5.5V supply and dual  $\pm 0.9V$  to  $\pm 2.75V$  supply. The power supply pin should have bypass capacitor (i.e. 0.1 $\mu$ F).

### No Phase Reversal

The NJU7755x series are designed to prevent phase reversal at the input voltage above the supply voltage. Figure1 shows no phase reversal characteristics with the input voltage exceeding the supply voltage.

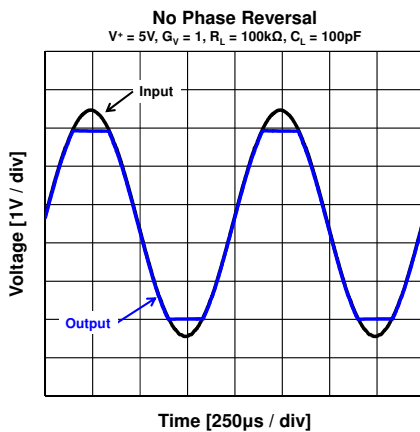


Figure1. No phase reversal

### Power-on Time

The NJU7755x series typically require a power-on time of 20 $\mu$ s (Figure2). Power-on time depends on the supply voltage, bypass capacitor, impedance of supply source and impedance other devices. While settling time, IC is unstable, such as output voltage, input offset voltage and slew rate.

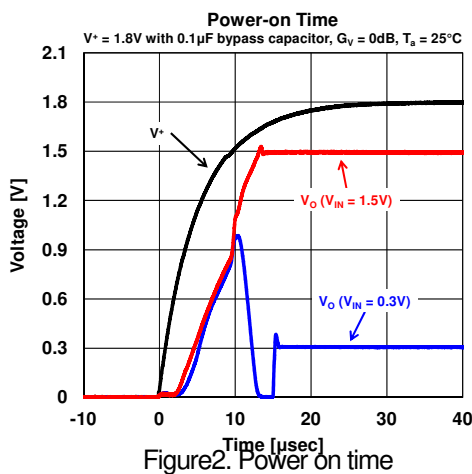


Figure2. Power on time

### Rail-to-Rail Input

The input stage of NJU7755x series has two input differential pairs, PMOS and NMOS (Figure3). When the common-mode input voltage is from 200mV below the negative supply voltage to the typically  $(V^+) - 1.3V$ , the PMOS pair is active. When the common-mode input voltage close to the positive supply, typically  $(V^+) - 1.3V$  to 200mV above positive supply, the NMOS pair is active. In the transition region, the performance of offset voltage, as shown in figure4, offset voltage drift, CMR, SVR and THD is slightly degraded.

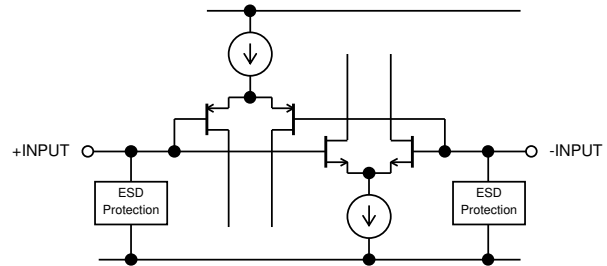


Figure3. Simplified Schematic of Input Stage

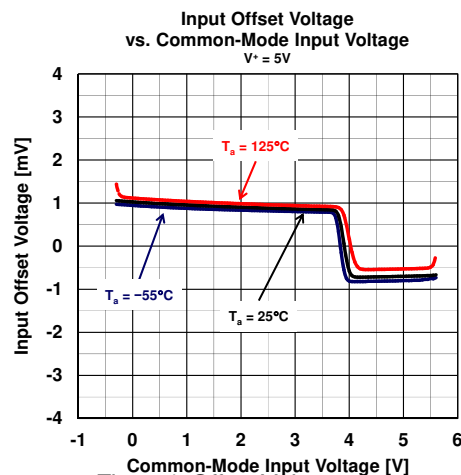


Figure4. Offset Voltage change with common-mode input voltage.

For the best performance design is inverting amplifier shown in Figure5. Inverting amplifier has a constant common-mode voltage equal to  $V_{ref}$ . If  $V_{ref}$  voltage is constant and is chosen to avoid transition region, output will be best linearity performance.

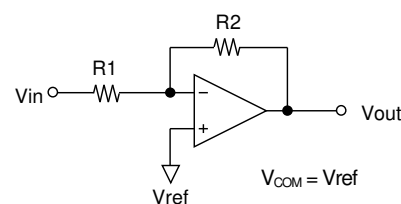


Figure5. Inverting Amplifier

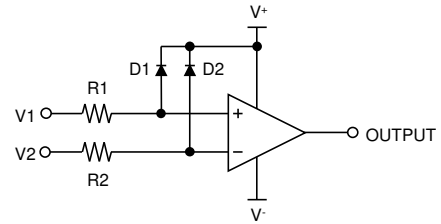
## APPLICATION NOTE

### Input Tolerant

In general, common OpAmp is protected by internal ESD diode that is connected from input pin to both the positive and negative power supply. In a buffer configuration, when input exceeds either supply voltage, ESD diode will be forward biased and current. If the current is high enough, even when input current over long periods of time or even short periods of time, can shift the electrical characteristics beyond the data sheet's guaranteed limits, or cause a permanent failure of the op amp.

The input of the NJU7755x series has an ESD protection as shown in Figure 3. The input bias current is minimized in the input voltage even in operating voltage range and exceeding the  $V^+$  supply, and the OpAmp is protected from overvoltage current (Figure6).

The maximum input voltage is absolute maximum rating of  $V^- + 7V$ , but usually recommend design so that the input voltage is up to  $V^- + 5.5V$ .

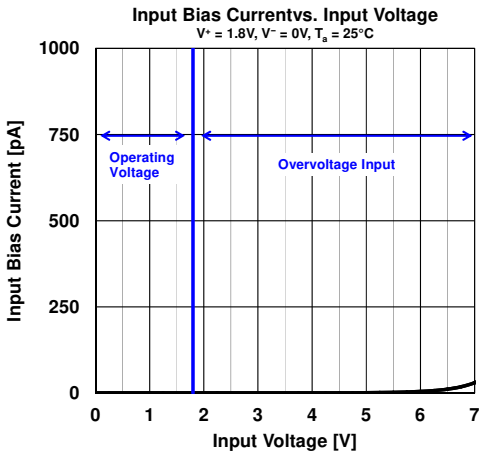


$$(R1, R2) > \frac{V^-(V1, V2)}{10mA}$$

$$(R1, R2) > \frac{(V1, V2) - V^+}{I_F}$$

$I_F$ : Forward current of external diode.

Figure7. Example of input protection



### Power Supply Protection for Overvoltage Condition

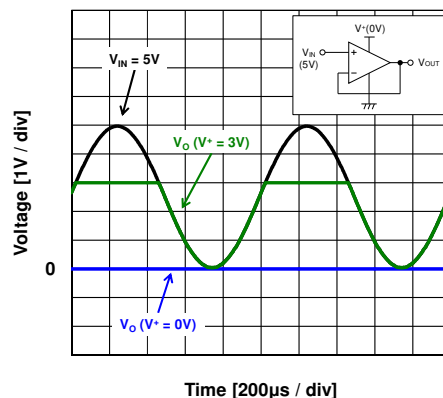
In general, many power supplies cannot sink current. If nothing within the circuit can sink the overvoltage current, if the overvoltage occurs with the supplies powered on, in the ESD diode protection OpAmp, the supply voltage can exceed the intended operating voltage of the system. Even if the overvoltage occurs with the system powered off, the overvoltage current can unintentionally power up the OpAmp or system. NJU7755x series prevents the positive overvoltage current flowing from input pin to positive supply pin, prevents rising the supply voltage, and prevents malfunctioning with OpAmp or system. Figure8 shows the output voltage when applying 5V peak to peak overvoltage to the input pin when the power supply  $V^+$  is 0V, 3V. Due to the input tolerant, the output voltage is clamped at  $V^+$  (0V, 3V).

NJU7755x series protects the input pin from overvoltage by shunting the overvoltage current to the  $V^-$  supply rail. When the input voltage for  $V^- - 0.3V$  to  $V^- + 7V$ , the ESD protection is not activate and minimize the input bias current (Figure6).

For the input voltage 300mV below the negative supply voltage, the ESD protection operates to protect the input terminal. At this moment, the current flowing in protection element is allowed up to 10 mA.

Momentary voltages above  $V^- + 7V$ , the ESD protection also activate, and clamp inputs, but cannot protect against overvoltage excepting ESD.

In some applications, it may be necessary to prevent excessive overvoltage. Figure6 is example to protect input transistors. The external resistors  $R1, R2$  limit the current through external diodes  $D1, D2$ .





## APPLICATION NOTE

### Power Supply Protection for Overvoltage Condition (Continues)

Input tolerant can be applied to the input buffer of the ADC (Figure9).

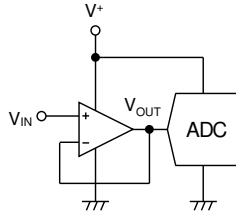
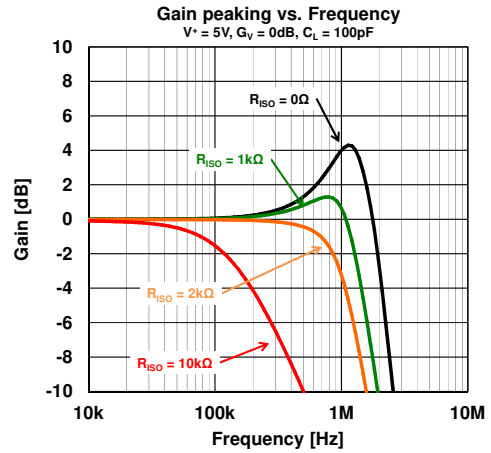


Figure9. ADC buffer with input tolerant



### Capacitive Load

The NJU7755x series can use at unity gain follower, but the unity gain follower is the most sensitive configuration to capacitive loading. The combination of capacitive load placed directly on the output of an amplifier along with the output impedance of the amplifier creates a phase lag which in turn reduces the phase margin of the amplifier.

If phase margin is significantly reduced, the response will cause overshoot and ringing in the step response.

The NJU7755x series is unity gain stable for capacitive loads of 100pF. To drive heavier capacitive loads, an isolation resistor,  $R_{ISO}$  as shown Figure10, should be used.  $R_{ISO}$  improves the feedback loop's phase margin by making the output load resistive at higher frequencies. The larger the value of  $R_{ISO}$ , the more stable the output voltage will be. However, larger values of  $R_{ISO}$  result in reduced output swing, reduced output current drive and reduced frequency bandwidth (Figure11).

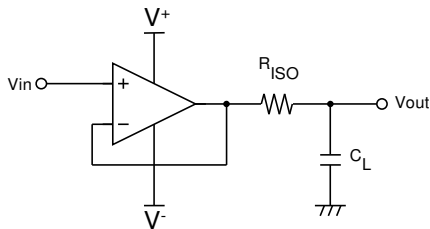
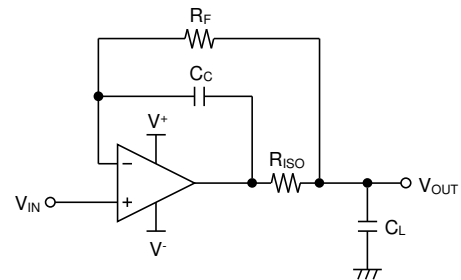


Figure10. Isolating capacitive load

Figure12 shows the isolation circuit with  $R_{ISO}$ ,  $R_F$  and  $C_C$ . Minimize the effect of voltage drop due to  $R_{ISO}$  and output current.



$$10R_{ISO}C_L < R_F C_C$$

$$R_{ISO} \text{ is more than } 300\Omega$$

Figure12. Isolating capacitive load with  $R_{ISO}$ ,  $R_F$  and  $C_C$

### Terminating unused OpAmps

Examples of common methods of terminating an uncommitted OpAmp are shown in Figure13. Improper termination can be result increase supply current, heating and noise in OpAmps.

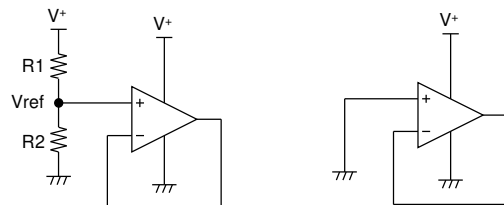
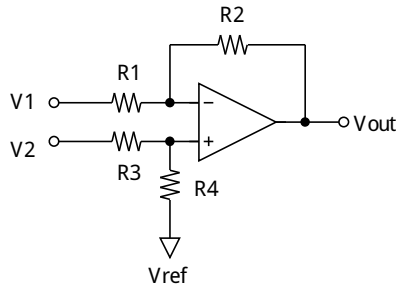


Figure13. Terminating unused OpAmps

## APPLICATION NOTE

### Differential Amplifier

Figure15 shows a one OpAmp differential amplifier that consists of the single OpAmp and four external resistors. Differential amplifier amplifies the difference between its two input pins, and rejects the common-mode input voltage at both input pins. This is used in variety of applications including current sensing, differential to single-end converter, isolation amplifier to remove common-mode noise.



$$V_{out} = \left( \frac{R1+R2}{R3+R4} \right) \frac{R4}{R1} V2 - \frac{R2}{R1} V1 + \left( \frac{R1+R2}{R3+R4} \right) \frac{R3}{R1} V_{ref}$$

$$R1 = R3, R2 = R4$$

$$V_{out} = \frac{R2}{R1} (V2 - V1) + V_{ref}$$

Figure15. Differential Amplifier

The differential amplifier's common-mode rejection ratio (CMR) is primarily determined by resistor mismatches, not by the OpAmp's CMR. Ideally, the resistors are chosen such that  $R2/R1 = R4/R3$ . The CMR due to the resistors in differential amplifier can be calculated using the below formula:

$$CMR_{R\_error} \approx 20 \log \left( \frac{1 + \frac{R2}{R1}}{4R_{error}} \right)$$

$CMR_{R\_error}$  = CMR due only to the resistors

$R_{error}$  = Resistor's tolerance

Example:

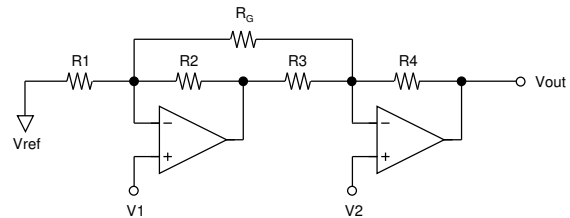
$R2 / R1 = 1$  and  $R_{error} = 0.1\%$ , then  $CMR = 54dB$

$R2 / R1 = 1$  and  $R_{error} = 1\%$ , then  $CMR = 34dB$

If using resistors with 1% tolerance and gain = 1, the CMR will only be 34dB.

### Instrumentation Amplifier

The instrumentation amplifier is suitable for requiring high input impedance and high common mode noise rejection at high gains. Figure16 and Figure17 is instrumentation amplifier using two or three OpAmp. Supply the reference voltage ( $V_{ref}$ ) with a low impedance source to keep accuracy.

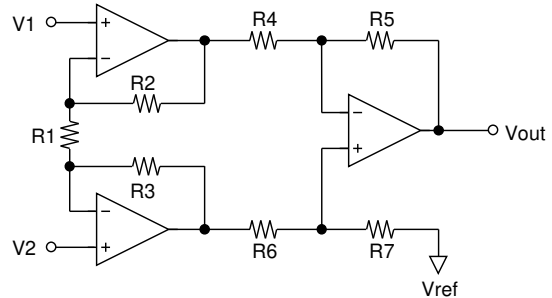


$$V_{out} = \left( 1 + \frac{R4}{R3} + \frac{2R4}{Rg} \right) (V2 - V1) + V_{ref}$$

$$R1 = R4, R2 = R3$$

$$CMR_{R\_error} \approx 20 \log \left( \frac{1 + \frac{R4}{R3} + \frac{2R4}{Rg}}{4R_{error}} \right)$$

Figure16. Instrumentation Amplifier with two OpAmp



$$V_{out} = \left( 1 + \frac{2R2}{R1} \right) \left( \frac{R5}{R4} \right) (V2 - V1) + V_{ref}$$

$$R2 = R3, R4 = R6, R5 = R7$$

$$CMR_{R\_error} \approx 20 \log \left( \frac{R1 + 2R2}{R1} \times \frac{1 + \frac{R5}{R4}}{4R_{error}} \right)$$

Figure17. Instrumentation Amplifier with three OpAmp

## APPLICATION NOTE

### Current Sensing

Current sensing applications are one such application in a wide range of electronic applications and mostly used for feedback control systems, including power metering battery life indicators and chargers, over-current protection and supervising circuit, automotive, and medical equipment. In such applications, it is desirable to use a shunt with very low resistance to minimize the series voltage drop and minimizes wasted power, and allows the measurement of high current. The NJU7755x series is ideal for these current sensing applications.

Figure18 shows a high-side current sensing circuit, and Figure19 shows a low-side current sensing circuit. The NJU7755x series has rail-to-rail input and output characteristics, thus allows the both of high-side and low-side current sensing circuit. Futuremore, low supply current of 50 $\mu$ A/ch can save the power at battery applications.

The differential amplifier's common-mode rejection ratio (CMR) is primarily determined by resistor mismatches. For details, refer to differential amplifiers in the application note.

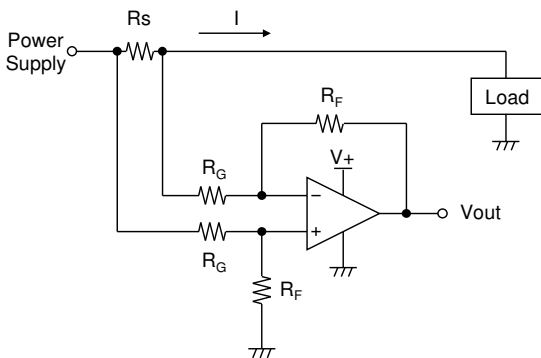


Figure18. High-Side Current Sensing

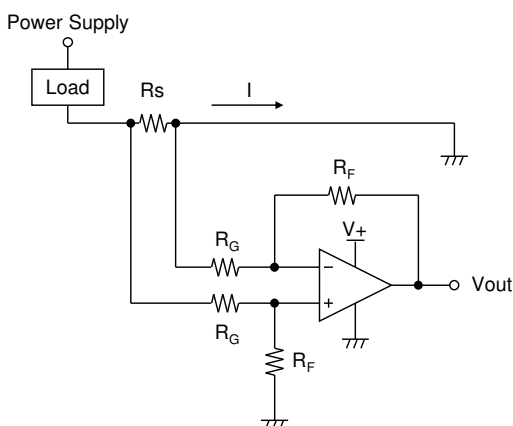
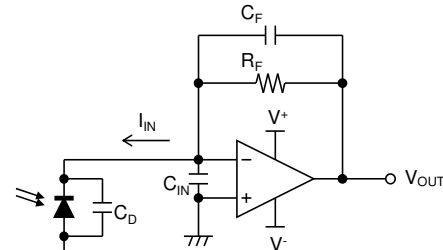


Figure19. Low-Side Current Sensing

### Transimpedance Amplifier

The features high input impedance with CMOS input and low power can be used for transimpedance amplifier applications shown in Figure20. The output voltage of amplifier is given by the equation  $V_{OUT} = I_{IN} \cdot R_F$ . Since the output voltage swing of amplifier is limited,  $R_F$  should be selected such that all possible values of  $I_{IN}$  can be detected.



$C_D$ : photodiode capacitance  
 $C_{IN}$ : OpAmp input capacitance

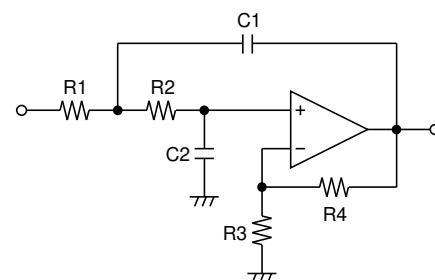
Figure20. Transimpedance amplifier

The  $C_D$ ,  $C_{IN}$  and  $R_F$  generate a phase lag which causes gain-peaking and can destabilized circuit. The essential component for obtaining a maximally flat response is a feedback capacitor  $C_F$ .  $C_F$  is usually added in parallel with  $R_F$  to maintain circuit stability and to control the frequency response. To maximally flat, 2nd order response,  $R_F$  and  $C_F$  should be chosen by using below equation.

$$C_F = \sqrt{\frac{C_{IN} + C_D}{GBW \times 2\pi \times R_F}}$$

### Sallen-Key 2nd-Order Active Low-Pass Filter

The Sallen-Key 2nd-order active low-pass filter is shown in Figure21. It can be used for a multiple pole filter required high attenuation.



$$R = R1 = R2, \quad C = C1 = C2$$

Q: Quality factor,  $G_{DC}$ : DC Gain

$$f_{3dB} = \frac{1}{2\pi RC}, \quad Q = \frac{1}{3 - G_{DC}}, \quad G_{DC} = 1 + \frac{R4}{R3} = 3 - \frac{1}{Q}$$

Figure21. Sallen-Key 2nd-Order Low-Pass Filter

## ■ APPLICATION NOTE

### EMIRR (EMI Rejection Ratio) Definition

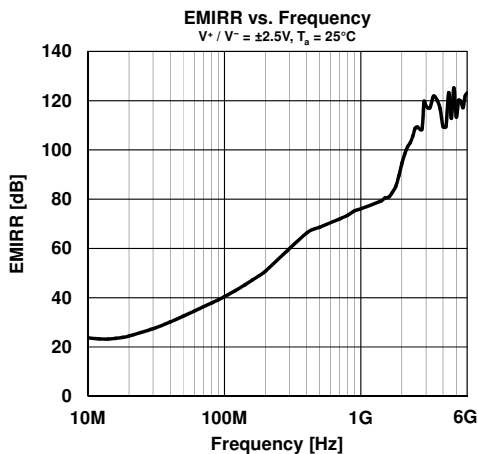
EMIRR is a parameter indicating the EMI robustness of an OpAmp. The definition of EMIRR is given by the following equation1.

$$EMIRR = 20 \cdot \log \left( \frac{V_{RF\_PEAK}}{|\Delta V_{IO}|} \right) \quad \text{--- eq.1}$$

$V_{RF\_PEAK}$ : RF Signal Amplitude [V<sub>p</sub>]

$\Delta V_{IO}$ : Input offset voltage shift quantity [V]

The tolerance of the RF signal can be grasped by measuring an RF signal and offset voltage shift quantity. Offset voltage shift is small so that a value of EMIRR is big. And it understands that the tolerance for the RF signal is high. In addition, about the input offset voltage shift with the RF signal, there is the thinking that influence applied to the input terminal is dominant. Therefore, generally the EMIRR becomes value that applied an RF signal to +INPUT terminal.

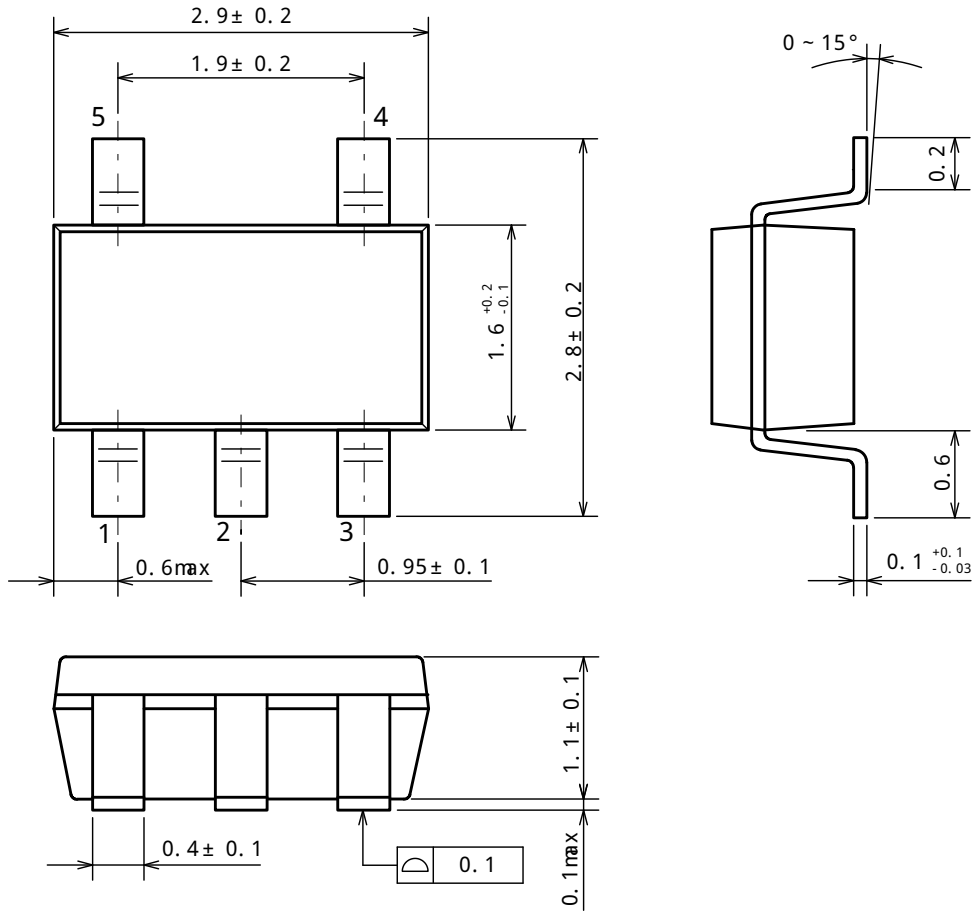


\*For details, refer to "Application Note for EMI Immunity" in our HP: <http://www.njr.com/>

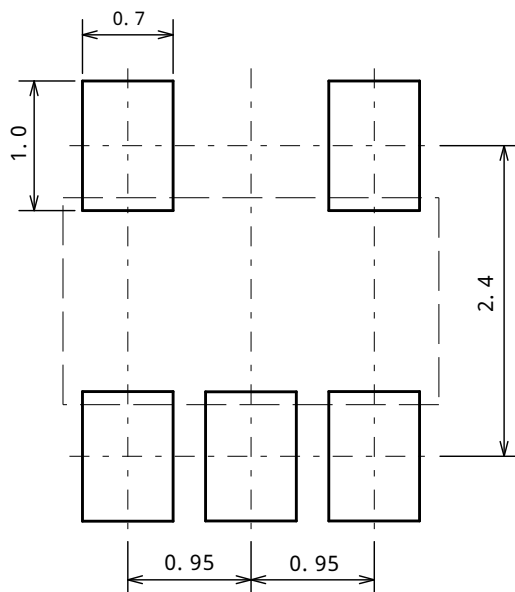
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Unit: mm

### ■ PACKAGE DIMENSIONS



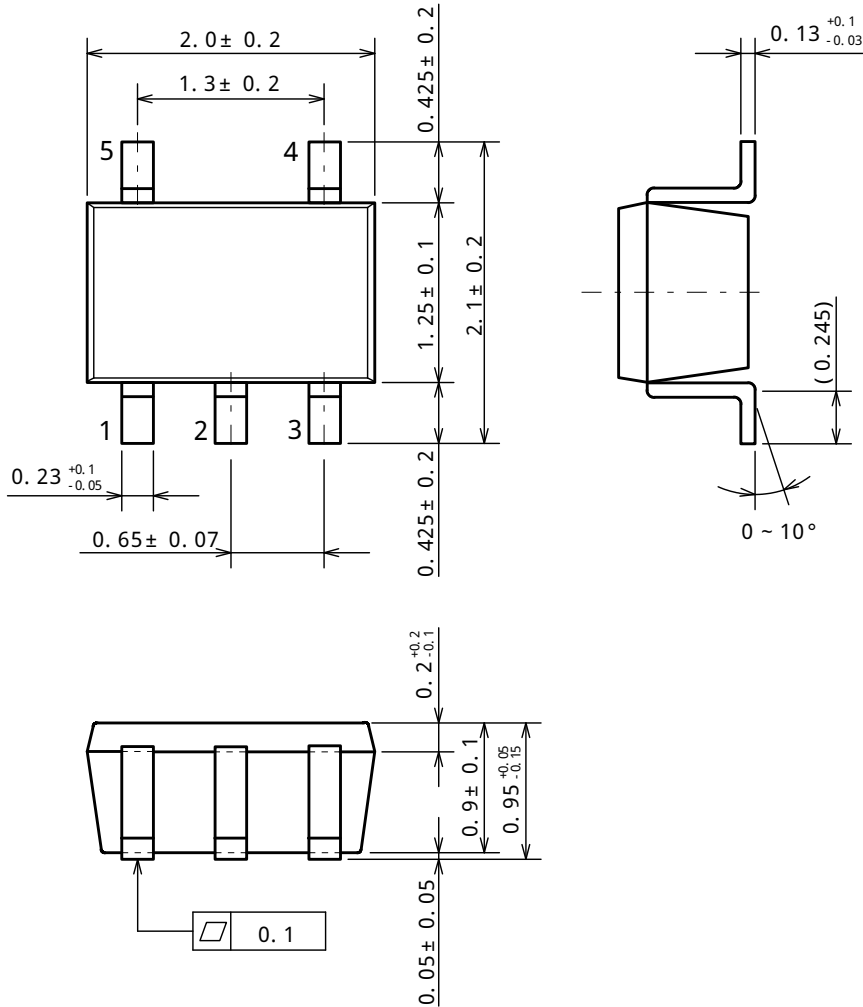
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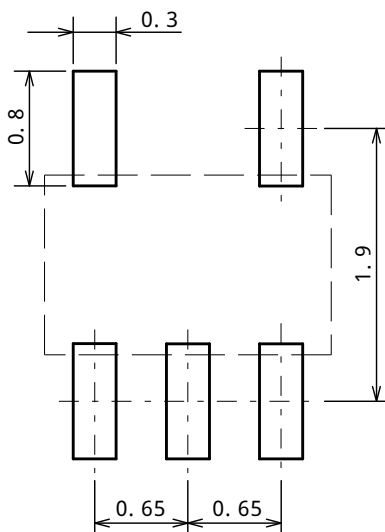
## SC-88A

Unit: mm

### ■ PACKAGE DIMENSIONS



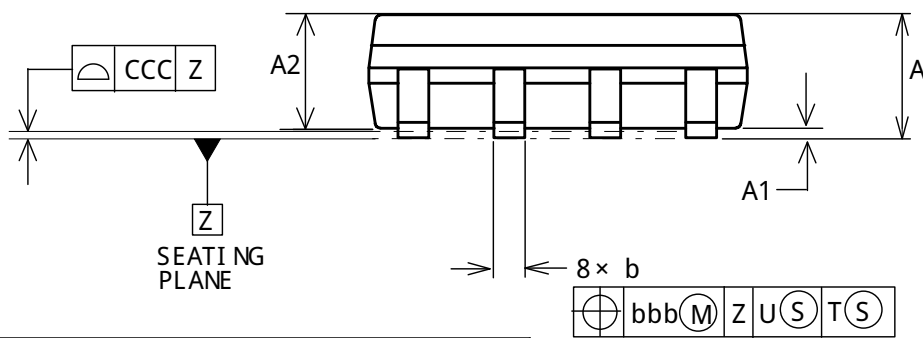
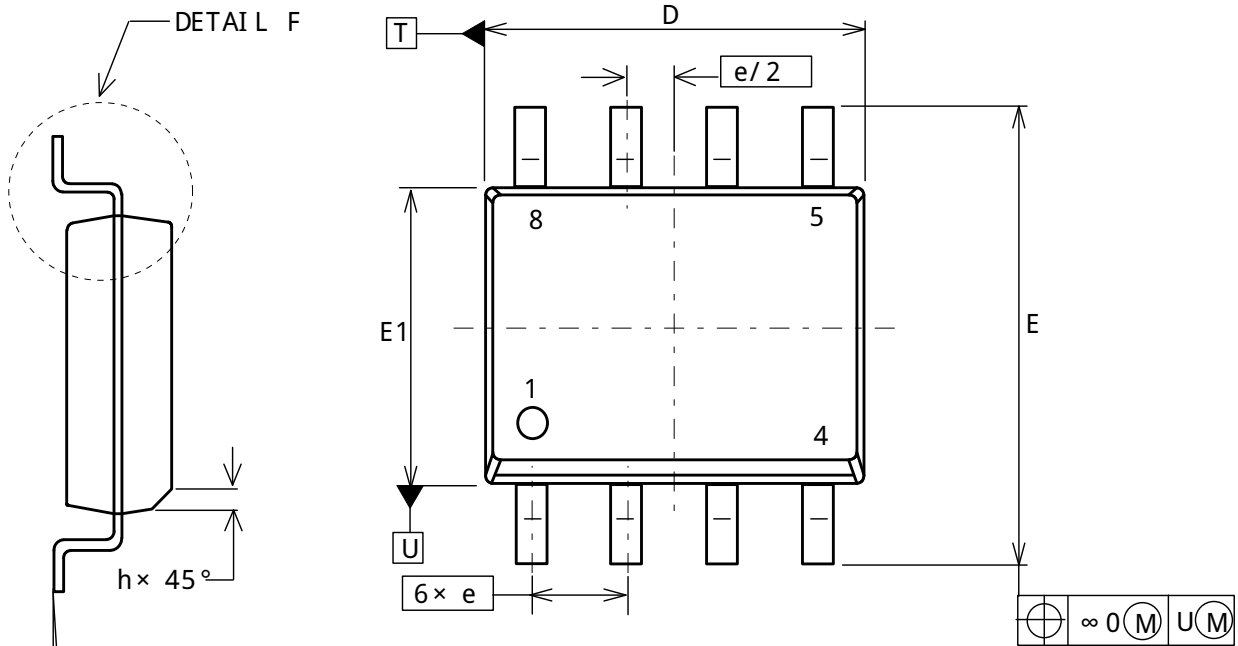
### ■ EXAMPLE OF SOLDER PADS DIMENSIONS



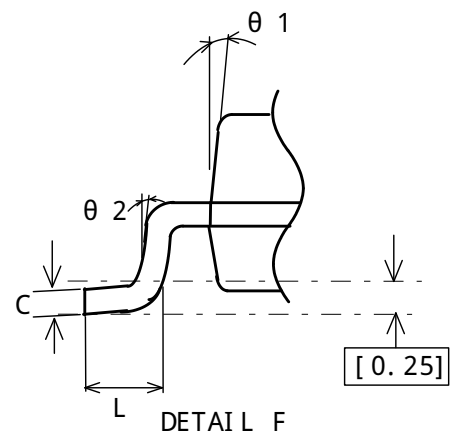
## SOP8

Unit: mm

### PACKAGE DIMENSIONS



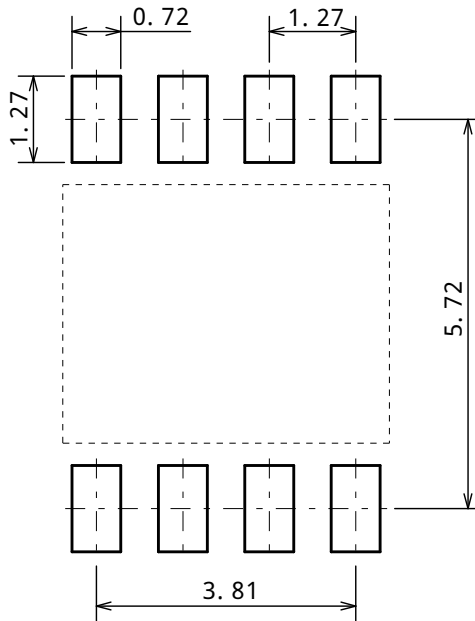
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		MIN	NCM	MAX	MIN	NCM	MAX
TOTAL THICKNESS	A	.053		.069	1.35		1.75
STAND OFF	A1	.004		.010	0.10		0.25
MOLD THICKNESS	A2	.049		-	1.25		-
LEAD WIDTH	b	.014		.019	0.35		0.49
L/F THICKNESS	C	.007		.010	0.19		0.25
BODY SIZE	D	.189		.197	4.80		5.00
	E1	.150		.157	3.80		4.00
LEAD PITCH	E	.228		.244	5.80		6.20
	e	.050 BSC			1.27 BSC		
	L	.015		.049	0.40		1.25
	h	.010		.020	0.25		0.50
	$\theta$	0°		7°	0°		7°
	$\theta 1$	5°		15°	5°		15°
	$\theta 2$	2°	7°	12°	2°	7°	12°
LEAD EDGE OFFSET	$\infty O$	.010			0.25		
LEAD OFFSET	bbb	.010			0.25		
COPLANARITY	CCC	.004			0.10		



## SOP8

Unit: mm

### ■ EXAMPLE OF SOLDER PADS DIMENSIONS

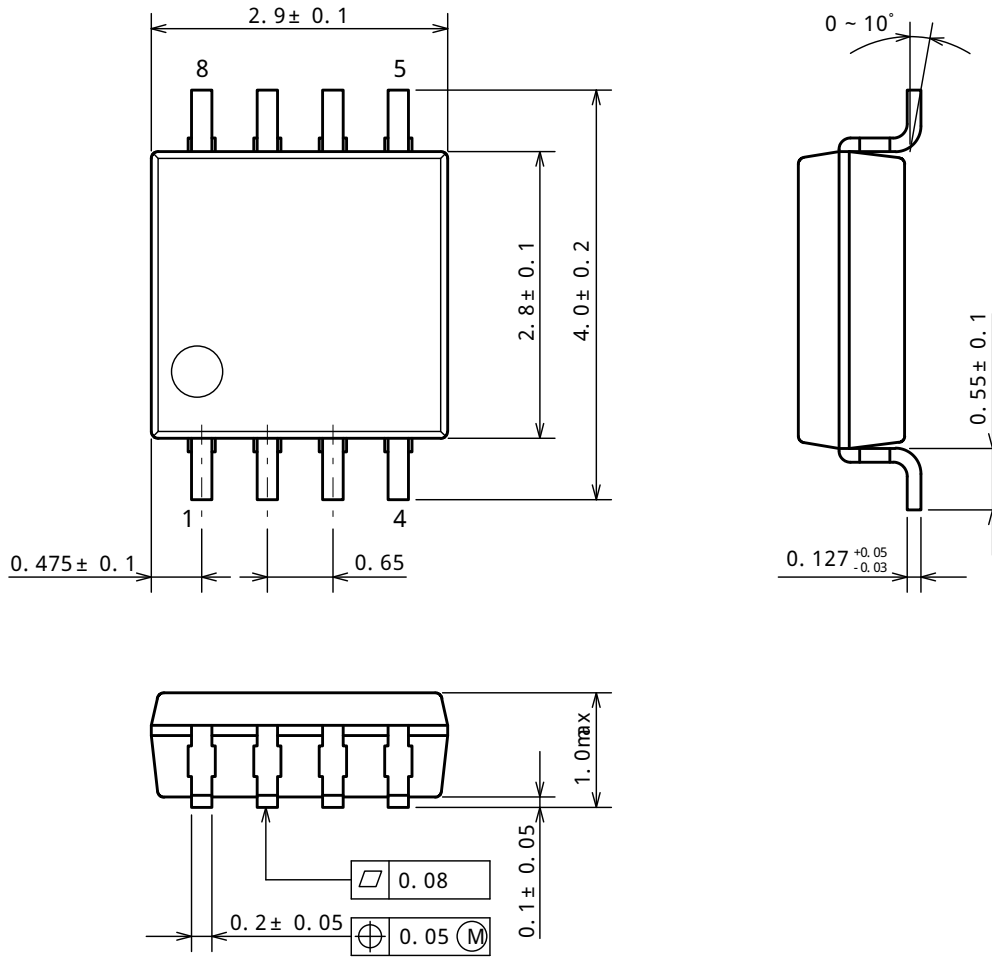




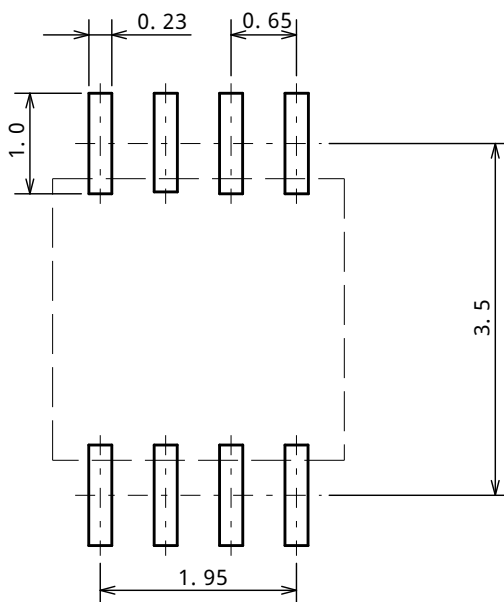
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Unit: mm

### ■ PACKAGE DIMENSIONS



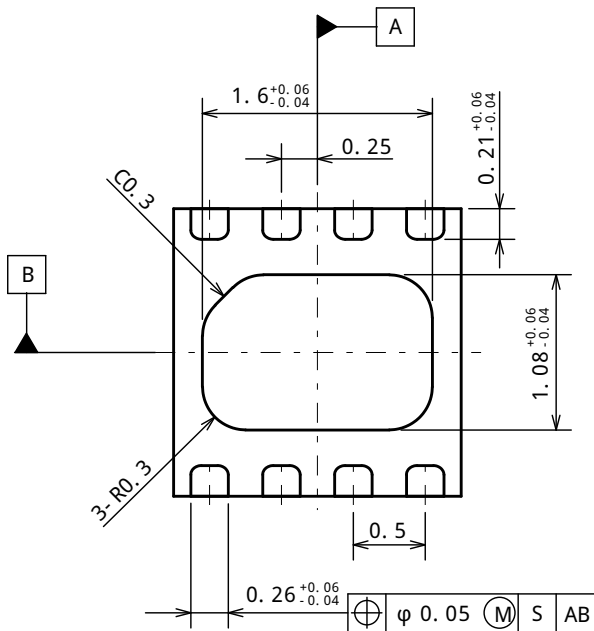
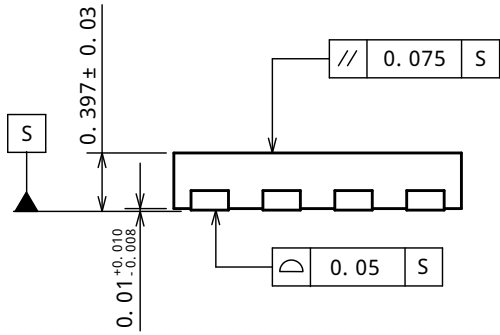
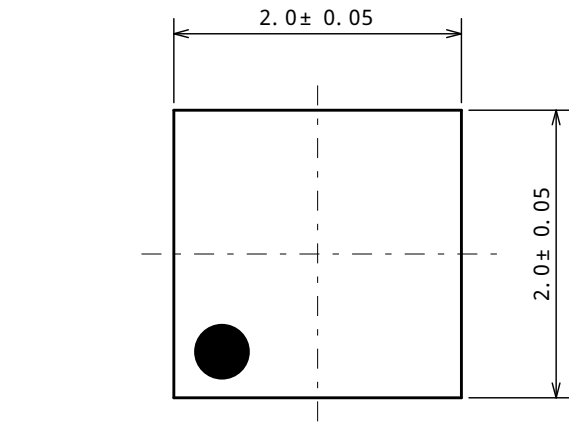
### ■ EXAMPLE OF SOLDER PADS DIMENSIONS



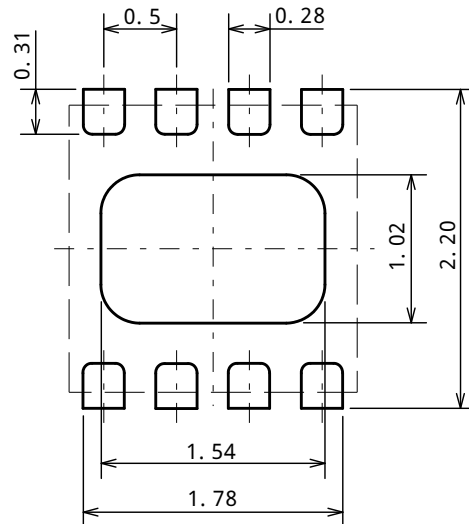
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Unit: mm

### ■ PACKAGE DIMENSIONS



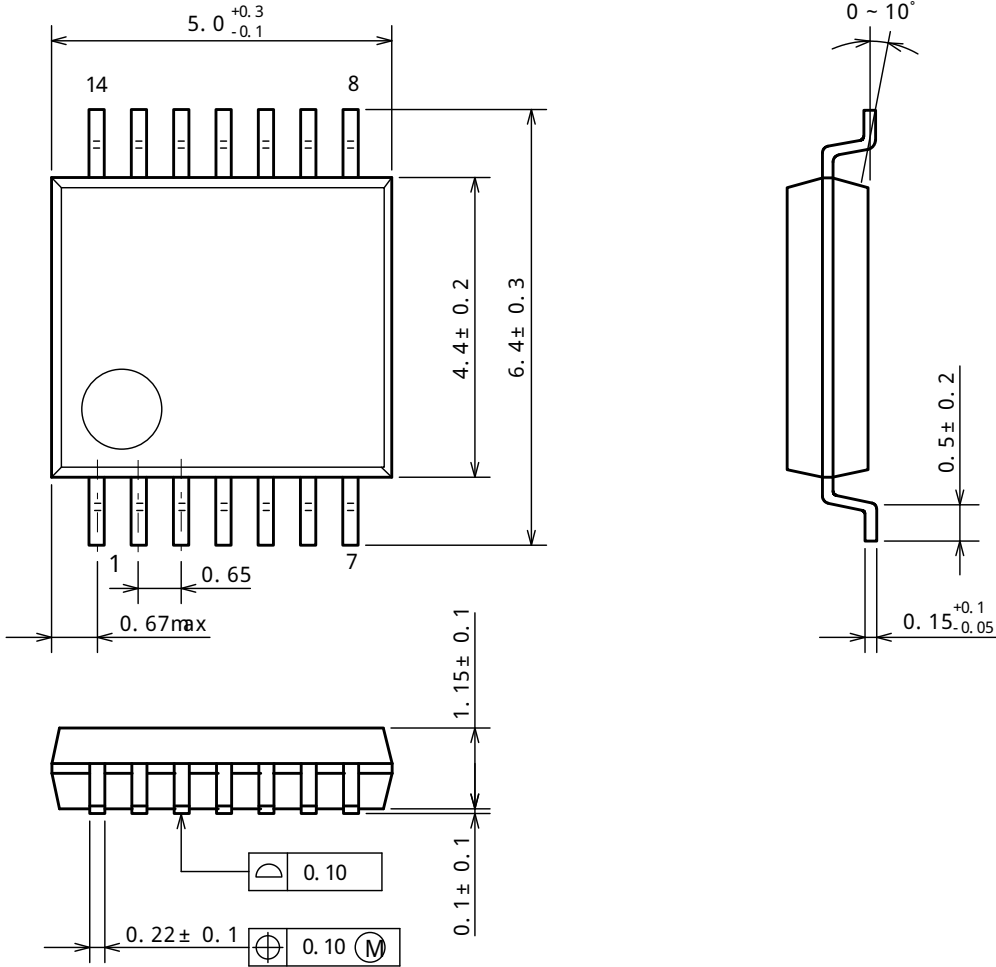
### ■ EXAMPLE OF SOLDER PADS DIMENSIONS



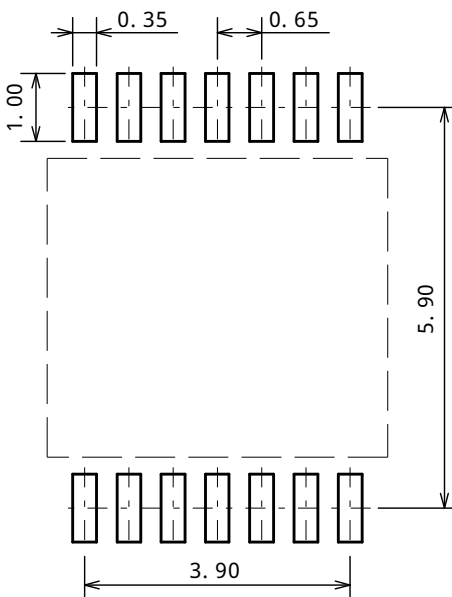
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Unit: mm

### ■ PACKAGE DIMENSIONS



### ■ EXAMPLE OF SOLDER PADS DIMENSIONS

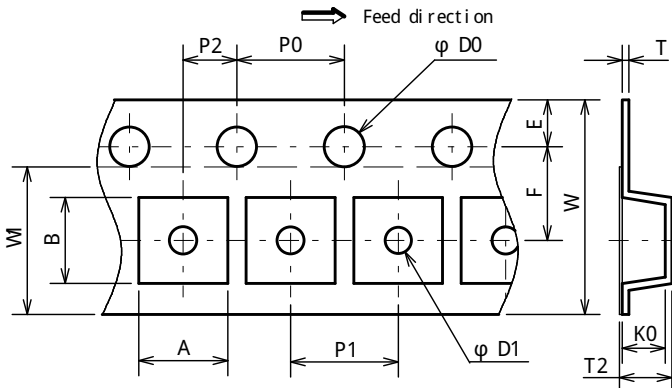


## SOT-23-5

### PACKING SPEC

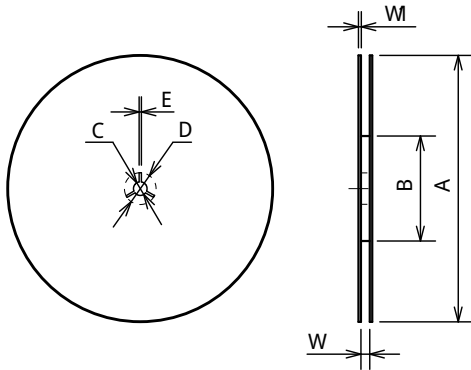
Unit: mm

#### TAPING DIMENSIONS



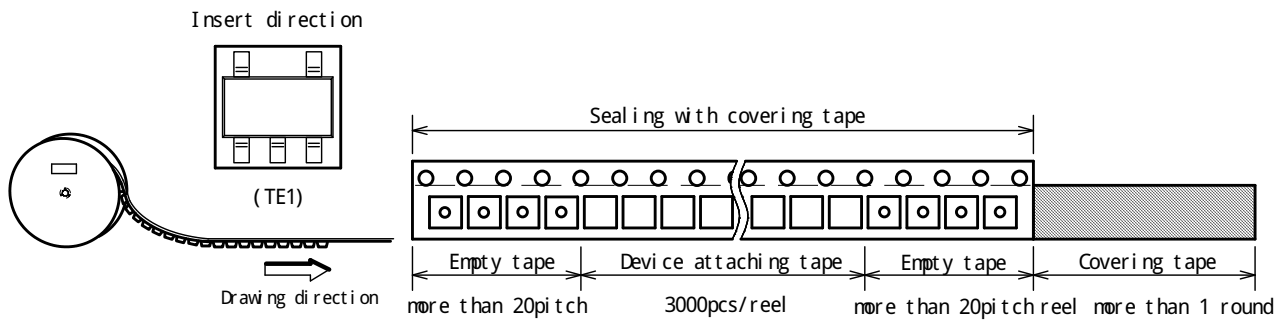
SYMBOL	DI MENSION	REMARKS
A	3.3± 0.1	BOTTOM DI MENSION
B	3.2± 0.1	BOTTOM DI MENSION
D0	1.55	
D1	1.05	
E	1.75± 0.1	
F	3.5± 0.05	
P0	4.0± 0.1	
P1	4.0± 0.1	
P2	2.0± 0.05	
T	0.25± 0.05	
T2	1.82	
K0	1.5± 0.1	
W	8.0± 0.3	
V	5.5	THICKNESS 0.1MAX

#### REEL DIMENSIONS

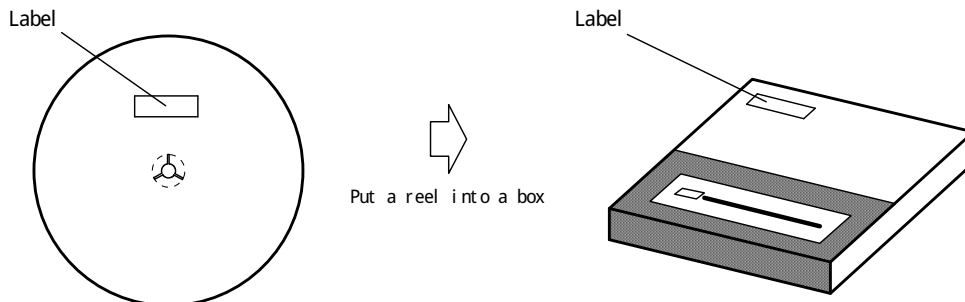


SYMBOL	DI MENSION
A	φ 180± 1
B	φ 60± 1
C	φ 13± 0.2
D	φ 21± 0.8
E	2± 0.5
W	9± 0.5
V	1.2± 0.2

#### TAPING STATE



#### PACKING STATE

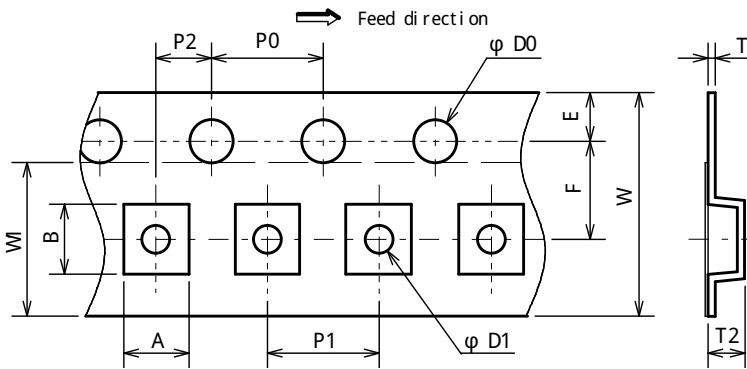


## SC-88A

### PACKING SPEC

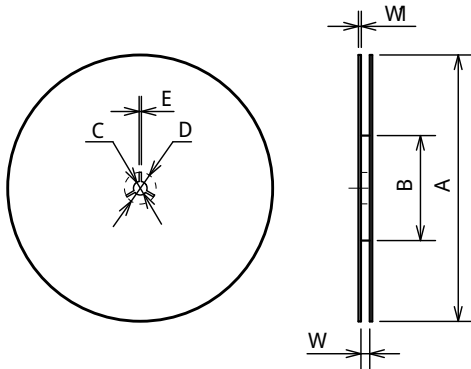
Unit: mm

#### TAPING DIMENSIONS



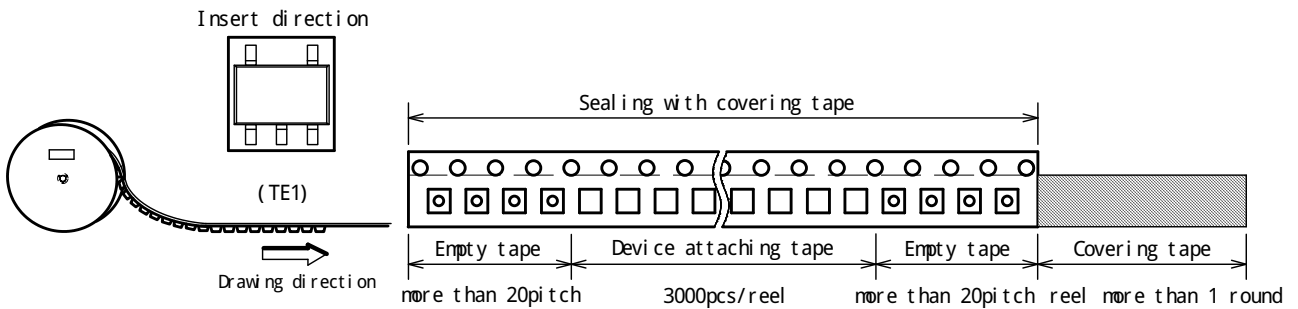
SYMBOL	DI MENSION	REMARKS
A	2.3± 0.1	BOTTOM DI MENSION
B	2.5± 0.1	BOTTOM DI MENSION
D0	1.55± 0.05	
D1	1.05± 0.05	
E	1.75± 0.1	
F	3.5± 0.05	
P0	4.0± 0.1	
P1	4.0± 0.1	
P2	2.0± 0.05	
T	0.25± 0.05	
T2	1.3± 0.1	
W	8.0± 0.2	
Wl	5.5	THICKNESS 0.1max

#### REEL DIMENSIONS

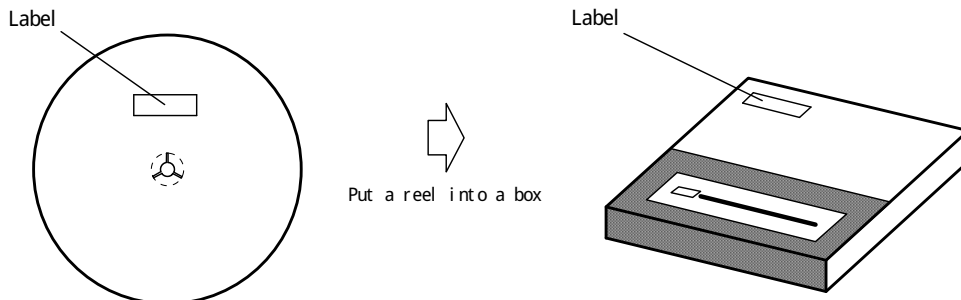


SYMBOL	DI MENSION
A	φ 180± 1
B	φ 60± 1
C	φ 13± 0.2
D	φ 21± 0.8
E	2± 0.5
W	9± 0.5
Wl	1.2± 0.2

#### TAPING STATE



#### PACKING STATE

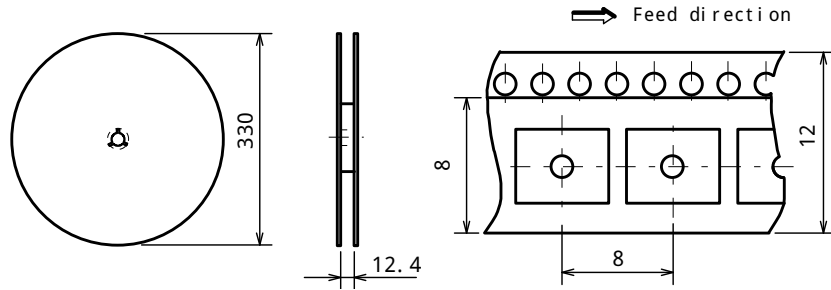


## SOP8

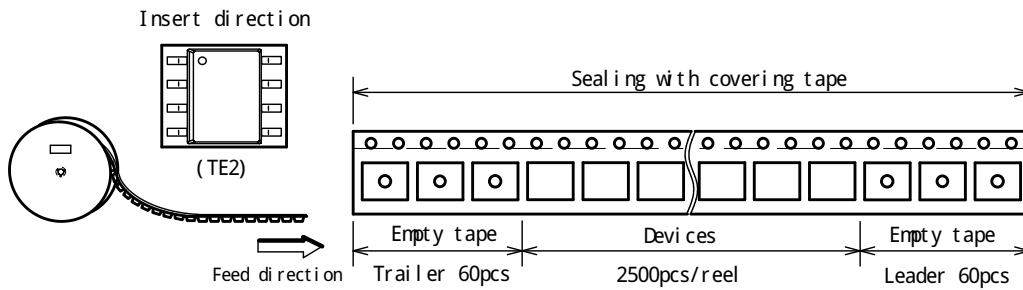
### PACKING SPEC

Unit: mm

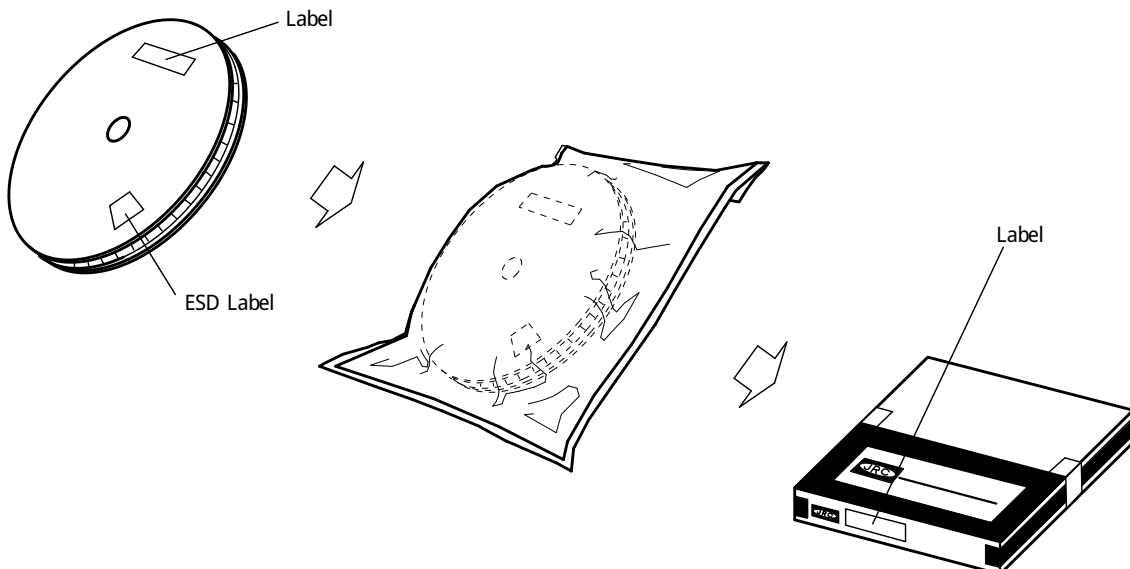
#### REEL DIMENSIONS / TAPING DIMENSIONS



#### TAPING STATE



#### PACKING STATE

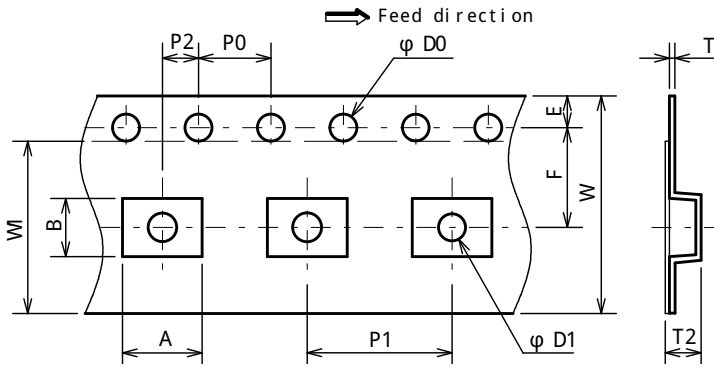


## MSOP8 (TVSP8) MEET JEDEC MO-187-DATHIN

### PACKING SPEC

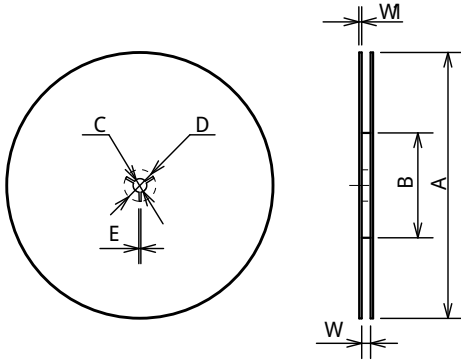
Unit: mm

#### TAPING DIMENSIONS



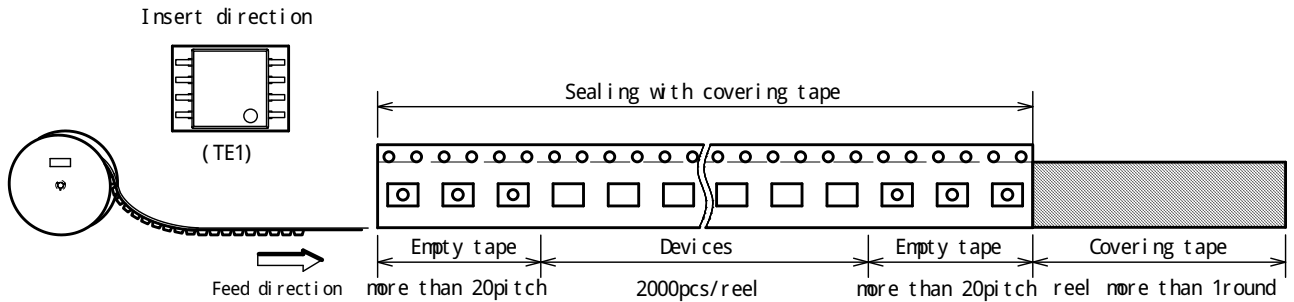
SYMBOL	DI MENSION	REMARKS
A	4.4	BOTTOM DI MENSION
B	3.2	BOTTOM DI MENSION
D0	1.5 <sup>+0.1</sup> <sub>0</sub>	
D1	1.5 <sup>+0.1</sup> <sub>0</sub>	
E	1.75± 0.1	
F	5.5± 0.05	
P0	4.0± 0.1	
P1	8.0± 0.1	
P2	2.0± 0.05	
T	0.30± 0.05	
T2	1.75 (MAX.)	
W	12.0± 0.3	
W1	9.5	THICKNESS 0.1max

#### REEL DIMENSIONS

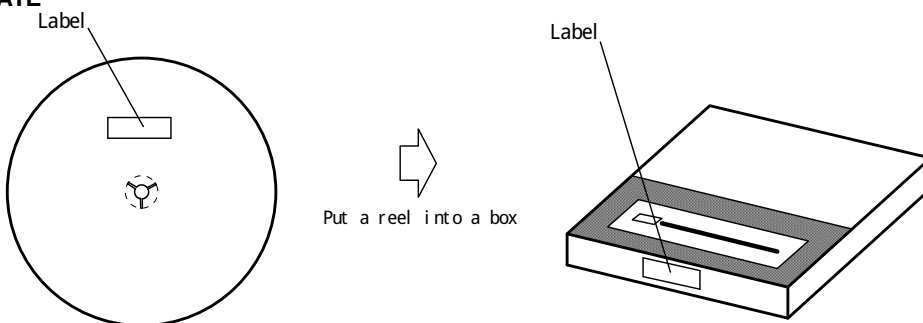


SYMBOL	DI MENSION
A	φ 254± 2
B	φ 100± 1
C	φ 13± 0.2
D	φ 21± 0.8
E	2± 0.5
W	13.5± 0.5
W1	2.0± 0.2

#### TAPING STATE



#### PACKING STATE

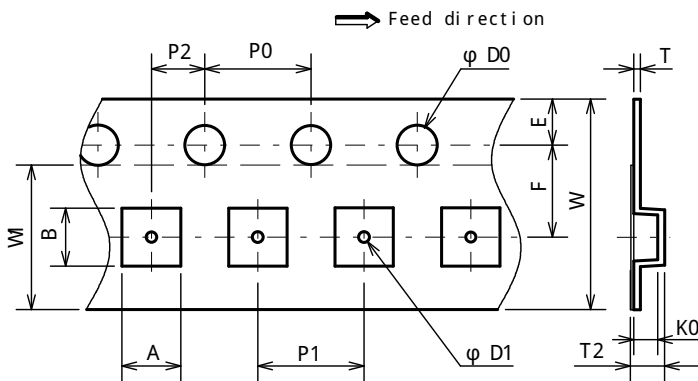


## DFN8-U1 (ESON8-U1)

### PACKING SPEC

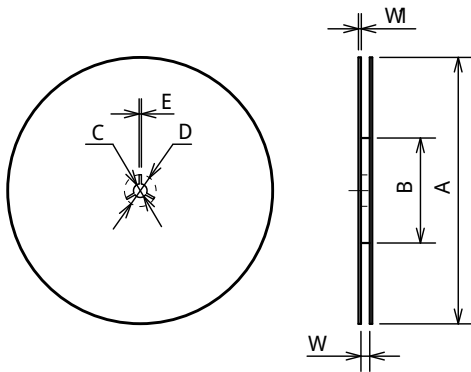
Unit: mm

#### TAPING DIMENSIONS



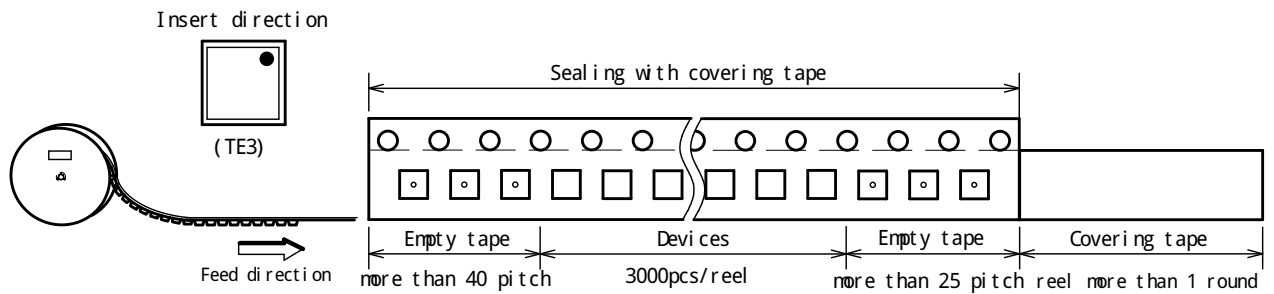
SYMBOL	DI MENSION	REMARKS
A	2.25± 0.05	BOTTOM DI MENSION
B	2.25± 0.05	BOTTOM DI MENSION
D0	1.5 <sup>+0.1</sup> <sub>0</sub>	
D1	0.5± 0.1	
E	1.75± 0.1	
F	3.5± 0.05	
P0	4.0± 0.1	
P1	4.0± 0.1	
P2	2.0± 0.05	
T	0.25± 0.05	
T2	1.00± 0.07	
K0	0.65± 0.05	
W	8.0± 0.2	
W1	5.5	THICKNESS 0.1max

#### REEL DIMENSIONS

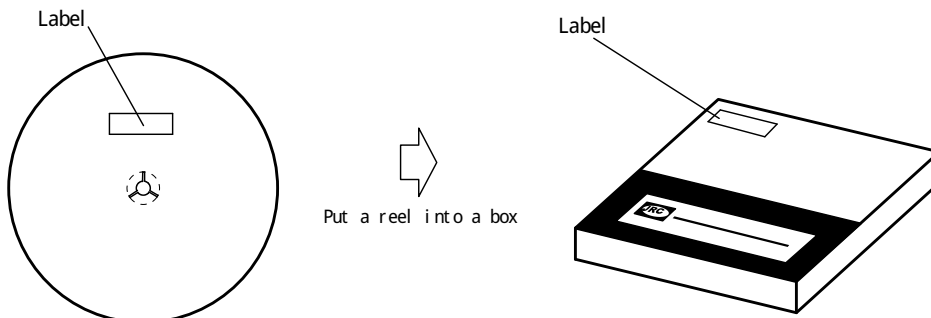


SYMBOL	DI MENSION
A	φ 180 <sup>0</sup> <sub>-1.5</sub>
B	φ 60 <sup>+1</sup> <sub>0</sub>
C	φ 13± 0.2
D	φ 21± 0.8
E	2± 0.5
W	9 <sup>+0.3</sup> <sub>0</sub>
W1	1.2

#### TAPING STATE



#### PACKING STATE



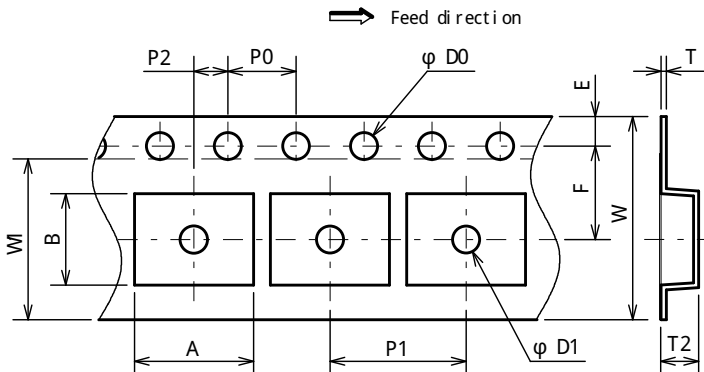


## SSOP14

### PACKING SPEC

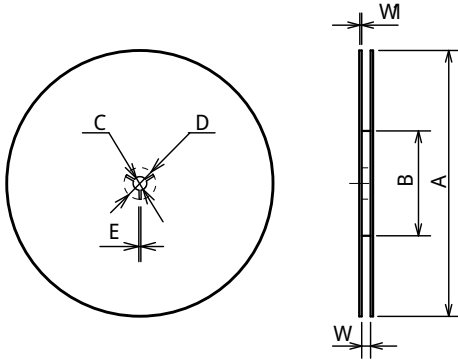
Unit: mm

#### TAPING DIMENSIONS



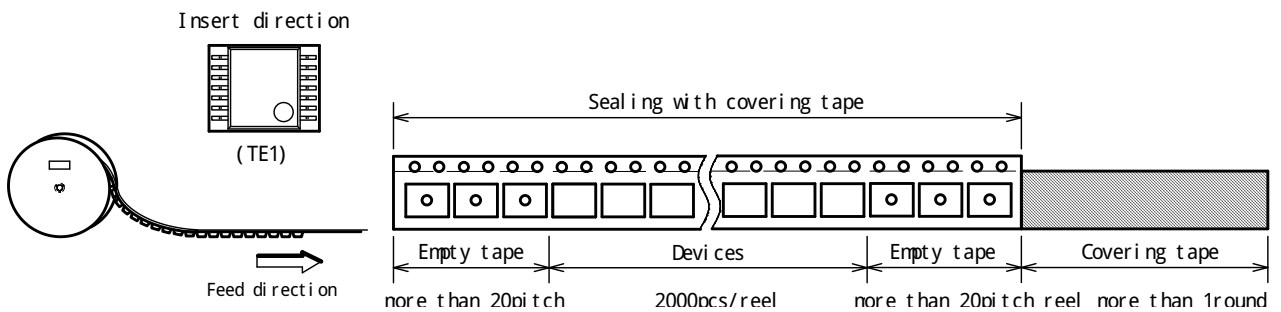
SYMBOL	DI MENSION	REMARKS
A	6.95	BOTTOM DI MENSION
B	5.4	BOTTOM DI MENSION
D0	1.55± 0.05	
D1	1.55± 0.1	
E	1.75± 0.1	
F	5.5± 0.05	
P0	4.0± 0.1	
P1	8.0± 0.1	
P2	2.0± 0.05	
T	0.3± 0.05	
T2	2.2	
W	12.0± 0.3	
Wl	9.5	THICKNESS 0.1max

#### REEL DIMENSIONS

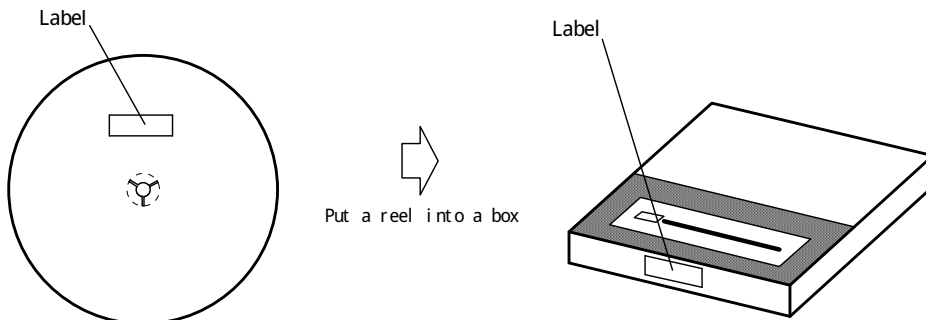


SYMBOL	DI MENSION
A	φ 254± 2
B	φ 100± 1
C	φ 13± 0.2
D	φ 21± 0.8
E	2± 0.5
W	13.5± 0.5
Wl	2± 0.2

#### TAPING STATE

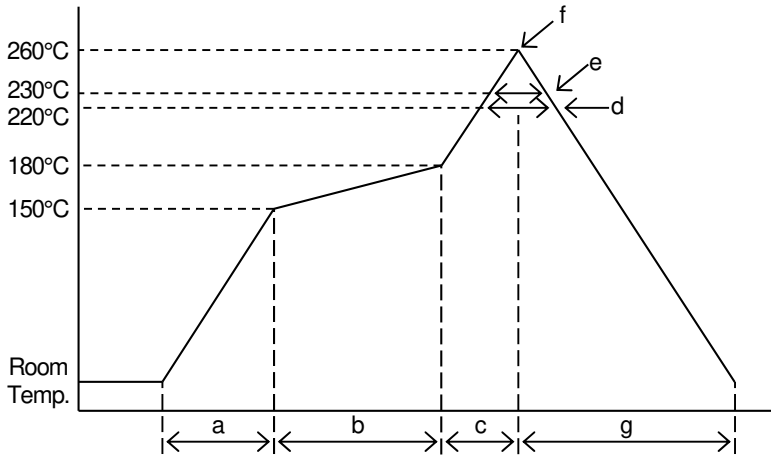


#### PACKING STATE



## ■ RECOMMENDED MOUNTING METHOD

### INFRARED REFLOW SOLDERING PROFILE



a	Temperature ramping rate	1 to 4°C/s
b	Pre-heating temperature	150 to 180°C
	Pre-heating time	60 to 120s
c	Temperature ramp rate	1 to 4°C/s
d	220°C or higher time	shorter than 60s
e	230°C or higher time	shorter than 40s
f	Peak temperature	lower than 260°C
g	Temperature ramping rate	1 to 6°C/s

The temperature indicates at the surface of mold package.

## ■ REVISION HISTORY

DATE	REVISION	CHANGES
April 10, 2018	1.0	New Release
May 27, 2019	2.0	Added DFN8-U1 (ESON8-U1) package. Changed status NJU77550 and NJU77551. Thermal Characteristics: Changed values of $\theta_{ja}$ . Added Power Dissipation vs. Ambient Temperature. Electrical Characteristics: Changed value and unit in High-level Output Voltage. Typical Characteristics: Deleted Figure of EMIRR vs. Frequency. Application Note: Changed Figure of EMIRR vs. Frequency in EMIRR (EMI Rejection Ratio) Definition. Recommended Mounting Method: Deleted Flow and Iron Soldering Profile.
September 5, 2019	2.1	Added note of input voltage in ABSOLUTE MAXIMUM RATINGS. Added condition of input voltage in RECOMMENDED OPERATING CONDITIONS.
November 15, 2019	2.2	Changed status NJU77552KU1
July 22, 2020	3.0	Updated datasheet format. Updated Features and Application note.

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