Self-Protected Low Side Driver with Temperature and Current Limit

42 V, 10 A, Single N−Channel, DPAK

NCV8408, NCV8408B

NCV8408/B is a single channel protected Low−Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain−to−Gate clamping for overvoltage protection. Thermal protection includes a latch which can be reset by toggling the input. This device is suitable for harsh automotive environments.

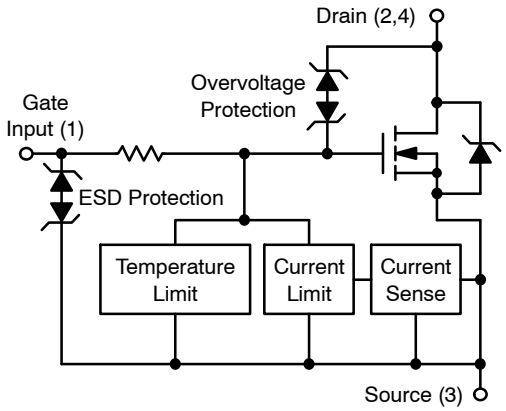
Features

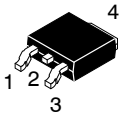
- Short Circuit Protection
- Thermal Shutdown with Latched Reset
- Gate Input Current Flag During Latched Fault Condition
- Overvoltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

V_{DSS} (Clamped)	$R_{DS(on)}$ TYP	I_D MAX (Limited)
42 V	55 mΩ @ 5 V	10 A





DPAK
CASE 369C
STYLE 2

ORDERING INFORMATION

Device	Package	Shipping†
NCV8408DTRKG	DPAK (Pb−Free)	2500/Tape & Reel
NCV8408BDTRKG	DPAK (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage Internally Clamped	V_{DSS}	42	Vdc
Drain−to−Gate Voltage Internally Clamped (R_{GS} = 1.0 MΩ)	V_{DGR}	42	V
Gate−to−Source Voltage	V_{GS}	±14	Vdc
Continuous Drain Current	I_D	Internally Limited	
Gate Input Current (V_{GS} = ±14 V_{DC})	I_{GS}	±10	mA
Source to Drain Current	I_{SD}	4.0	A
Total Power Dissipation @ T_A = 25°C (Note 1) @ T_A = 25°C (Note 2)	P_D	 1.8 2.3	W
Thermal Resistance Junction−to−Ambient Steady State (Note 1) Junction−to−Ambient Steady State (Note 2) Junction−to−Tab Steady State (Note 3)	 $R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JT}$	 70 55 2.1	°C/W
Single Pulse Inductive Load Switching Energy (V_{DD} = 20 Vdc, V_{GS} = 5.0 V, I_L = 8.0 A) Repetitive Pulse Inductive Load Switching Energy (V_{DD} = 20 Vdc, V_{GS} = 5.0 V, I_L = 8.0 A, T_J = 25°C) Repetitive Pulse Inductive Load Switching Energy (V_{DD} = 20 Vdc, V_{GS} = 5.0 V, I_L = 6.8 A, T_J = 105°C)	E_{AS} E_{AR} E_{AR}	185 128 92	mJ
Load Dump Voltage (V_{GS} = 0 and 10 V, R_I = 2.0 Ω, R_L = 4.5 Ω, t_d = 400 ms, T_J = 25°C)	V_{LD}	63	V
Operating Junction Temperature	T_J	−40 to 150	°C
Storage Temperature	T_{stg}	−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted onto minimum pad FR4 PCB (1 oz Cu, 0.06” thick).
2. Surface−mounted onto 2″ square FR4 PCB, (1″ square, 1 oz Cu, 0.06” thick).
3. Surface−mounted onto minimum pad FR4 PCB (2 oz Cu, 0.06” thick).

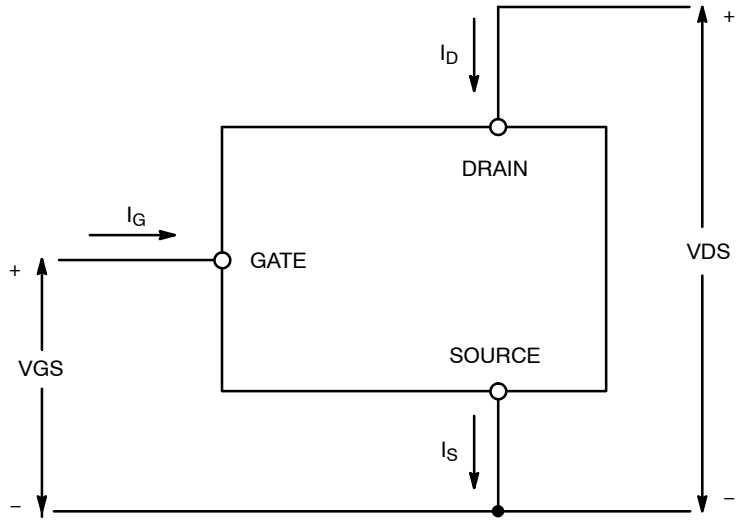


Figure 1. Voltage and Current Convention

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Clamped Breakdown Voltage (Note 4) (V_{GS} = 0 V, I_D = 10 mA, T_J = 25°C) (V_{GS} = 0 V, I_D = 10 mA, T_J = 150°C) (Note 6) (V_{GS} = 0 V, I_D = 10 mA, T_J = −40°C) (Note 6)		$V_{(BR)DSS}$	 42 40 43	 46 45 47	 51 51 51	V
Zero Gate Voltage Drain Current (V_{GS} = 0 V, V_{DS} = 32 V, T_J = 25°C) (V_{GS} = 0 V, V_{DS} = 32 V, T_J = 150°C) (Note 6)		I_{DSS}	 − −	 0.6 2.5	 5.0 10	μA
INPUT CHARACTERISTICS (Note 4)						
Gate Input Current − Normal Operation	(V_{GS} = 5.0 V)	I_{GSSF}	−	25	50	μA
Gate Input Current − Protection Latched	(V_{GS} = 5.0 V) (Note 6)	I_{GSSL}	−	440	−	μA
Gate Threshold Voltage	(V_{GS} = V_{DS}, I_D = 1 mA)	$V_{GS(th)}$	1.0	1.7	2.2	V
Gate Threshold Temperature Coefficient		$V_{GS(th)}/T_J$	−	5.0	−	−mV/°C
Latched Reset Voltage	(Note 6)	V_{LR}	0.8	1.4	1.9	V
Latched Reset Time	(V_{GS} = 5.0 V to V_{GS} < 1 V) (Note 6)	t_{LR}	10	40	100	μs
Internal Gate Input Resistance			−	25.5	−	kΩ
ON CHARACTERISTICS (Note 4)						
Static Drain−to−Source On−Resistance (V_{GS} = 5.0 V, I_D = 3.0 A, T_J @ 25°C) (V_{GS} = 5.0 V, I_D = 3.0 A, T_J @ 150°C) (Note 6)		$R_{DS(on)}$	 − −	 55 100	 60 120	mΩ
Source−Drain Forward On Voltage	(V_{GS} = 0 V, I_S = 7.0 A)	V_{SD}	−	0.95	−	V
SWITCHING CHARACTERISTICS (Note 6)						
Turn−OFF/ON Slew Rate Matching	V_{GS} = 5.0 V, V_{DS} = 13 V, R_L = 4 Ω; T_J = −40°C T_J = 150°C T_J = 25°C −40°C < T_J < 150°C	T_{Match}	 −15 −15 −5 −20	 − − − −	 15 15 5 20	%
Turn−ON Delay Time	V_{GS} = 5 V, V_{DS} = 13 V R_L = 4 Ω, −40°C < T_J < 150°C	$t_{d(ON)}$		10	20	μs
Rise Time (10% I_D to 90% I_D)		t_r		20	40	
Turn−OFF Delay Time		$t_{d(OFF)}$		30	60	
Fall Time (90% I_D to 10% I_D)		t_f		20	40	
Slew−Rate ON (90% V_D to 10% V_D)		$-dV_{DS}/dt_{ON}$		0.5		V/μs
Slew−Rate OFF (10% V_D to 90% V_D)		dV_{DS}/dt_{OFF}		0.5		
SELF PROTECTION CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Note 5)						
Current Limit V_{GS} = 5.0 V, V_{DS} = 10 V, T_J @ 25°C V_{GS} = 5.0 V, V_{DS} = 10 V, T_J = 150°C (Note 6) V_{GS} = 5.0 V, V_{DS} = 10 V, T_J = −40°C (Note 6)		I_{LIM}	 10 10 9	 13 − −	 16 18 16	A
Temperature Limit (Turn−off)	V_{GS} = 5.0 V V_{GS} = 10 V	$T_{LIM(off)}$	150 150	175 165	200 185	°C
ESD ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)						
Electro−Static Discharge Capability	Human Body Model (HBM)	ESD	4000	−	−	V
Electro−Static Discharge Capability	Machine Model (MM)	ESD	400	−	−	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.
5. Fault conditions are viewed as beyond the normal operating range of the part.
6. Not subject to production testing.

TEST CIRCUITS AND WAVEFORMS

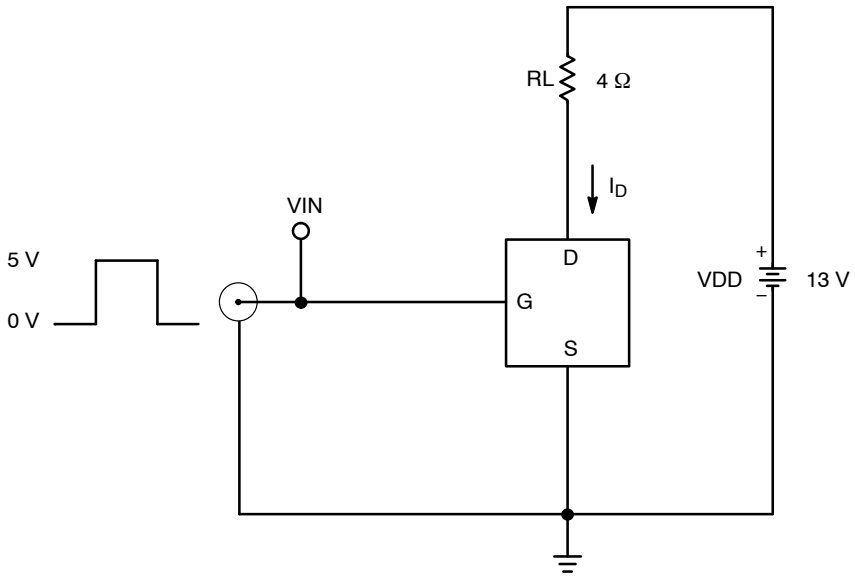


Figure 2. Resistive Load Switching Test Circuit

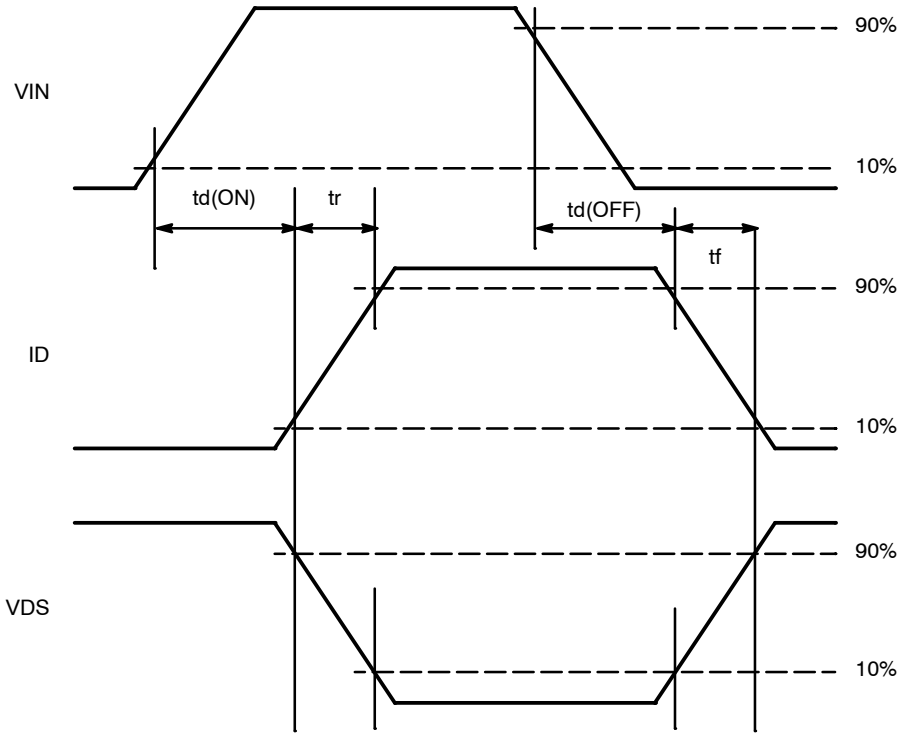


Figure 3. Resistive Load Switching Waveforms

TEST CIRCUITS AND WAVEFORMS

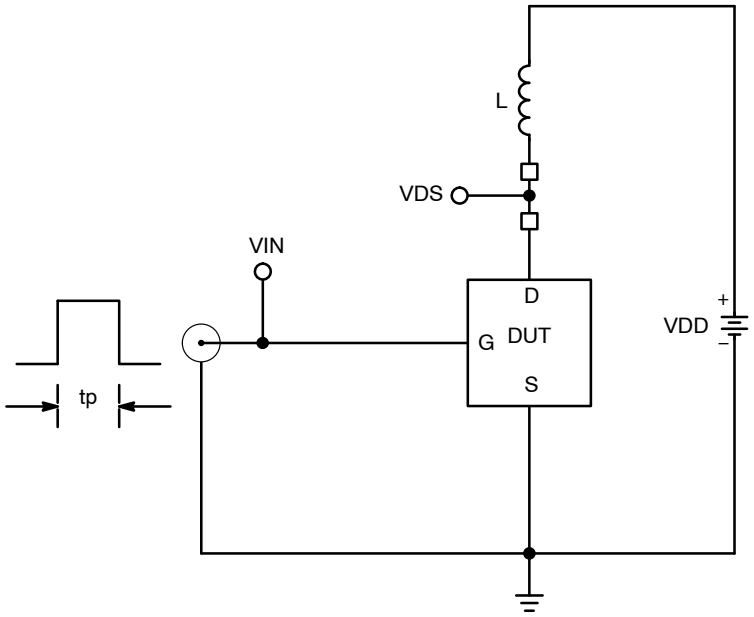


Figure 4. Inductive Load Switching Test Circuit

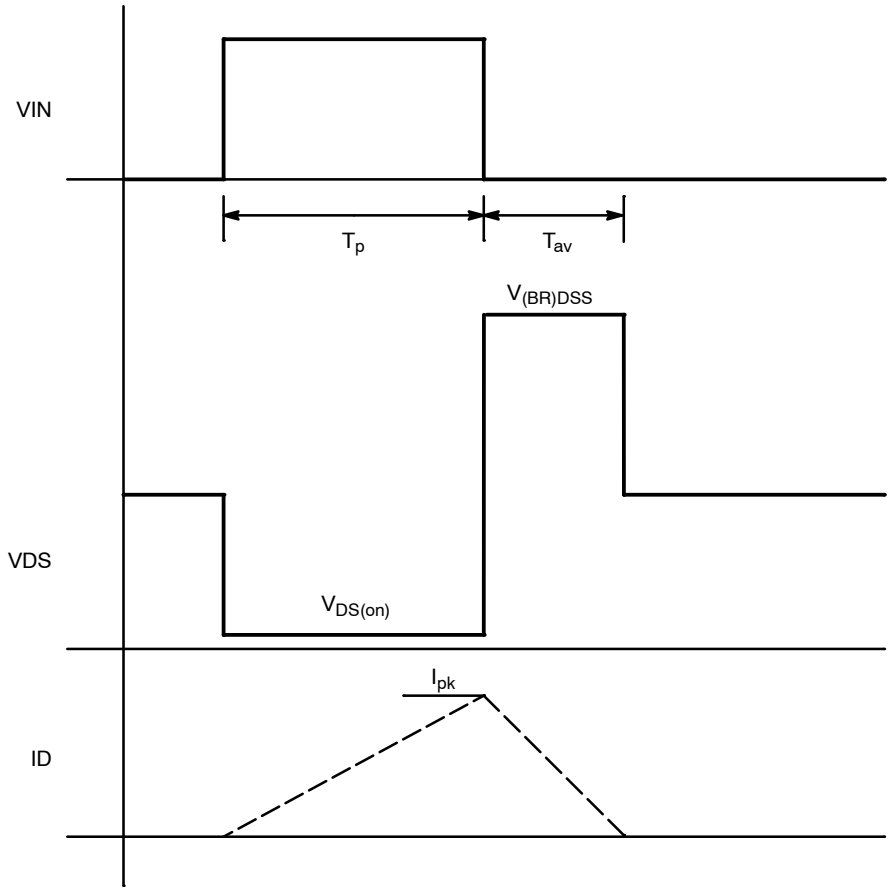


Figure 5. Inductive Load Switching Waveforms

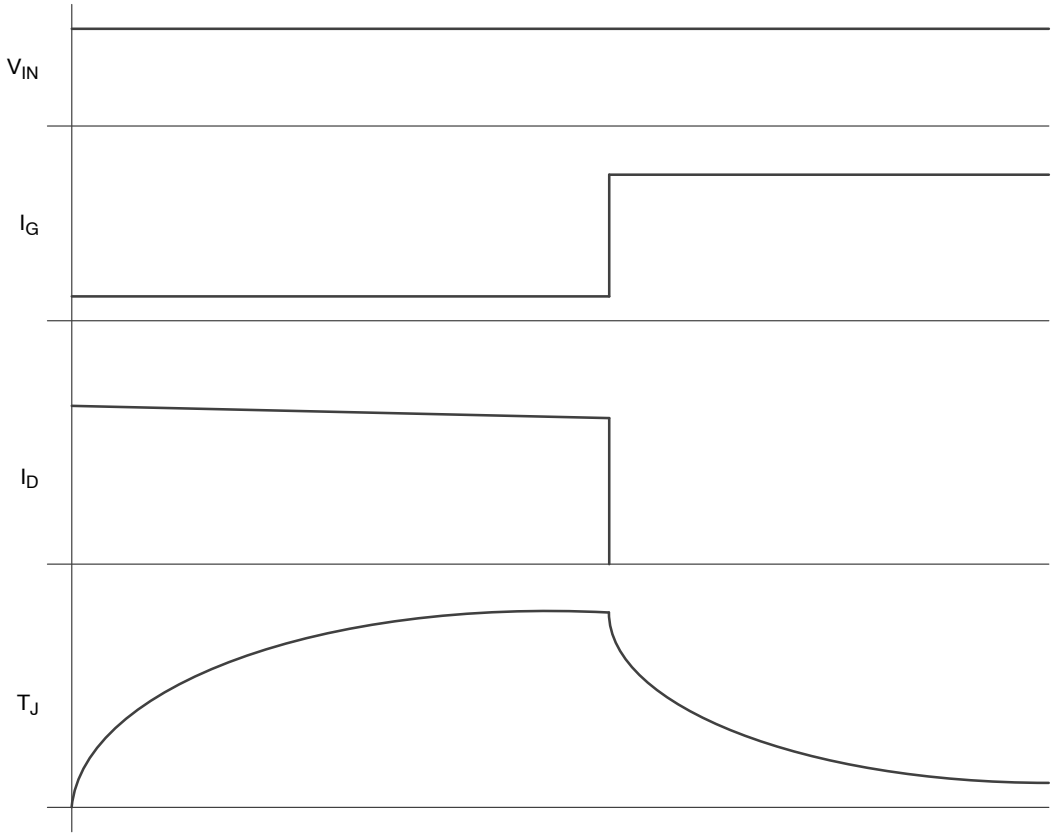


Figure 6. Short−Circuit Protection Behavior

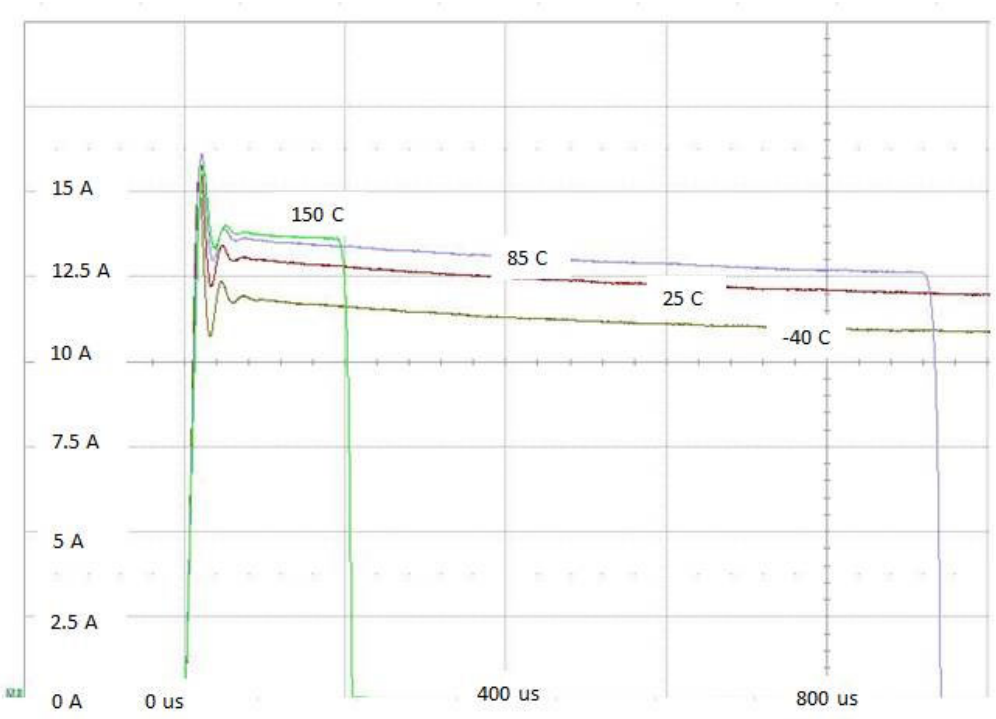


Figure 7. Turn on into Short Circuit Device Response

TYPICAL CHARACTERISTICS

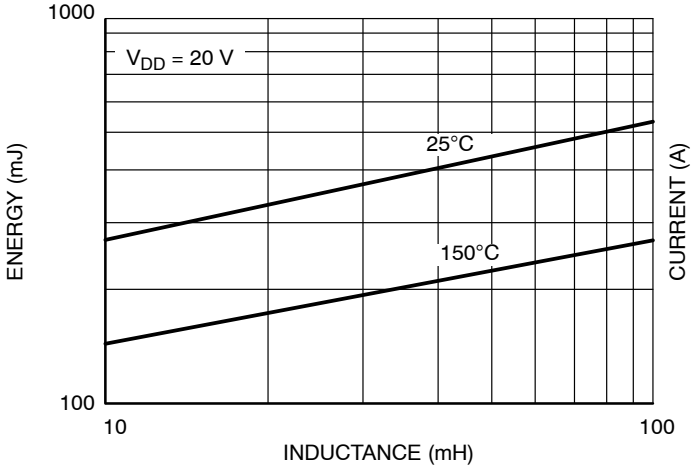


Figure 8. NCV8408 Maximum Switch Off Energy vs Inductance

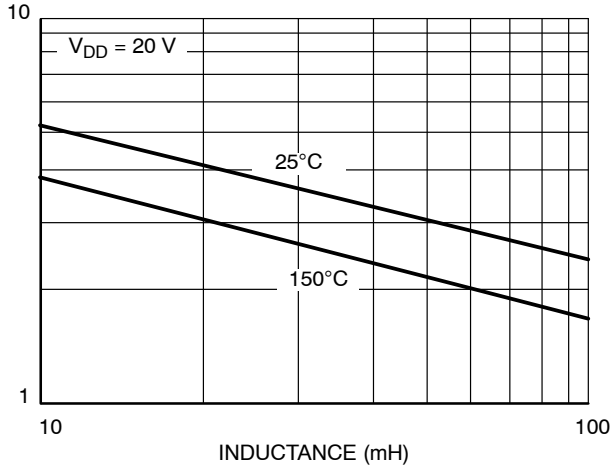


Figure 9. NCV8408 Maximum Switch Off Current vs Inductance

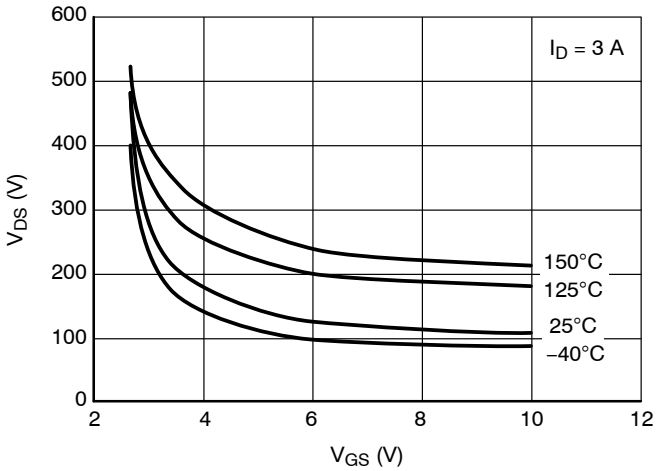


Figure 10. V_{GS} vs V_{DS}

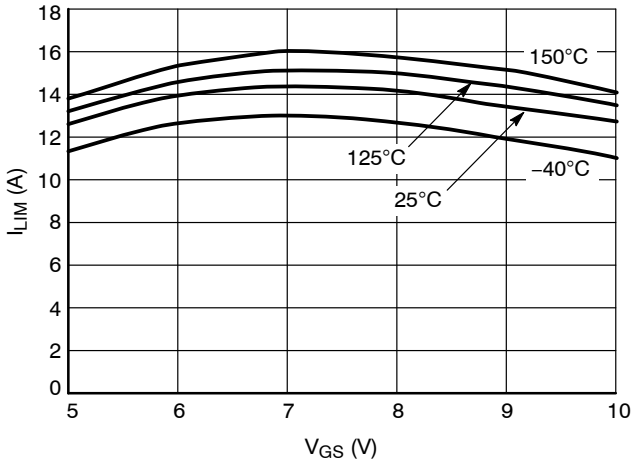


Figure 11. Current Limit vs. Gate Voltage

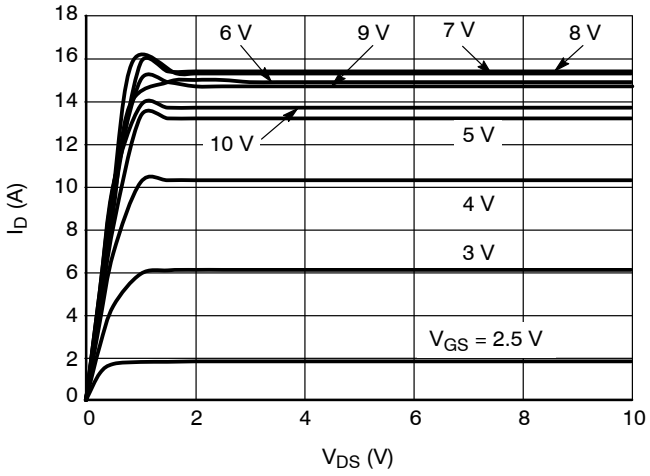


Figure 12. Drain Current vs. Drain Voltage

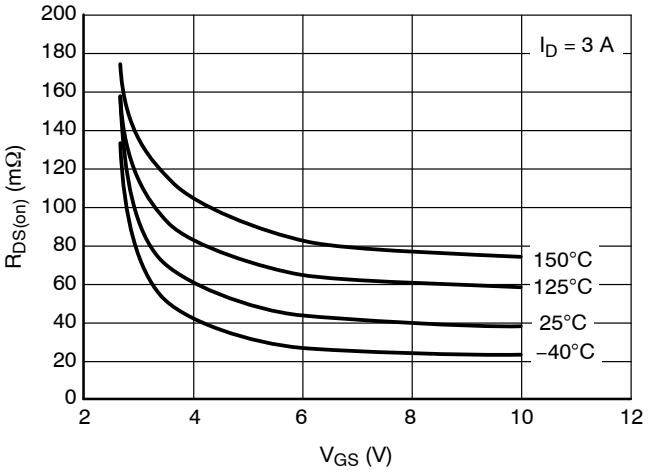


Figure 13. $R_{DS(on)}$ vs. Gate Voltage

TYPICAL CHARACTERISTICS

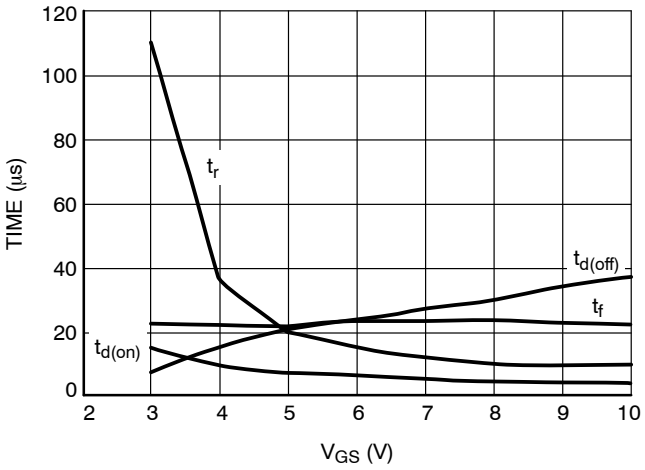


Figure 14. Resistive Switching

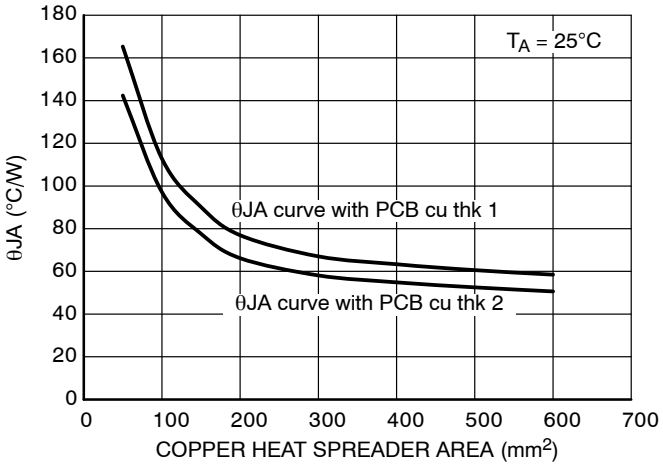


Figure 15. $R_{\theta JA}$ vs. Copper Area

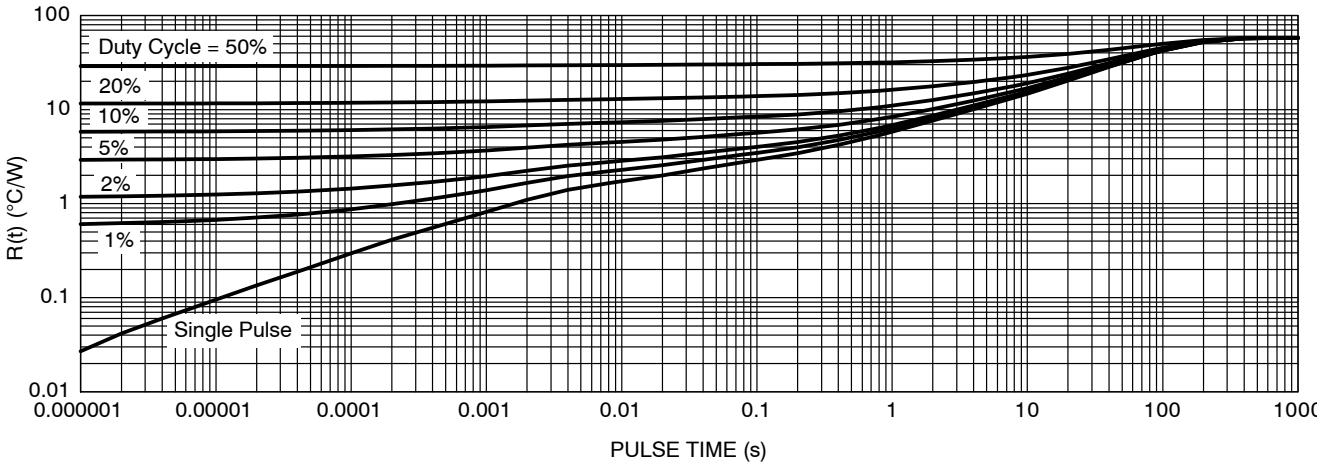
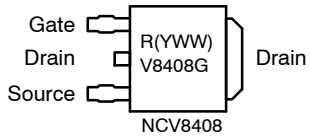
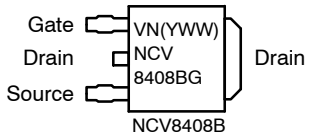


Figure 16. Transient Thermal Resistance

MARKING DIAGRAMS

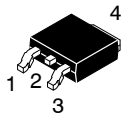


R =Site Code
Y = Year
WW = Work Week
G = Pb−Free Package



VN = Site Code
Y = Year
WW = Work Week
G = Pb−Free Package

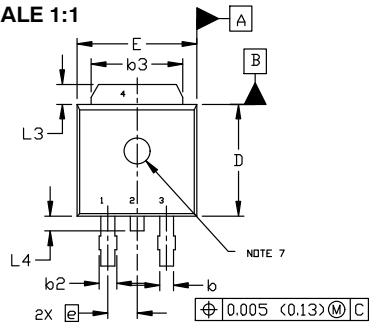
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



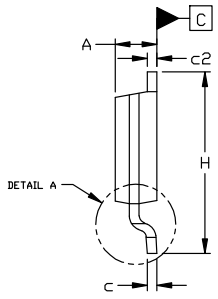
DPAK (SINGLE GAUGE)
CASE 369C
ISSUE G

DATE 31 MAY 2023

SCALE 1:1



TOP VIEW

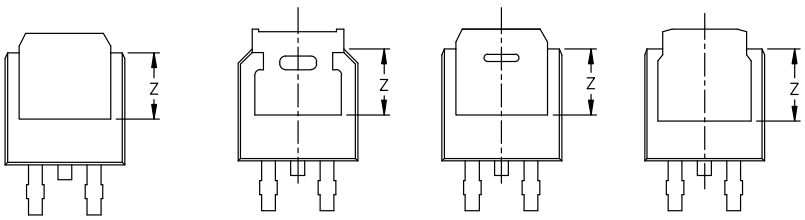


SIDE VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

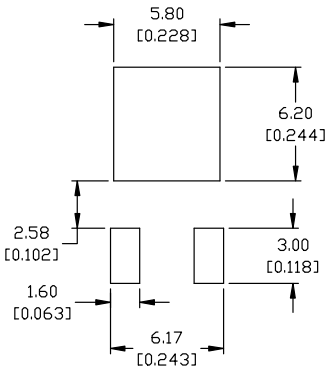
DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	----	0.040	---	1.01
Z	0.155	----	3.93	---



BOTTOM VIEW

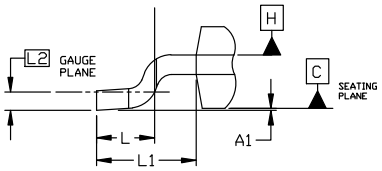
BOTTOM VIEW

ALTERNATE CONSTRUCTIONS



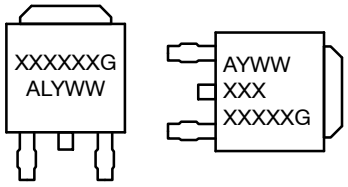
RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



DETAIL A
ROTATED 90° CW

GENERIC MARKING DIAGRAM*



IC **Discrete**

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

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DESCRIPTION:	**DPAK (SINGLE GAUGE)**	**PAGE 1 OF 1**

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