

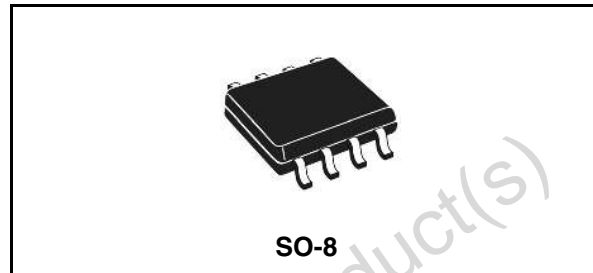
## High current MOSFET driver

### Features

- Dual MOSFET driver for synchronous rectified converters
- High driving current for fast external MOSFET switching
- High frequency operation
- Integrated bootstrap diode
- Adaptive dead-time management
- Flexible gate-drive: 5V to 12V compatible
- High-impedance (HiZ) management for output stage shutdown
- Preliminary OV protection
- SO-8 package

### Applications

- High current VRM / VRD for Desktop / Server / Workstation CPUs
- High current DC / DC converters



### Description

L6741 is a flexible, high-frequency dual-driver specifically designed to drive N-channel MOSFETs connected in Synchronous-Rectified Buck topology. Combined with ST PWM controllers, the driver allows implementing complete voltage regulator solutions for modern high-current CPUs. L6741 embeds high-current drivers for both high-side and low-side MOSFETS. The device accepts flexible power supply (5V to 12V) to optimize the gate-drive voltage for High-Side and Low-Side maximizing the System Efficiency.

The Bootstrap diode is embedded saving the use of external diodes. Anti shoot-through management avoids high-side and low-side mosfet to conduct simultaneously and, combined with Adaptive Dead-Time control, minimizes the LS body diode conduction time.

L6741 embeds Preliminary OV Protection: after Vcc overcomes the UVLO and while the device is in HiZ, the Low-Side MOSFET is turned ON to protect the load in case the output voltage overcomes a warning threshold protecting the load from High-Side MOSFET failures.

The driver is available is SOP8 package.

**Table 1. Device summary**

Order code	Package	Packaging
L6741	SO-8	Tube
L6741TR	SO-8	Tape & Reel

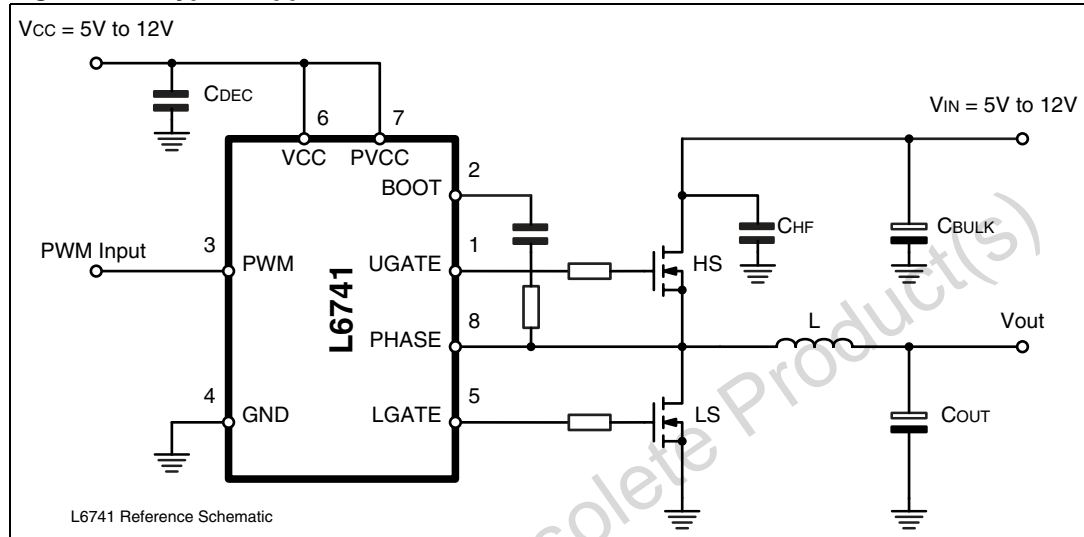
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# 1 Typical application circuit and block diagram

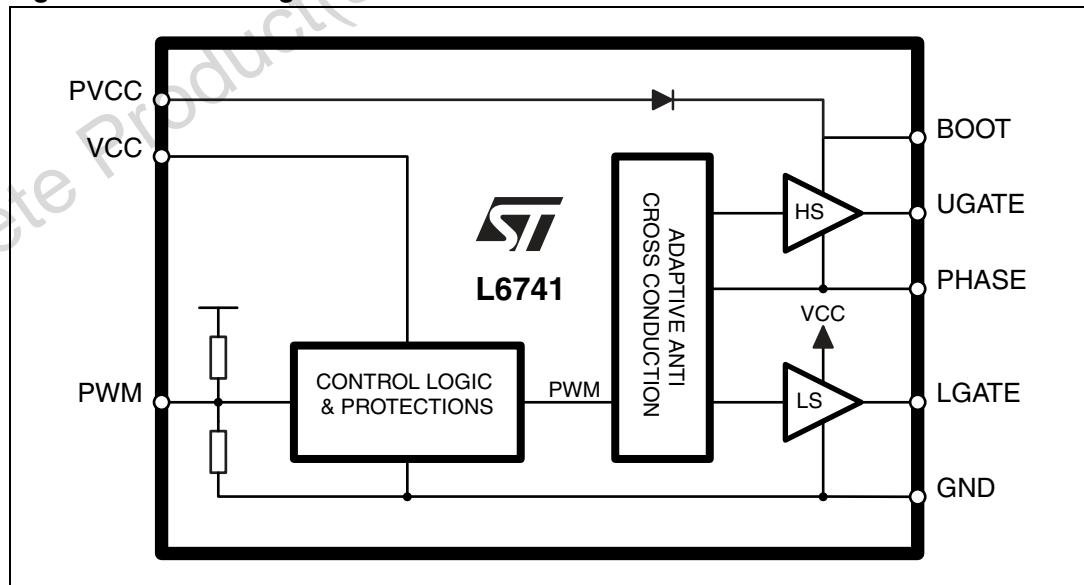
## 1.1 Application circuit

Figure 1. Typical application circuit



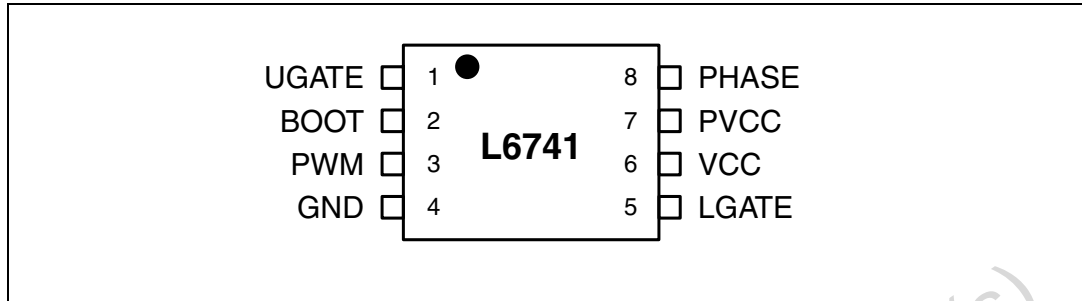
## 1.2 Block diagram

Figure 2. Block diagram



## 2 Pins description and connection diagrams

Figure 3. Pins connection (Top view)



### 2.1 Pin description

Table 2. Pins descriptions

Pin n	Name	Function
1	UGATE	High-side driver output. Connect to High-Side MOSFET gate.
2	BOOT	High-side driver supply. this pin supplies the high-side floating driver. Connect through a $R_{BOOT} - C_{BOOT}$ capacitor to the PHASE pin. Internally connected to the cathode of the integrated Bootstrap diode. See <a href="#">Section 5.3</a> for guidance in designing the capacitor value.
3	PWM	Control input for the driver (5V compatible). This pin controls the state of the driver and which external MOSFET have to be turned-ON. If left floating, it causes the driver to enter the High-Impedance (HiZ) state which causes all mosfets to be OFF. See <a href="#">Section 5.1</a> for details about HiZ.
4	GND	All internal references, logic and drivers are referenced to this pin. Connect to the PCB ground plane.
5	LGATE	Low-side driver output. Connect directly to the Low-Side MOSFET gate. A small series resistor can be useful to reduce dissipated power especially in high frequency applications.
6	VCC	Device and LS driver power supply. Connect to any voltage between 5V and 12V. Bypass with low-ESR MLCC capacitor to GND.
7	PVCC	Integrated bootstrap diode anode supply. Connect to any voltage between 5V and 12V to supply the HS driver accordingly.
8	PHASE	High-side driver return path. Connect to the high-side MOSFET source. This pin is also monitored for the adaptive dead-time management and Pre-OV protection.

### 3 Thermal data

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJA}$	Thermal resistance junction to ambient (Device soldered on 2s2p PC Board - 67mm x 67mm)	85	°C/W
$T_{MAX}$	Maximum junction temperature	150	°C
$T_{STG}$	Storage temperature range	0 to 150	°C
$T_J$	Junction temperature range	0 to 125	°C
$P_{TOT}$	Maximum power dissipation at 25°C (Device soldered on 2s2p PC Board)	1.15	W

## 4 Electrical specifications

### 4.1 Absolute maximum ratings

**Table 4. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}, V_{PVCC}$	to GND	-0.3 to 15	V
$V_{BOOT}, V_{UGATE}$	to GND to PHASE	41 15	V
$V_{PHASE}$	to GND	-8 to 26	V
$V_{LGATE}$	to GND	-0.3 to $V_{CC} + 0.3$	V
$V_{PWM}$	to GND	-0.3 to 7	V
$V_{CC}, V_{PVCC}$	to GND	-0.3 to 15	V

## 4.2 Electrical characteristics

**Table 5. Electrical characteristics**  
( $V_{CC} = 12V \pm 15\%$ ,  $T_J = 0^\circ\text{C}$  to  $70^\circ\text{C}$  unless otherwise specified).

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
<b>Supply current and power-ON</b>						
$I_{CC}$	VCC supply current	UGATE and LGATE = OPEN BOOT = 12V		5		mA
$I_{BOOT}$	BOOT supply current	UGATE = OPEN; PHASE to GND; BOOT = 12V		2		mA
$UVLO_{VCC}$	VCC Turn-ON	VCC rising			4.1	V
	VCC Turn-OFF	VCC falling	3.5			V
<b>PWM input</b>						
PWM	Input high - $V_{PWM\_IH}$	PWM rising	2.3			V
	Input low - $V_{PWM\_IL}$	PWM falling			1	V
$t_{HiZ}$	HiZ Hold-off Time			150		ns
<b>Gate drivers</b>						
$R_{HIHS}$	HS Source resistance	BOOT - PHASE = 12V; 100mA		2.3	2.8	$\Omega$
$I_{UGATE}$	HS Source Current <sup>(1)</sup>	BOOT - PHASE = 12V; $C_{UGATE}$ to PHASE = 3.3nF		2		A
$R_{LOHS}$	HS Sink Resistance	BOOT - PHASE = 12V; 100mA		2	2.5	$\Omega$
$R_{HILS}$	LS Source Resistance	100mA		1.3	1.8	$\Omega$
$I_{LGATE}$	LS Source Current <sup>(1)</sup>	$C_{LGATE}$ to GND = 5.6nF		3		A
$R_{LOLS}$	LS Sink Resistance	100mA		1	1.5	$\Omega$
<b>Protections</b>						
$V_{PRE\_OV}$	Pre-OV threshold	PHASE rising		1.8		V

1. Parameter guaranteed by designed, not fully tested in production

## 5 Device description and operation

L6741 provides high-current driving control for both High-Side and Low-Side N-Channel MOSFETS connected as Step-Down DC-DC Converter driven by an external PWM signal. The integrated high-current drivers allow using different types of power MOSFETs (also multiple MOS to reduce the equivalent  $R_{ds(ON)}$ ), maintaining fast switching transition.

The driver for the High-Side MOSFET use BOOT pin for supply and PHASE pin for return. The driver for the Low-Side MOSFET use the VCC pin for supply and PGND pin for return.

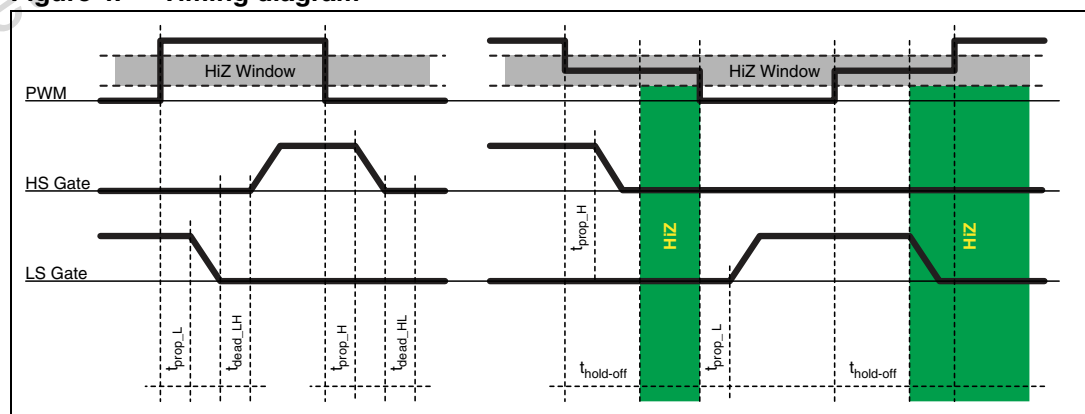
L6741 embodies a anti-shoot-through and adaptive dead-time control to minimize Low-Side body diode conduction time maintaining good efficiency saving the use of external Schottky diodes: when the high-side mosfet turns off, the voltage on its source begins to fall; when the voltage reaches about 2V, the Low-Side MOSFET gate drive voltage is suddenly applied. When the Low-Side MOSFET turns off, the voltage at LGATE pin is sensed. When it drops below about 1V, the High-Side MOSFET gate drive voltage is suddenly applied. If the current flowing in the inductor is negative, the source of highside mosfet will never drop. To allow the Low-Side MOSFET to turn-on even in this case, a watchdog controller is enabled: if the source of the High-Side MOSFET doesn't drop, the Low-Side MOSFET is switched on so allowing the negative current of the inductor to recirculate. This mechanism allows the system to regulate even if the current is negative.

Before VCC overcome the UVLO threshold, L6741 keeps firmly-OFF both High-Side and Low-Side MOSFETS then, after the UVLO has crossed, the PWM input keeps the control of the driver operations. If the PWM input is left floating, the internal resistor divider sets the HiZ: both MOSFETS are kept in the OFF state until PWM transition.

After UVLO crossing and while in HiZ, the Preliminary-OV protection is activated: if the voltage senses through the PHASE pin overcome about 2V, the Low-Side MOSFET is latched ON in order to protect the load from dangerous over-voltage. The Driver status is reset from a PWM transition.

Driver power supply as well as power conversion input are flexible: every combination of 5V and 12V can be chosen for High-Side and Low-Side MOSFET voltage drive. Furthermore, 5V, 12V bus or any intermediate bus that allows the conversion can be chosen freely.

**Figure 4. Timing diagram**



## 5.1 High-impedance (HiZ) management

The Driver is able to manage High-Impedance state by keeping all MOSFETs in off state. If the PWM signal remains in the HiZ window for a time longer than the hold-off time, the device detects the HiZ condition so turning off all the MOSFETs. The HiZ window is defined as the PWM voltage range comprised between  $V_{PWM\_IL}$  and  $V_{PWM\_IH}$ .

The device may exit from the HiZ state only after a PWM transition to logic zero ( $V_{PWM} < V_{PWM\_IL}$ ).

See [Figure 4](#) for details about HiZ timings.

The implementation of the High-Impedance state allows the controller that will be connected to the driver to manage High-Impedance state of its output, avoiding to produce negative undershoot on the regulated voltage during the shut-down stage. Furthermore, different power management states may be managed such as pre-bias start-up.

## 5.2 Preliminary OV protection

After VCC has overcome its UVLO threshold and while the PWM signal is in the HiZ window, L6741 activate the Preliminary-OV protection.

The intent of this protection is to protect the load especially from High-Side MOSFET failures during the system start-up. In fact, VRM, and most in general PWM controllers, have a 12V bus compatible turn-on threshold and results to be non-operative if VCC is below that turn-on thresholds (that results being in the range of about 10V). In case of an High-Side mosfet failure, the controller won't recognize the over voltage until  $VCC = \sim 10V$  (unless other special features are implemented): but in that case the output voltage is already at the same voltage ( $\sim 10V$ ) and the load (CPU in most cases) already burnt.

L6741 by-pass the PWM controller by latching on the Low-Side MOSFET in case the PHASE pin voltage overcome 2V during the HiZ state. When the PWM input exits form the HiZ window, the protection is reset and the control of the output voltage is transferred to the controller connected to the PWM input.

Since the Driver has its own UVLO threshold, a simple way to provide protection to the output in all conditions when the device is OFF consists in supplying the controller through the  $5V_{SB}$  bus:  $5V_{SB}$  is always present before any other voltage and, in case of High-Side short, the Low-Side mosfet is driven with 5V assuring a reliable protection of the load.

Preliminary OV is active after UVLO and while the Driver is in HiZ state and it is disabled after the first PWM transition. The controller will have to manage its output voltage from that time on.

## 5.3 Internal BOOT diode

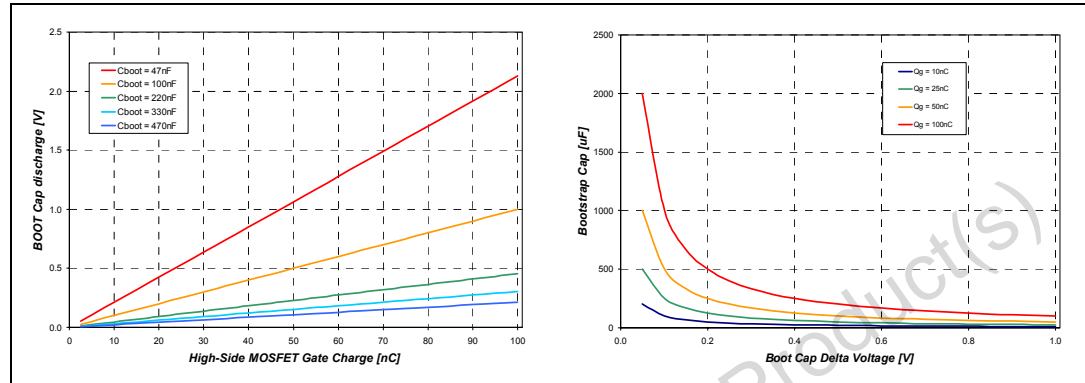
L6741 embeds a boot diode to supply the High-Side driver saving the use of an external component. Simply connecting an external capacitor between BOOT and PHASE complete the High-Side supply connections.

To prevent bootstrap capacitor to extra-charge as a consequence of large negative spikes, an external series resistance  $R_{BOOT}$  (in the range of few ohms) may be required in series to BOOT pin.



Bootstrap capacitor needs to be designed in order to show a negligible discharge due to the High-Side MOSFET turn-on. In fact it must give a stable voltage supply to the High-Side driver during the MOSFET turn-on also minimizing the power dissipated by the embedded Boot Diode. *Figure 5* gives some guidelines on how to select the capacitance value for the bootstrap according to the desired discharge and depending on the selected mosfet.

**Figure 5. Bootstrap capacitance design**



## 5.4 Gate driver voltage flexibility

L6741 allows the user to freely-select the gate drive voltage in order to optimize the efficiency of the application.

The Low-Side MOSFET driving voltage depends on the voltage applied to VCC and can range between 5V to 12V buses.

The High-Side MOSFET driving voltage depends on the voltage applied to PVCC (directly impacting the bootstrap capacitor voltage) and can range between 5V to 12V buses.

## 5.5 Power dissipation

L6741 embeds high current drivers for both High-Side and Low-Side MOSFETs: it is then important to consider the power that the device is going to dissipate in driving them in order to avoid overcoming the maximum junction operative temperature.

Two main terms contribute in the device power dissipation: bias power and drivers' power.

- Device Power ( $P_{DC}$ ) depends on the static consumption of the device through the supply pins and it is simply quantifiable as follow:

$$P_{DC} = V_{CC} \cdot I_{CC} + V_{PVCC} \cdot I_{PVCC}$$

- Drivers' power is the power needed by the driver to continuously switch ON and OFF the external MOSFETs; it is a function of the switching frequency and total gate charge of the selected MOSFETs. It can be quantified considering that the total power  $P_{SW}$  dissipated to switch the MOSFETs dissipated by three main factors: external gate resistance (when present), intrinsic MOSFET resistance and intrinsic driver resistance.

This last term is the important one to be determined to calculate the device power dissipation.

The total power dissipated to switch the mosfets results:

$$P_{SW} = F_{SW} \cdot (Q_{GHS} \cdot PVCC + Q_{GLS} \cdot VCC)$$

When designing an application based on L6741 it is recommended to take into consideration the effect of external gate resistors on the power dissipated by the driver. External gate resistors help the device to dissipate the switching power since the same power  $P_{SW}$  will be shared between the internal driver impedance and the external resistor resulting in a general cooling of the device.

Referring to *Figure 6*, classical mosfet driver can be represented by a push-pull output stage with two different mosfets: P-MOSFET to drive the external gate high and N-MOSFET to drive the external gate low (with their own  $R_{dsON}$ :  $R_{hi\_HS}$ ,  $R_{lo\_HS}$ ,  $R_{hi\_LS}$ ,  $R_{lo\_LS}$ ). The external power mosfet can be represented in this case as a capacitance ( $C_{G\_HS}$ ,  $C_{G\_LS}$ ) that stores the gate-charge ( $Q_{G\_HS}$ ,  $Q_{G\_LS}$ ) required by the external power MOSFET to reach the driving voltage (PVCC for HS and VCC for LS). This capacitance is charged and discharged at the driver switching frequency  $F_{SW}$ .

The total power  $P_{sw}$  is dissipated among the resistive components distributed along the driving path. According to the external Gate resistance and the power-MOSFET intrinsic gate resistance, the driver dissipates only a portion of  $P_{sw}$  as follow:

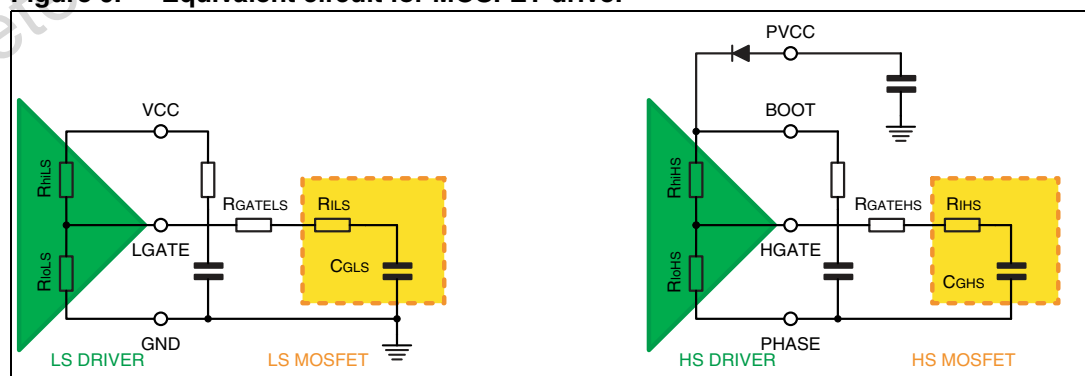
$$P_{SW-HS} = \frac{1}{2} \cdot C_{GHS} \cdot PVCC^2 \cdot F_{sw} \cdot \left( \frac{R_{hiHS}}{R_{hiHS} + R_{GateHS} + R_{iHS}} + \frac{R_{IoHS}}{R_{IoHS} + R_{GateHS} + R_{iHS}} \right)$$

$$P_{SW-LS} = \frac{1}{2} \cdot C_{GLS} \cdot VCC^2 \cdot F_{sw} \cdot \left( \frac{R_{hiLS}}{R_{hiLS} + R_{GateLS} + R_{iLS}} + \frac{R_{IoLS}}{R_{IoLS} + R_{GateLS} + R_{iLS}} \right)$$

The total power dissipated from the driver can then be determined as follow:

$$P = P_{DC} + P_{SW-HS} + P_{SW-LS}$$

**Figure 6. Equivalent circuit for MOSFET drive.**



## 5.6 Layout guidelines

L6741 provides driving capability to implement high-current step-down DC-DC converters.

The first priority when placing components for these applications has to be reserved to the power section, minimizing the length of each connection and loop as much as possible. To minimize noise and voltage spikes (also EMI and losses) power connections must be a part of a power plane and anyway realized by wide and thick copper traces: loop must be anyway minimized. The critical components, such as the power MOSFETs, must be close one to the other. However, some space between the power MOSFET is still required to assure good thermal cooling and airflow.

Traces between the driver and the MOSFETs should be short and wide to minimize the inductance of the trace so minimizing ringing in the driving signals. Moreover, VIAs count needs to be minimized to reduce the related parasitic effect.

The use of multi-layer printed circuit board is recommended.

Small signal components and connections to critical nodes of the application as well as bypass capacitors for the device supply are also important. Locate the bypass capacitor (VCC, PVCC and BOOT capacitors) close to the device with the shortest possible loop and use wide copper traces to minimize parasitic inductance.

Systems that do not use Schottky diodes in parallel to the Low-Side MOSFET might show big negative spikes on the phase pin. This spike can be limited as well as the positive spike but has an additional consequence: it causes the bootstrap capacitor to be over-charged. This extra-charge can cause, in the worst case condition of maximum input voltage and during particular transients, that boot-to-phase voltage overcomes the abs.max.ratings also causing device failures. It is then suggested in this cases to limit this extra-charge by adding a small resistor  $R_{BOOT}$  in series to the boot capacitor. The use of  $R_{BOOT}$  also contributes in the limitation of the spike present on the BOOT pin.

For heat dissipation, place copper area under the IC. This copper area may be connected with internal copper layers through several VIAs to improve the thermal conductivity. The combination of copper pad, copper plane and VIAs under the driver allows the device to reach its best thermal performances.

**Figure 7. Driver turn-on and turn-off paths**

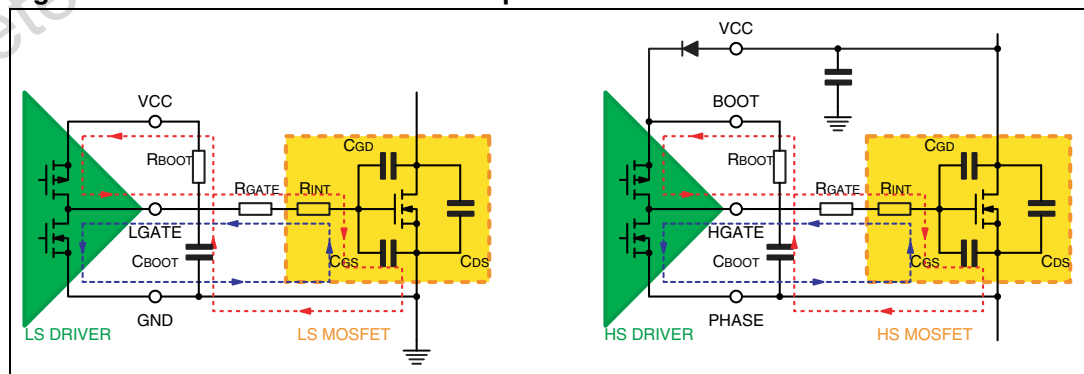
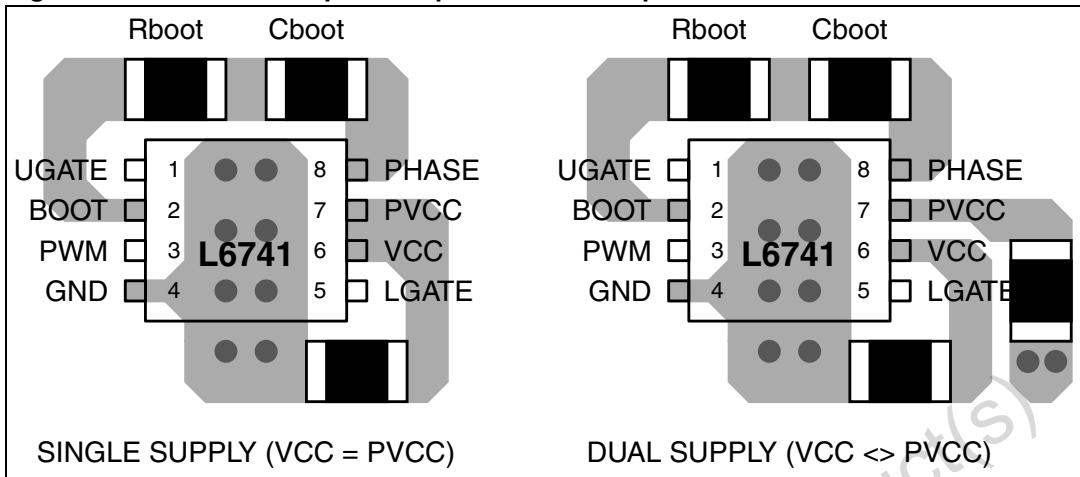


Figure 8. External components placement example.



Obsolete Product(s) - Obsolete Product(s)

## 6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

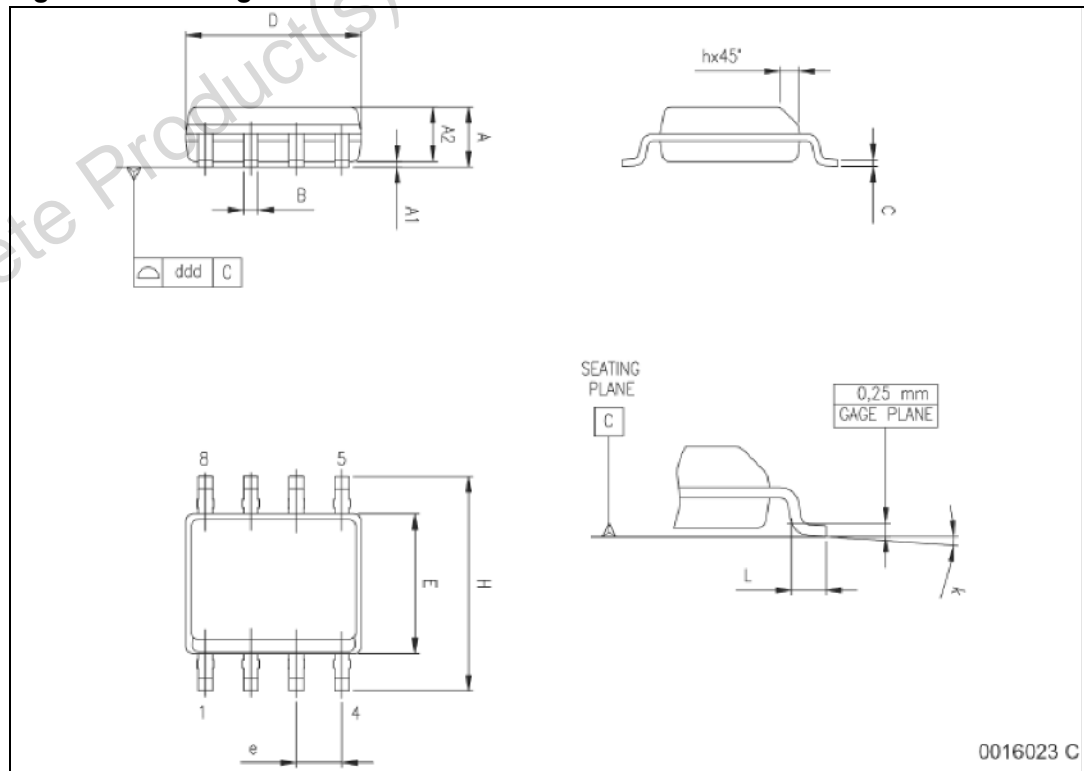
Obsolete Product(s) - Obsolete Product(s)

Table 6. SO-8 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D (1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

Figure 9. Package dimensions



## 7 Revision history

**Table 7. Document revision history**

Date	Revision	Changes
20-Aug-2007	1	Initial release.

Obsolete Product(s) - Obsolete Product(s)

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