Dual High Speed Driver

Description

The SG1626 series is a dual inverting monolithic high speed driver that is pin-to-pin compatible with the DS0026, TSC426 and ICL7667. This device utilizes high voltage Schottky logic to convert TTL signals to high speed outputs up to 18 V. The totem pole outputs have 3 A peak current capability, which enables them to drive 1000 pF loads in typically less than 25 ns. These speeds make it ideal for driving power MOSFETs and other large capacitive loads requiring high speed switching.

In addition to the standard packages, the 16-pin SOIC (DW-package) is available for commercial and industrial applications. These packages offer improved thermal performance for applications requiring high frequencies and/or high peak currents.

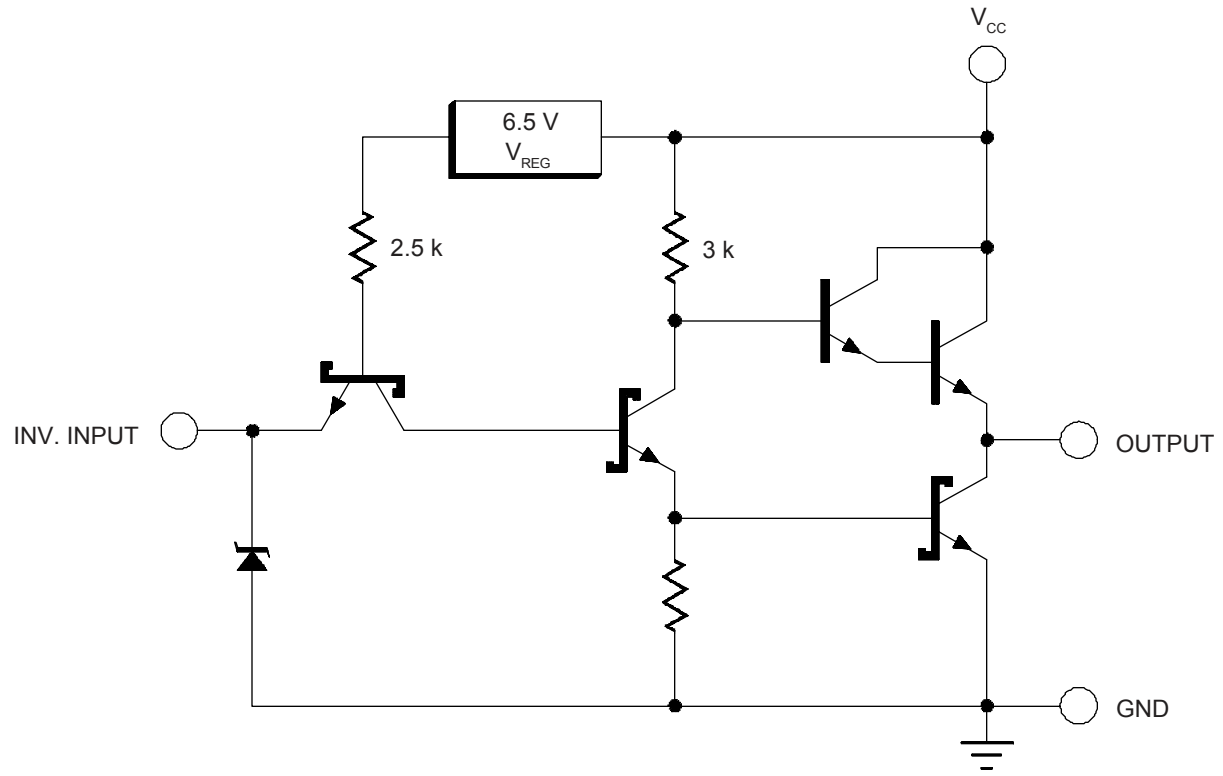
Features

- Pin-to-Pin Compatible with DS0026, TSC426 and ICL7667.
- Totem Pole Outputs with 3.0 A Peak Current Capability.
- Supply Voltage to 22 V.
- Rise and Fall times less than 25 ns.
- Propagation Delays less than 20 ns.
- Inverting High-Speed High-Voltage Schottky Logic.
- Efficient Operation at High Frequency.
- Available in:
  - 8 - Pin Plastic and Ceramic DIP
  - 16 - Pin Plastic SOIC
  - 8 - Pin TO-99
  - 20 - Pin Ceramic LCC

High Reliability Features

- Available to MIL-STD-883, ¶ 1.2.1
- MSC-AMS level “S” Processing Available

Block Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC}) ..... 22 V
Logic Input Voltage ..... 7 V
Source/Sink Output Current (Each Output)
  Continuous ..... ±0.5 A
  Pulse, 500 ns ..... ±3.0 A

Operating Junction Temperature
  Hermetic (T, Y - Packages) ..... 150°C
  Plastic (M, DW, L- Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 s) ..... 300°C

RoHS Peak Package Solder Reflow Temp. (40 s max. exp.)..... 260°C (+0, -5)

Note 1.
Exceeding these ratings could cause damage to the device.
All voltages are with respect to ground.
All currents are positive into the specified terminal.

Thermal Data

Y Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 50°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 130°C/W
M Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 60°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 95°C/W
DW Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 40°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 95°C/W
T Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 25°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 130°C/W

L Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 35°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 120°C/W

Note A. Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
Note B. The above numbers for θ_{JC} are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θ_{JA} numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC}) ..... 4.5 V to 20 V (Note 3)
Frequency Range ..... DC to 1.5 MHz
Peak Pulse Current ..... ±3 A
Logic Input Voltage ..... -0.5 to 5.5 V

Operating Ambient Temperature Range (T_J)
  SG1626 ..... -55°C to 125°C
  SG2626 ..... -25°C to 85°C
  SG3626 ..... 0°C to 70°C

Note 2. Range over which the device is functional.
Note 3. AC performance has been optimized for V_{CC} = 8 V to 20 V.

Electrical Characteristics

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1626 with -55°C ≤ T_A ≤ 125°C, SG2626 with - 25°C ≤ T_A ≤ 85°C, SG3626 with 0°C ≤ T_A ≤ 70°C, and V_{CC} = 20 V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1626/2626/3626			Units
		Min.	Typ.	Max.	
Static Characteristics					
Logic 1 Input Voltage		2.0			V
Logic 0 Input Voltage				0.7	V
Input High Current	V_{IN} = 2.4 V			500	µA
Input High Current	V_{IN} = 5.5 V			1.0	mA
Input Low Current	V_{IN} = 0 V			-4	mA
Input Clamp Voltage	I_{IN} = -10 mA			-1.5	V
Output High Voltage (Note 4)	I_{OUT} = -200 mA	V_{CC}-3			V
Output Low Voltage (Note 4)	I_{OUT} = 200 mA			1.0	V
Supply Current Outputs Low	V_{IN} = 2.4 V (both inputs)		18	27	mA
Supply Current Outputs High	V_{IN} = 0 V (both inputs)		7.5	12	mA

Note 4. V_{CC} = 10 V to 20 V.

Electrical Characteristics (Continued)

Parameter	Test Conditions (Figure 1)	SG1626/2626/3626 T_A= 25°C			SG1626 T_A=-55°C to 125°C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Dynamic Characteristics (Note 6)								
Propagation Delay High-Low	C_L = 1000 pF (Note 5)			18			30	ns
(TPHL)	C_L = 2500 pF		17	25			40	ns
Propagation Delay Low-High	C_L = 1000 pF (Note 5)			25			40	ns
(TPLH)	C_L = 2500 pF		25	35			50	ns
Rise Time (TTLH)	C_L = 1000 pF (Note 5)			30			35	ns
	C_L = 2500 pF		30	40			50	ns
Fall Time (TTHL)	C_L = 1000 pF (Note 5)			20			30	ns
	C_L = 2500 pF		30	40			50	ns
Supply Current (I_{CC})	C_L = 2500 pF, Freq. = 200 kHz							
(both outputs)	Duty Cycle = 50%		30	35			40	mA

Note 5. These parameters, specified at 1000 pF, although guaranteed over recommended operating conditions, are not 100% tested in production.
Note 6. V_{CC} = 15 V.

AC Test Circuit and Switching Time Waveforms (Figure 1)

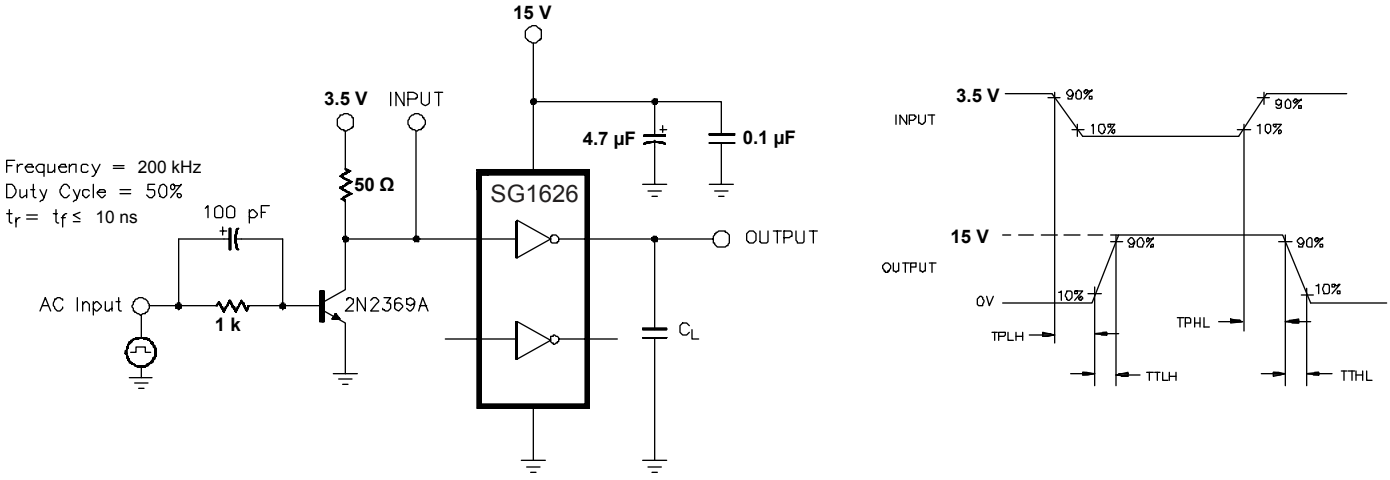


Figure 1 · AC Test Circuit and Switching Time Waveforms

Characteristics Curves

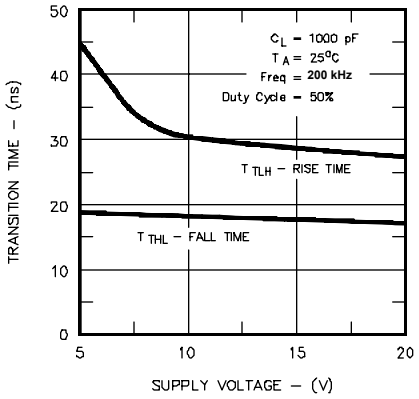


Figure 2 · Transition Times vs. Supply Voltage

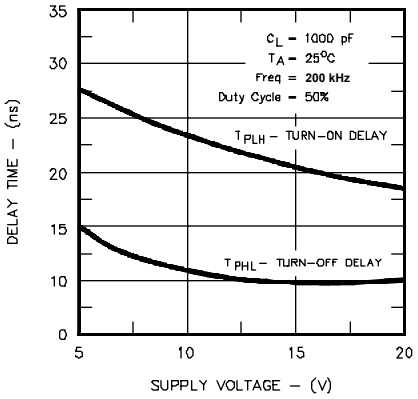


Figure 3 · Propagation Delay vs. Supply Voltage

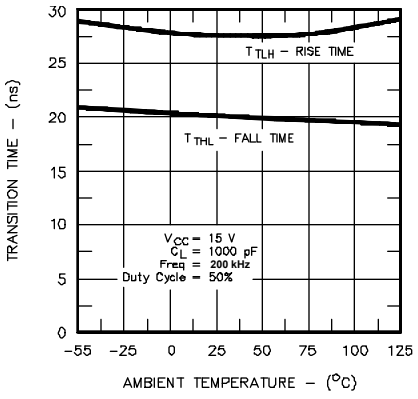


Figure 4 · Transition Times vs. Ambient Temperature

Characteristics Curves (Continued)

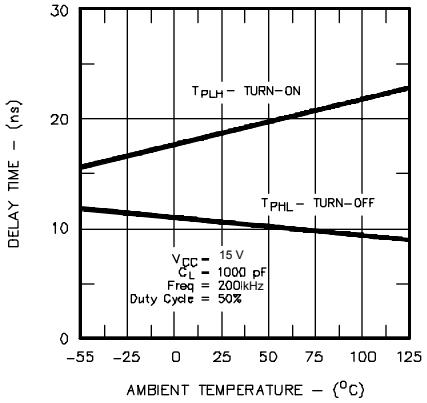


Figure 5 · Propagation Delay vs. Ambient Temperature

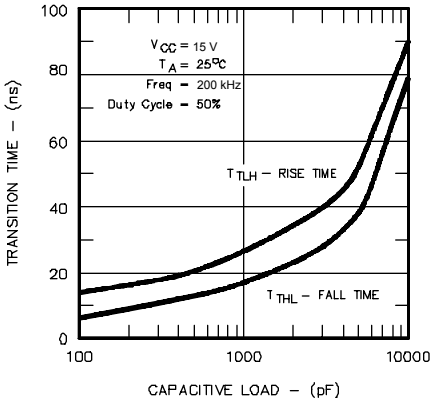


Figure 6 · Transition Times vs. Capacitive Load

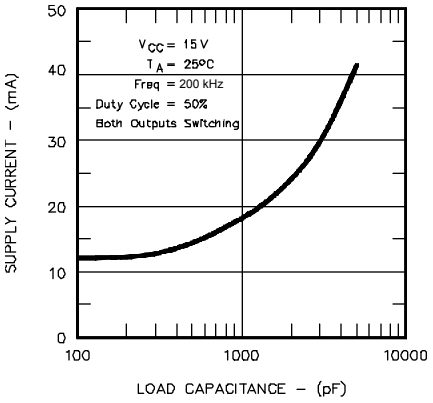


Figure 7 · Supply Current vs. Capacitive Load

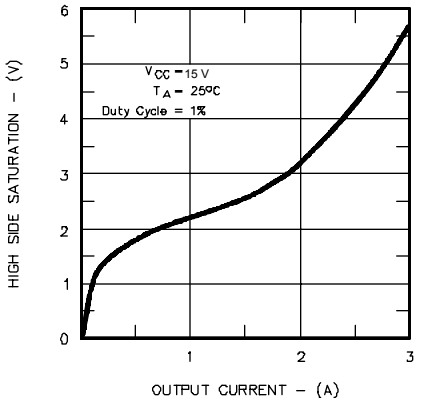


Figure 8 · High Side Saturation vs. Output Current

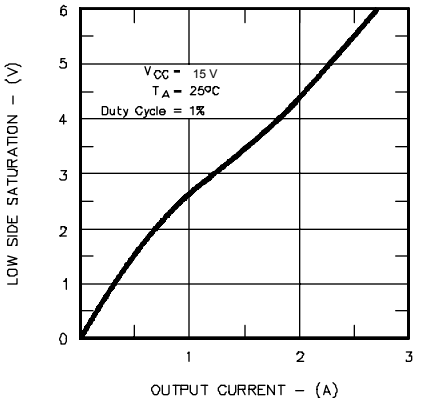


Figure 9 · Low Side Saturation vs. Output Current

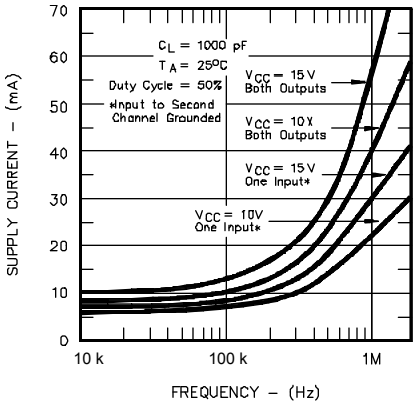


Figure 10 · Supply Current vs. Frequency

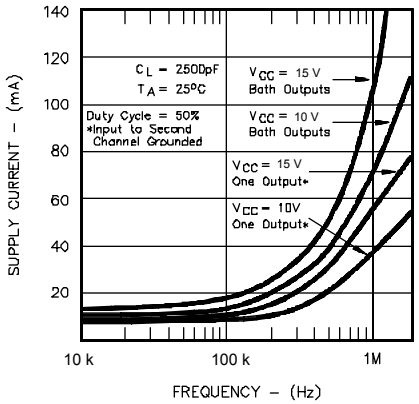


Figure 11 · Supply Current vs. Frequency

Application Information

POWER DISSIPATION

The SG1626, while more energy-efficient than earlier gold-doped driver IC's, can still dissipate considerable power because of its high peak current capability at high frequencies. Total power dissipation in any specific application will be the sum of the DC or steady-state power dissipation, and the AC dissipation caused by driving capacitive loads.

The DC power dissipation is given by:

$P_{DC} = +V_{CC} \cdot I_{CC}$ [1]

where I_{CC} is a function of the driver state, and hence is duty-cycle dependent.

The AC power dissipation is proportional to the switching frequency, the load capacitance, and the square of the output voltage. In most applications, the driver is constantly changing state, and the AC contribution becomes dominant when the frequency exceeds 100-200 kHz.

The SG1626 driver family is available in a variety of packages to accommodate a wide range of operating temperatures and power dissipation requirements. The Absolute Maximums section of the data sheet includes two graphs to aid the designer in choosing an appropriate package for his design.

The designer should first determine the actual power dissipation of the driver by referring to the curves in the data sheet relating operating current to supply voltage, switching frequency, and capacitive load. These curves were generated from data taken on actual devices. The designer can then refer to the Absolute Maximum Thermal Dissipation curves to choose a package type, and to determine if heat-sinking is required.

DESIGN EXAMPLE

Given: Two 2500 pF loads must be driven push-pull from a +15 V supply at 100 kHz. This is a commercial application where the maximum ambient temperature is +50°C, and cost is important.

1. From Figure 11, the average driver current consumption under these conditions will be 18 mA, and the power dissipation will be 15 V x 18 mA, or 270 mW.

2. From the Ambient Thermal Characteristic curve, it can be seen that the M package, which is an 8-pin plastic DIP with a copper lead frame, has more than enough thermal conductance from junction to ambient to support operation at an ambient temperature of +50°C. The SG3626M driver would be specified for this application.

SUPPLY BYPASSING

Since the SG1626 can deliver peak currents above 3 A under some load conditions, adequate supply bypassing is essential for proper operation. Two capacitors in parallel are recommended to guarantee low supply impedance over a wide bandwidth: a 0.1 µF ceramic disk capacitor for high frequencies, and a 4.7 µF solid tantalum capacitor for energy storage. In military applications, a CK05 or CK06 ceramic operator with a CSR-13 tantalum capacitor is an effective combination. For commercial applications, any low-inductance ceramic disk capacitor teamed with a Sprague 150D or equivalent low ESR capacitor will work well. The capacitors must be located as close as physically possible to the V_{CC} pin, with combined lead and pc board trace lengths held to less than 0.5 inches.

GROUNDING CONSIDERATIONS

Since ground is both the reference potential for the driver logic and the return path for the high peak output currents of the driver, use of a low-inductance ground system is essential. A ground plane is highly recommended for best performance. In dense, high performance applications a 4-layer pc board works best; the 2 inner planes are dedicated to power and ground distribution, and signal traces are carried by the outside layers. For cost-sensitive designs a 2-layer board can be made to work, with one layer dedicated completely to ground, and the other to power and signal distribution. A great deal of attention to component layout and interconnect routing is required for this approach.

LOGIC INTERFACE

The logic input of the 1626 is designed to accept standard DC-coupled 5 V logic swings, with no speed-up capacitors required. If the input signal voltage exceeds 6 V, the input pin must be protected against the excessive voltage in the HIGH state. Either a high speed blocking diode must be used, or a resistive divider to attenuate the logic swing is necessary.

LAYOUT FOR HIGH SPEED

The SG1626 can generate relatively large voltage excursions with rise and fall times around 20-30 nanoseconds with light capacitive loads. A Fourier analysis of these time domain signals will indicate strong energy components at frequencies much higher than the basic switching frequency. These high frequencies can induce ringing on an otherwise ideal pulse if sufficient inductance occurs in the signal path (either the positive signal trace or the ground return). Overshoot on the rising edge is undesirable because the excess drive voltage could rupture the gate oxide of a power MOSFET. Trailing edge undershoot is dangerous because the negative voltage excursion can forward-bias the parasitic PN substrate diode of the driver, potentially causing erratic operation or outright failure.

Ringing can be reduced or eliminated by minimizing signal path inductance, and by using a damping resistor between the drive output and the capacitive load. Inductance can be reduced by keeping trace lengths short, trace widths wide, and by using 2oz. copper if possible. The resistor value for critical damping can be calculated from:

$R_D = 2\sqrt{L/C_L}$ [2]

where L is the total signal line inductance, and C_L is the load capacitance. Values between 10 and 100 Ω are usually sufficient. Inexpensive carbon composition resistors are best because they have excellent high frequency characteristics. They should be located as close as possible to the gate terminal of the power MOSFET.

Typical Applications

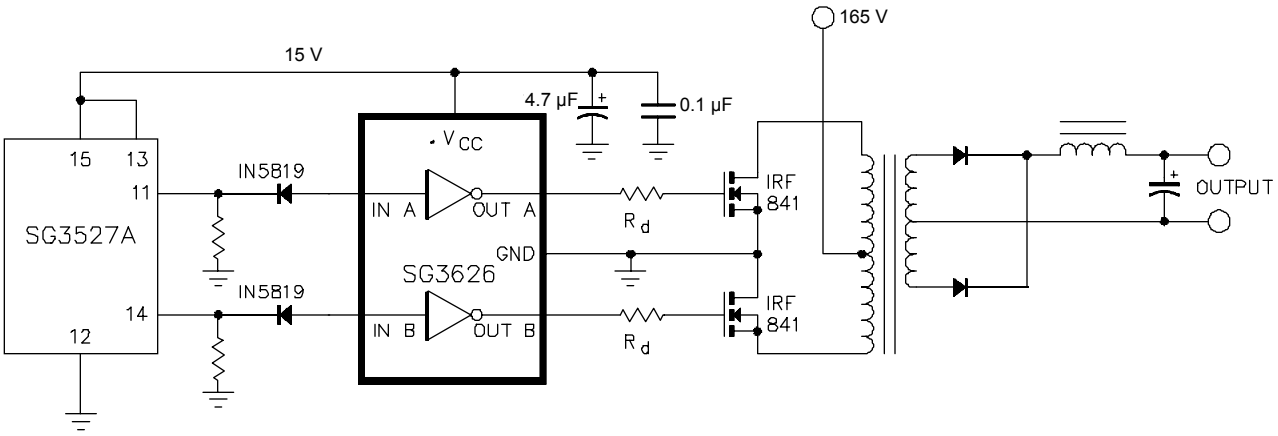


Figure 12.
When the SG3626 is driven from a totem-pole source with a peak output greater than 6 V, a low-current, fast-switching blocking diode is required at each logic input for protection. In this push-pull converter, the inverted logic outputs of the 3527A are ideal control sources for the power driver.

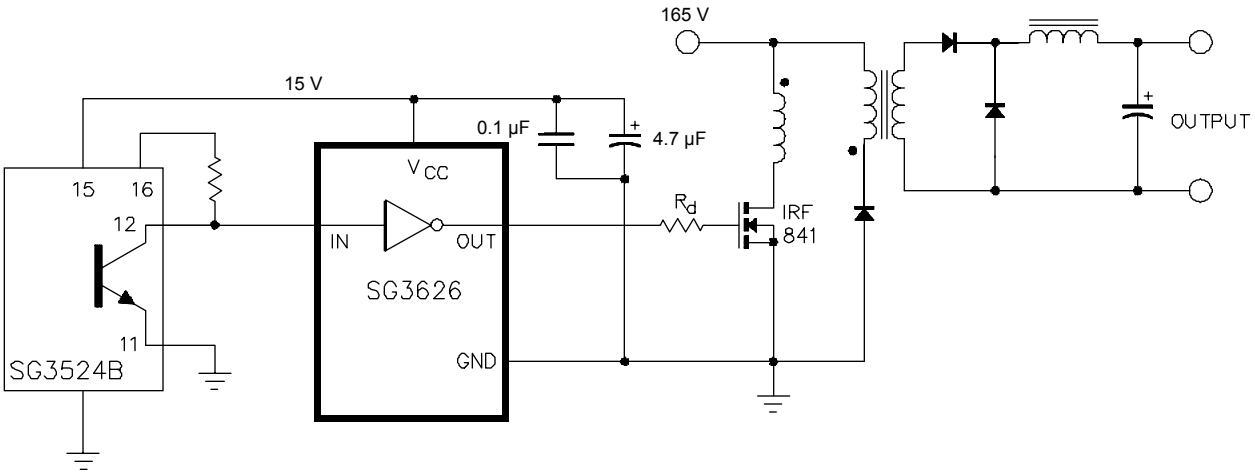


Figure 13.

In this forward converter circuit, the control capabilities of the SG3524B PWM are combined with the powerful totem-pole drivers found in the SG3626. This inexpensive configuration results in very fast charge and discharge of the power MOSFET gate capacitance for efficient switching.

Typical Applications (Continued)

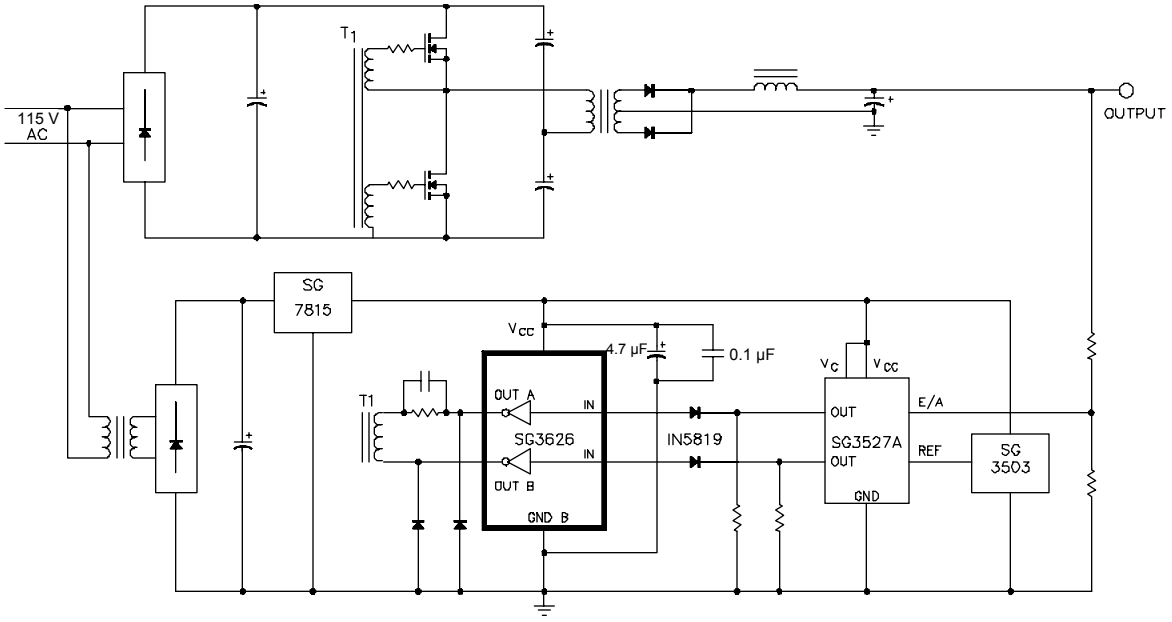


Figure 14.
In half or full-bridge power supplies, driving the isolation transformers directly from the PWM can cause excessive IC temperatures, especially above 100 kHz. This circuit uses the high drive capacity of the SG3626 to solve the problem.

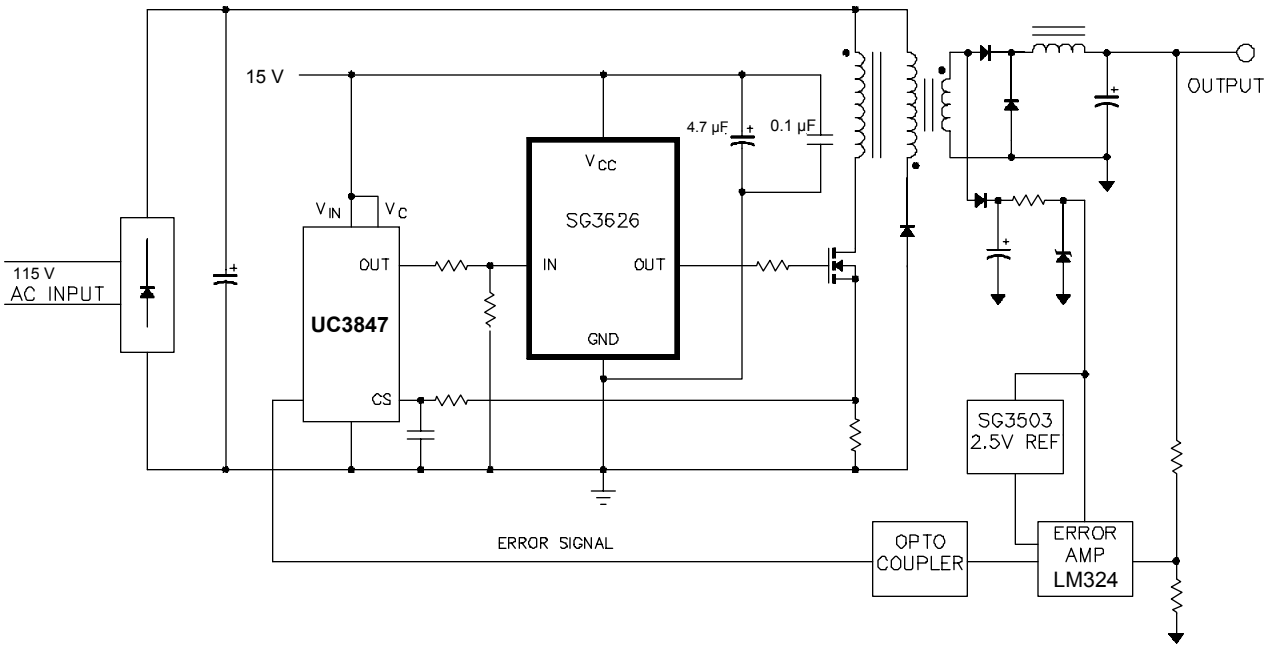
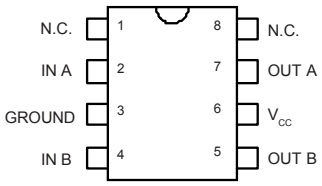
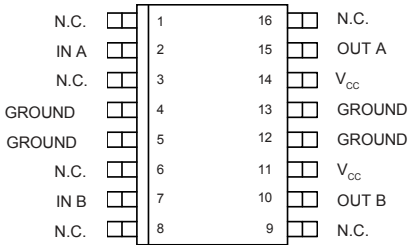
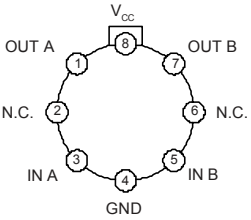
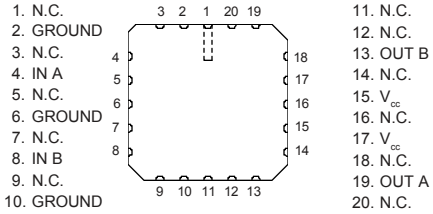


Figure 15.
A low-impedance resistive divider network can also be used as the interface between the PWM high-voltage logic output and the SG3626 power driver. In this 200 kHz current mode converter, the UC3847 provides control, while the SG3626 provides high power drive and minimizes ground spiking in the control IC.

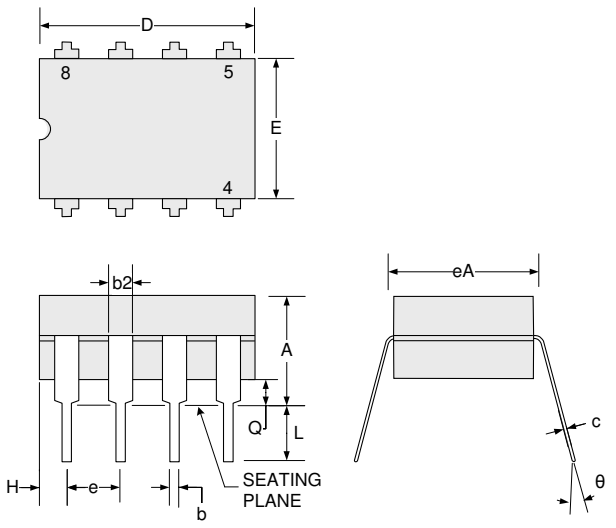
Connection Diagrams and Ordering Information (See Notes Below)

Package	Part Number	Ambient Temperature Range	Connection Diagram
8-PIN CERAMIC DIP Y - PACKAGE	SG1626Y-883B SG1626Y-DESC SG1626Y	-55°C to 125°C -55°C to 125°C -55°C to 125°C	
8-PIN PLASTIC DIP M - PACKAGE	SG2626M SG3626M	-25°C to 85°C 0°C to 70°C	M Package: RoHS Compliant / Pb-free Transition DC: 0503 M Package: RoHS / Pb-free 100% Matte Tin Lead Finish
16-PIN WIDE BODY PLASTIC SOIC DW - PACKAGE	SG2626DW SG3626DW	-25°C to 85°C 0°C to 70°C	 DW Package: RoHS Compliant / Pb-free Transition DC: 0516 DW Package: RoHS / Pb-free 100% Matte Tin Lead Finish
8-PIN TO-99 METAL CAN T - PACKAGE	SG1626T-DESC	-55°C to 125°C	
20-PIN CERAMIC (LCC) LEADLESS CHIP CARRIER L- PACKAGE	SG1626L-883B	-55°C to 125°C	

Note 1. Contact factory for DESC product availability.
2. All packages are viewed from the top.
3. Hermetic Packages Y, T, & L use Sn63/Pb37 hot solder lead finish, contact factory for availability of RoHS versions.

Package Outline Dimensions

Controlling dimensions are in inches, metric equivalents are shown for general information.

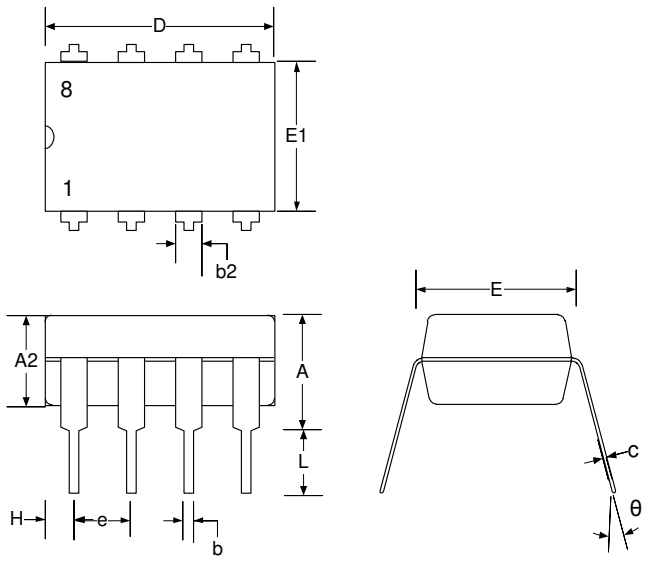


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.08	0.170	0.200
b	0.38	0.51	0.015	0.020
b2	1.04	1.65	0.045	0.065
c	0.20	0.38	0.008	0.015
D	9.52	10.29	0.375	0.405
E	5.59	7.11	0.220	0.280
e	2.54 BSC		0.100 BSC	
eA	7.37	7.87	0.290	0.310
H	0.63	1.78	0.025	0.070
L	3.18	4.06	0.125	0.160
θ	-	15°	-	15°
Q	0.51	1.02	0.020	0.040

Note:

Dimensions do not include protrusions; these shall not exceed 0.155 mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 16 · Y 8-Pin CERDIP Package Dimensions



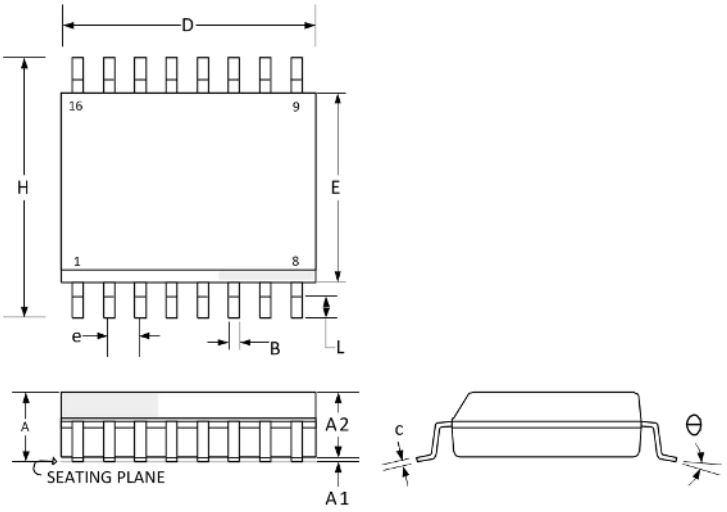
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	5.08	-	0.200
A2	3.30 Typ.		1.30 Typ.	
b	0.38	0.51	0.145	0.020
b2	0.76	1.65	0.030	0.065
c	0.20	0.38	0.008	0.015
D	-	10.16	-	0.400
E	7.62 BSC		0.300 BSC	
e	2.54 BSC		0.100 BSC	
E1	6.10	6.86	0.240	0.270
L	3.05	-	0.120	-
θ	0°	15°	0°	15°

Note:

Dimensions do not include mold flash or protrusions; these shall not exceed 0.155 mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 17 · M 8-Pin PDIP Package Dimensions

Package Outline Dimensions (continued)



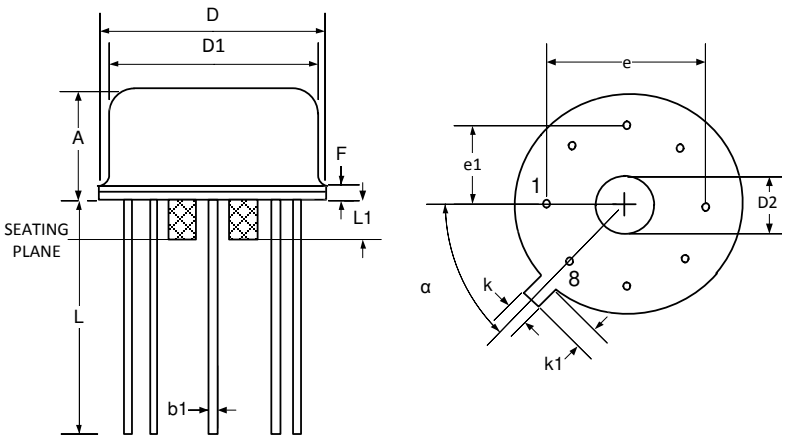
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.06	2.65	0.081	0.104
A1	0.10	0.30	0.004	0.012
A2	2.03	2.55	0.080	0.100
B	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
D	10.08	10.50	0.397	0.413
E	7.40	7.60	0.291	0.299
e	1.27 BSC		0.05 BSC	
H	10.00	10.65	0.394	0.419
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°
*LC	-	0.10	-	0.004

* Lead co planarity

Note:

Dimensions do not include protrusions; these shall not exceed 0.155 mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 18 · DW 16-Pin SOWB Package Dimensions



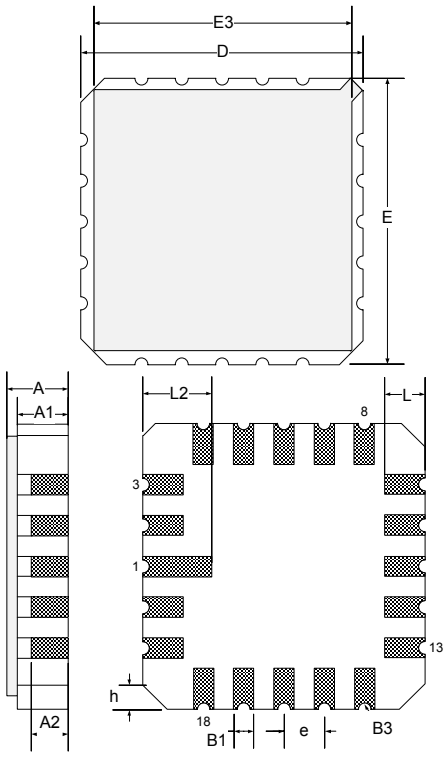
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
D	8.89	9.40	0.350	0.370
D1	8.00	8.51	0.315	0.335
A	4.191	4.699	0.165	0.185
b1	0.406	0.533	0.016	0.021
F	-	1.016	-	0.040
e1	2.54 TYP		0.100 TYP	
e	5.08 TYP		0.200 TYP	
k	0.711	0.864	0.028	0.034
k1	0.737	1.143	0.029	0.045
L	12.70	14.48	0.500	0.570
α	45° TYP		45° TYP	
D2	3.556	4.064	0.140	0.160
L1	0.254	1.016	0.010	0.040

Note:

Dimensions do not include protrusions; these shall not exceed 0.155 mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 19 · T 8-Pin Metal Can TO-99 Package Outline Dimensions

Package Outline Dimensions (continued)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
D/E	8.64	9.14	0.340	0.360
E3	-	8.128	-	0.320
e	1.270 BSC		0.050 BSC	
B1	0.635 TYP		0.025 TYP	
L	1.02	1.52	0.040	0.060
A	1.626	2.286	0.064	0.090
h	1.016 TYP		0.040 TYP	
A1	1.372	1.68	0.054	0.066
A2	-	1.168	-	0.046
L2	1.91	2.41	0.075	0.95
B3	0.203R		0.008R	

Note:
All exposed metalized area shall be gold plated 60 micro-inch minimum thickness over nickel plated unless otherwise specified in purchase order.

Figure 20 · L 20-Pin Ceramic LCC Package Outline Dimensions

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