EVALMASTERGAN2

Data brief

Demonstration board for MASTERGAN2 high power density half-bridge high voltage driver with two 650V enhanced mode GaN HEMT

Features

- Half-bridge evaluation board equipped with MASTERGAN2 and able to withstand 600 V
- VCC input on screw connector or pin strip configured for MASTERGAN2 supply voltages
- Complete set of features to drive MASTERGAN2 with single or complementary driving signal
- Embedded deadtime generator to convert single PWM signal into dual complementary LIN and HIN signals with independently adjustable deadtimes
- On board 3.3 V regulator for external circuitry supply (up to 50 mA)
- 35°C/W junction to ambient thermal resistance to evaluate large power topologies
- High frequency connector for MASTERGAN2 GL and GH pin monitoring
- Spare footprint for low-side shunt, external bootstrap diode and high voltage high capacitance bulk capacitor
- RoHS compliant

Description

The EVALMASTERGAN2 board is an easy to use and quick to adapt tool to evaluate the characteristics of MASTERGAN2 and to quickly create new topologies without the need of complete PCB design.

The EVALMASTERGAN2 provides an on-board programmable inputs deadtime generator with a single VCC supply (typ. 6 V). An embedded Linear voltage regulator offers 3.3 V rail to supply low voltage logic circuit like microcontrollers or FPGA.

Some spare footprint is also included to customize the board to operate with the final application. These customizations include: use of separate input signal or single PWM signal, use of external bootstrap diode, separate supply for VCC, PVCC or Vbo and also the use of low-side shunt resistor for peak current mode topologies.

All MASTERGAN2 pins are accessible.

The EVALMASTERGAN2 is 56 x 70 mm wide, FR-4 PCB resulting in an $R_{th(J-A)}$ of 35°C/W, without forced airflow.

Product status link
EVALMASTERGAN2

1 Architecture and components placement

Figure 1. **EVALMASTERGAN2 – top component placement**

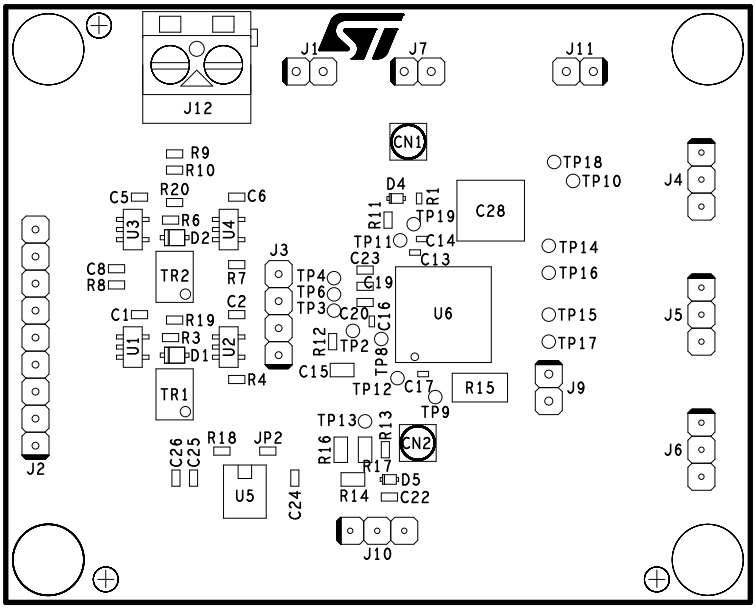
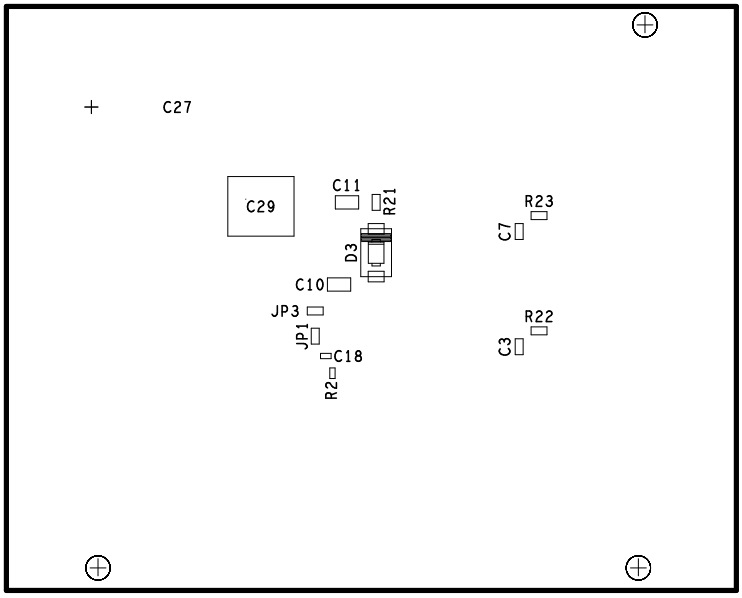


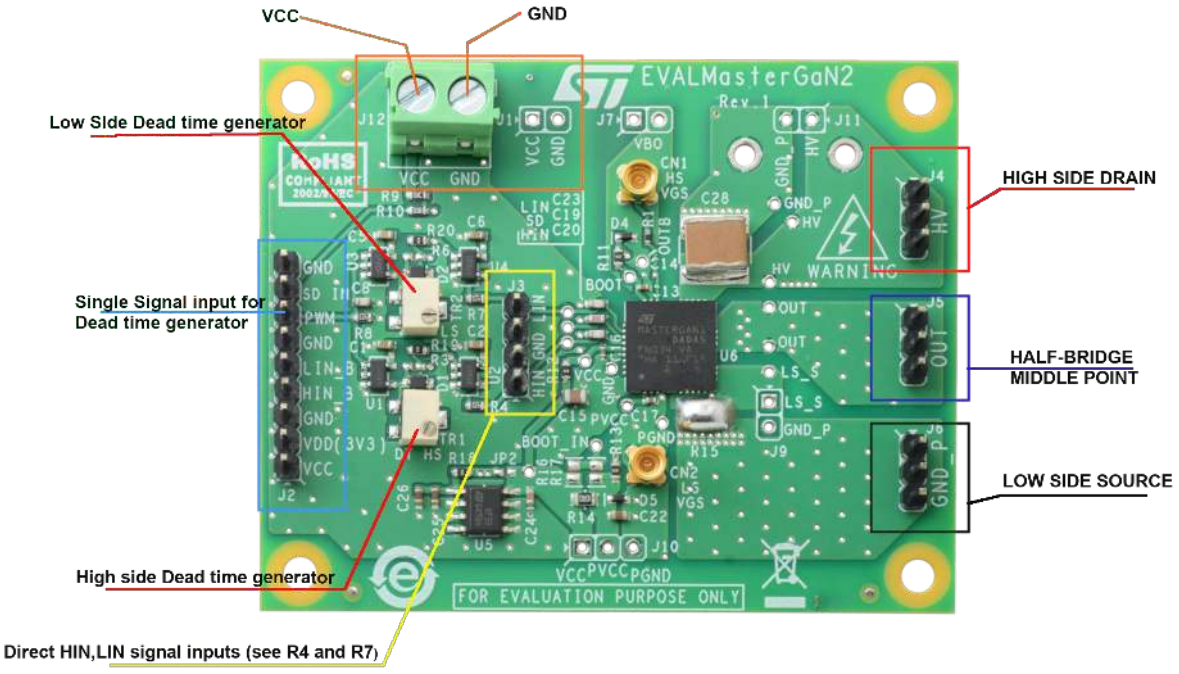
Figure 2. **EVALMASTERGAN2 – bottom component placement**



2 Board power-up and input connection

The following image shows how to supply MASTERGAN2, how to provide LIN and HIN inputs and set the programmable deadtime generator.

Figure 3. EVALMASTERGAN2 – Supply and signal connection



The LIN, HIN inputs can be supplied from the on-board deadtime generator or directly from an external generator (as DSP/MCU) with the following settings:

Table 1. Connector Map

Ref	Pin #	Name	Function	Description
J2	1	VCC	INPUT power	Board supply voltage: set to a value between 4.5 V and 6 V
	2	VDD (3V3)	OUT power	Output voltage of on-board 3.3 V regulator: it can be used to supply external circuitry (50 mA max.)
	3	GND	PWR	Board reference potential
	4	HIN_B	OUT digital	Buffered HIN signal (0-3.3 V level output)
	5	LIN_B	OUT digital	Buffered LIN signal (0-3.3 V level output)
	6	GND	PWR	Board reference potential
	7	PWM	INPUT digital	PWM input signal (0 to 3.3 V or 5 V) (see Table 3)
	8	SD_IN	INPUT digital	Disable input signal (0 to 3.3 V or 5 V) (see Table 3)
	9	GND	PWR	Board reference potential

Ref	Pin #	Name	Function	Description
J3	1	HIN	OUT (INPUT) digital	The pin is connected to HIN pin of MASTERGAN2: the pin can be used either to monitor the output of the deadtime generator or to force the input to MASTERGAN2 according to the status of R4 (see Table 2)
	2	GND	PWR	Board reference potential
	3	GND	PWR	Board reference potential
	4	LIN	OUT (INPUT) digital	The pin is connected to LIN pin of MASTERGAN2: the pin can be used either to monitor the output of the deadtime generator or to force the input to MASTERGAN2 according to the status of R7 (see Table 2)
J4	1,2,3	HV	INPUT power	These three pins are connected to VS pins of MASTERGAN2: connect high voltage potential to this pin according to MASTERGAN2 recommended values (520 V)
J5	1,2,3	OUT	OUTPUT power	These three pins are connected to OUT pins of MASTERGAN2: connect the load to this terminal (resonant tanks, transformers…)
J6	1,2,3	LS_S	POWER	These three pins are connected to SENSE pins of MASTERGAN2: the board is configured with shorted sense resistor (R15), therefore this pin can be connected to the reference voltage of high voltage potential (GND_P)
J12	1	VCC	INPUT power	Board supply voltage: set to a value between 4.5 V and 6 V
	2	GND	POWER	Board reference potential
CN1		GH	OUTPUT	To be used with proper MMCX male connector to monitor the GH pin of MASTERGAN2 with high bandwidth, high voltage differential probes (optically isolated probes are recommended)
CN2		GL	OUTPUT	To be used with proper MMCX male connector to monitor the GL pin of MASTERGAN2 with high bandwidth differential probes (optically isolated probes are recommended)

Table 2. Device input selection

R4, R7	Input source	Function and description
0-47 Ω (closed)	J2: PWM pin	LIN & HIN are generated by the on-board deadtime generator from a single PWM signal on J2, PIN 7.
Open	J3: LIN & HIN pin	Direct connection to LIN & HIN MASTERGAN2 pins. LIN, HIN input range: up to 20 V

Table 3. Input signal truth table

SD_IN	PWM	LIN	HIN
L	X	L	L
H	L	H	L
H	H	L	H

The recommended power-on sequence is to turn VCC on first, then apply the HV bus voltage. The recommended power-off sequence is to turn off the HV bus supply first, then VCC.

3 Schematic diagram

Figure 4. **EVALMASTERGAN2 schematic – High density power driver**

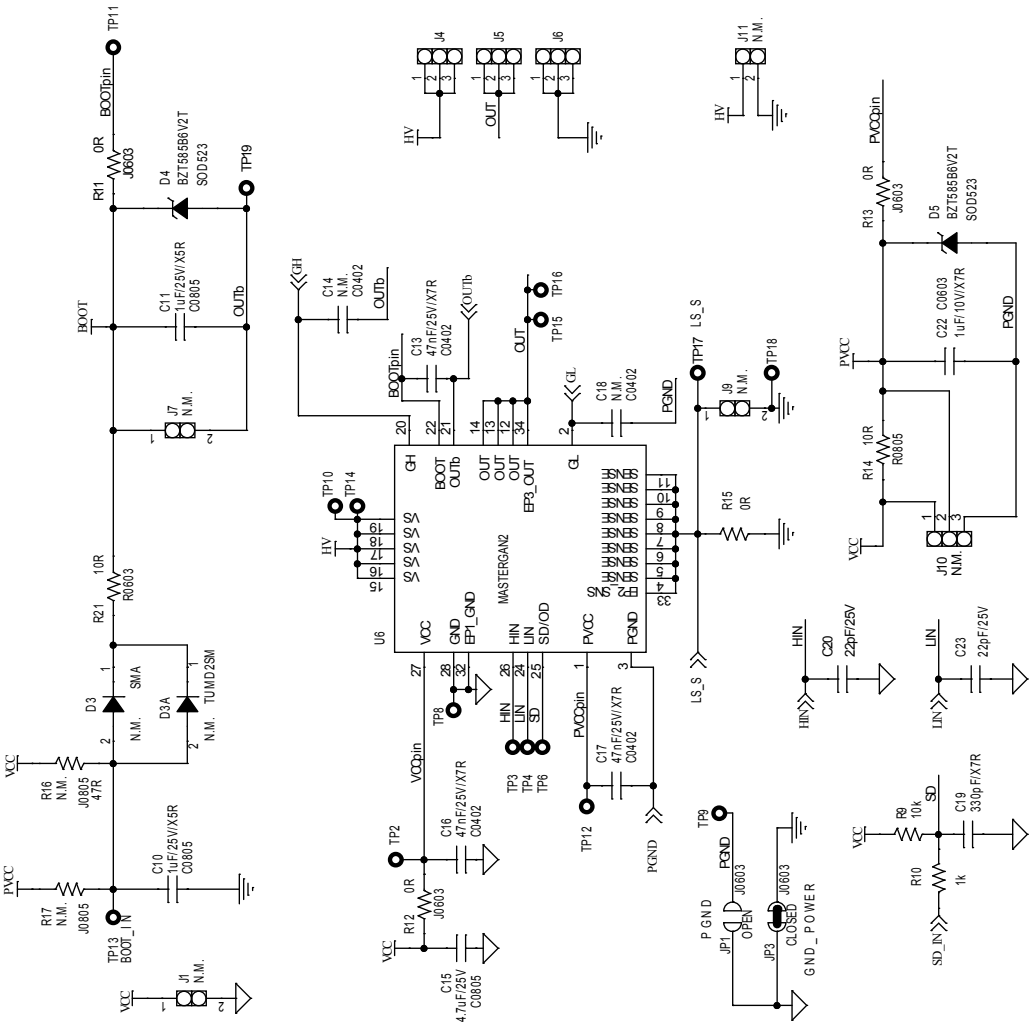
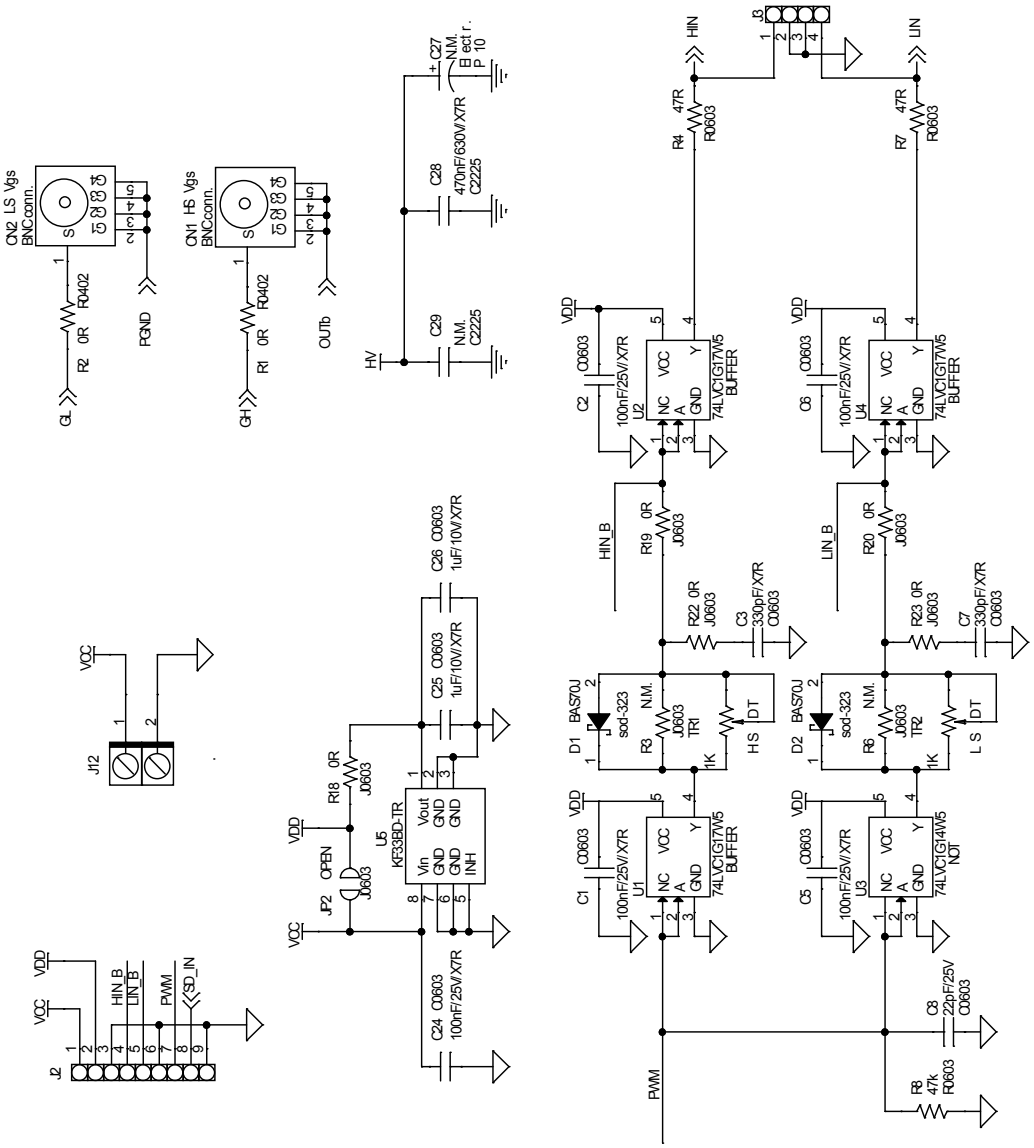


Figure 5. **EVALMASTERGAN2 schematic – Deadtime generator and connectors**



4 Bill of material

Table 4. **Bill of material**

Item	Q.ty	Ref.	Value	Description	Manufacturer	Part Number
1	2	CN1, CN2	BNC connector	MMCX straight receptacle	Cinch	135-3701-201
2	5	C1, C2, C5, C6, C24	100nF/X7R, Size 0603, 25 V,	SMT ceramic capacitor		
5	2	C10, C11	1uF/X5R, size 0805, 25 V,	SMT ceramic capacitor		
6	3	C13, C16, C17	47nF/X7R, size 0402, 25 V,	SMT ceramic capacitor		
7	2	C14, C18	N.A., size 0402,	SMT ceramic capacitor		
8	1	C15	4.7uF/X7R, size 0805, 25 V,	SMT ceramic capacitor		
9	3	C22, C25, C26	1uF/X7R, size 0603, 10 V,	SMT ceramic capacitor		
10	1	C27	N.A.	Electrolytic Cap, diam. 22 p. 10,		
11	1	C28	470nF/X7R, size 2225, 630 V,	SMT ceramic capacitor		
12	1	C29	N.A., size 2225, 630 V,	SMT ceramic capacitor		
13	2	D1, D2	BAS70J	Schottky diodes	STMicroelectronics	BAS70JFILM
14	1	D3	N.A.	600 V, 1 A, Turbo 2 ultrafast high voltage rectifier	STMicroelectronics	STTH1R06A
15	1	D3A	N.A.	600 V, 0.2 A super-fast recovery diodes	ROHM Semiconductor	RFU02VSM6S
16	2	D4, D5	BZT585B6V2T	ZENER 6.2 V 300 mW	Diodes Incorporated	BZT585B6V2T
17	2	JP1, JP2	OPEN, soldering pads,	SMT jumper		
18	3	J1, J7, J9	N.A.	Strip connector 2 pos, 2.54 mm		
19	1	J2	STRIP 1x9	Strip connector 9 pos, 2.54 mm		
20	1	J3	STRIP 1x4	Strip connector 4 pos, 2.54 mm		
21	3	J4, J5, J6	STRIP 1x3	Strip connector 3 pos, 2.54 mm		
22	1	J10	N.A.	Strip connector 3 pos, 2.54 mm		
23	1	J11	N.A.	Strip connector 2 pos, 2.54 mm		
24	1	J12	2P_screw, pitch 5.08 mm,	Terminal block T.H. 2 pos, 5.08 mm	Wurth Elektronik	691213510002
25	2	R1, R2	0R, size 0402	SMT resistor		
26	2	R3, R6	N.A., size 0603	SMT resistor		
27	2	R4, R7	47R, size 0603	SMT resistor		

Item	Q.ty	Ref.	Value	Description	Manufacturer	Part Number
28	1	R8	47k, size 0603	SMT resistor		
29	1	R9	10k, size 0603,	SMT resistor		
30	1	R10	1k, size 0603,	SMT resistor		
31	9	R11, R12, R13, R18, R19, R20, R22, R23, JP3	0R, size 0603,	SMT resistor		
32	1	R14	10R, size 0805,	SMT resistor		
33	1	R15	CLOSED, soldering pads,	SMT jumper		
34	2	R16, R17	N.A., size 0603,	SMT resistor		
35	1	R21	10R, size 0603,	SMT resistor		
37	2	TR1, TR2	1K, 12 turns	5 mm 12 turns Surface Mount Miniature Trimmers	BOURNS	3224W-1-102E
38	3	U1, U2, U4	74LVC1G17W5	Single Schmitt-Trigger Buffer Buffer	Diodes Incorporated	74LVC1G17W5 / -7
39	1	U3	74LVC1G14W5	Single Schmitt-Trigger Buffer Inverter	Diodes Incorporated	74LVC1G14W5 / -7
40	1	U5	KF33BD-TR	Very low drop voltage regulators with inhibit	STMicroelectronics	KF33BD-TR
41	1	U6	MASTERGAN2	High power density half-bridge high voltage driver with two 650 V enhanced mode GaN HEMT	STMicroelectronics	MASTERGAN2

Revision history

Table 5. **Document revision history**

Date	Version	Changes
02-Dec-2020	1	Initial release.
05-Nov-2021	2	Modified Figure 3, 4 and 5

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