SN54ABT543A, SN74ABT543A
OCTAL REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS157F – JANUARY 1991 – REVISED MAY 1997

- **State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation**

- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**

- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**

- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**

- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (NT) and Ceramic (JT) DIPs**

SN54ABT543A . . . JT OR W PACKAGE
SN74ABT543A . . . DB, DW, NT, OR PW PACKAGE
(TOP VIEW)

$\overline{LEBA}$	1	24	V_{CC}
$\overline{OEBA}$	2	23	$\overline{CEBA}$
A1	3	22	B1
A2	4	21	B2
A3	5	20	B3
A4	6	19	B4
A5	7	18	B5
A6	8	17	B6
A7	9	16	B7
A8	10	15	B8
$\overline{CEAB}$	11	14	$\overline{LEAB}$
GND	12	13	$\overline{OEAB}$
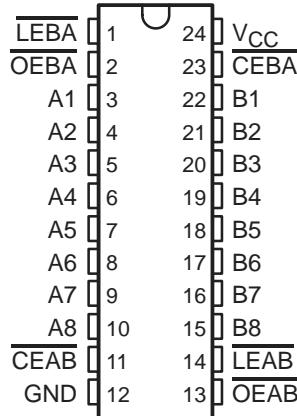
SN54ABT543A . . . FK PACKAGE
(TOP VIEW)

Top row pins: A1, $\overline{OEBA}$, $\overline{LEBA}$, NC, V_{CC}, $\overline{CEBA}$, B1
Pin numbers top: 4 3 2 1 28 27 26

A2	5	25	B2
A3	6	24	B3
A4	7	23	B4
NC	8	22	NC
A5	9	21	B5
A6	10	20	B6
A7	11	19	B7

Bottom pin numbers: 12 13 14 15 16 17 18
Bottom row pins: A8, $\overline{CEAB}$, GND, NC, $\overline{OEAB}$, $\overline{LEAB}$, B8
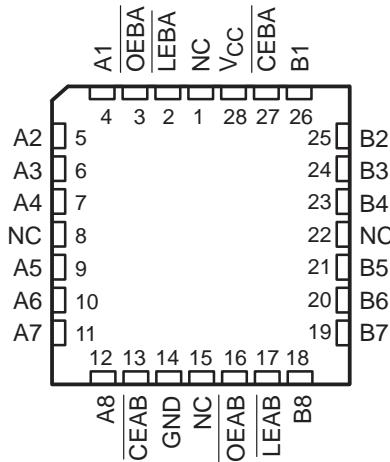
NC – No internal connection

description

The 'ABT543A octal transceivers contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT543A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT543A is characterized for operation from –40°C to 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

FUNCTION TABLE†

INPUTS				OUTPUT B
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.

‡ Output level before the indicated steady-state input conditions were established

logic symbol§
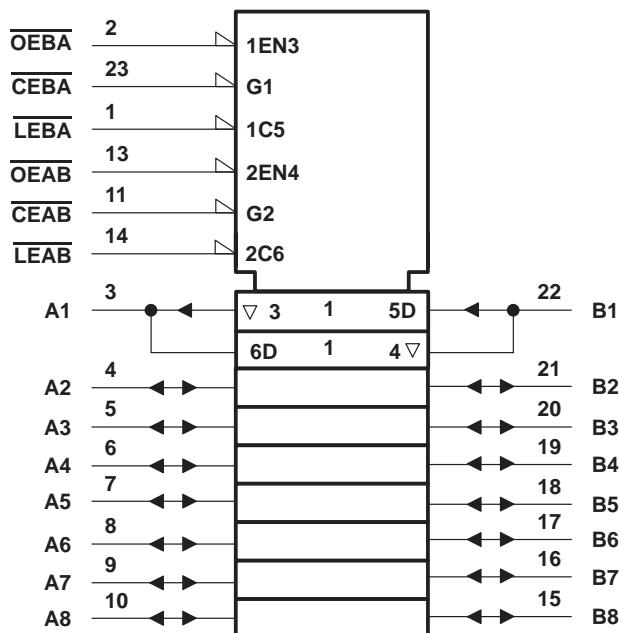
§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.

logic diagram (positive logic)

To Seven Other Channels
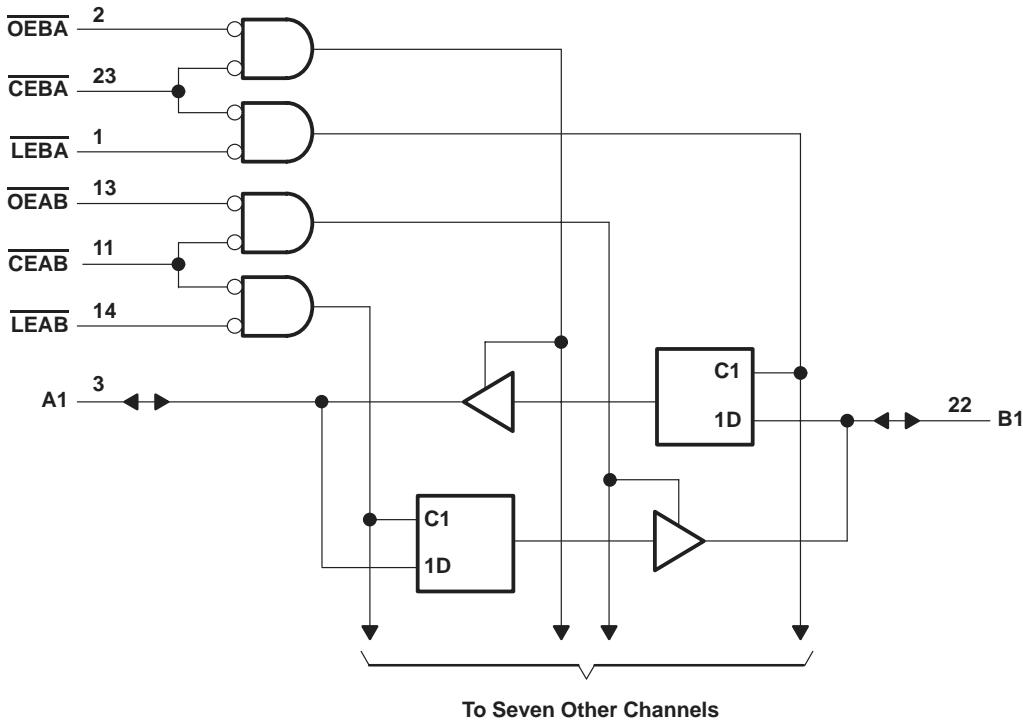
Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) .... −0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O .... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT543A .... 96 mA
                                           SN74ABT543A .... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) .... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) .... −50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package .... 104°C/W
                                                DW package .... 81°C/W
                                                NT package .... 67°C/W
                                                PW package .... 120°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

			SN54ABT543A		SN74ABT543A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A = 25°C$			SN54ABT543A		SN74ABT543A		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2		−1.2		−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.5			2.5		2.5		V
		V_{CC} = 5 V,	I_{OH} = −3 mA	3			3		3		
		V_{CC} = 4.5 V	I_{OH} = −24 mA	2			2				
			I_{OH} = −32 mA	2*					2		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 48 mA			0.55		0.55			V
			I_{OL} = 64 mA			0.55*				0.55	
V_{hys}					100						mV
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = V_{CC} or GND			±1		±1		±1	µA
	A or B ports					±100		±100		±100	
I_{OZH}‡		V_{CC} = 5.5 V,	V_O = 2.7 V			10§		10§		10§	µA
I_{OZL}‡		V_{CC} = 5.5 V,	V_O = 0.5 V			−10§		−10§		−10§	µA
I_{off}		V_{CC} = 0,	V_I or V_O ≤ 4.5 V			±100				±100	µA
I_{CEX}		V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶		V_{CC} = 5.5 V,	V_O = 2.5 V	−50*	−100	−180*	−50	−200	−50	−180	mA
I_{CC}	A or B ports	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		1	250*		350		250	µA
			Outputs low		24	30*		34		30	mA
			Outputs disabled		0.5	250*		350		250	µA
ΔI_{CC}#		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	Control inputs	V_I = 2.5 V or 0.5 V			4						pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V			7						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at V_{CC} = 5 V.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ This data sheet limit may vary among suppliers.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ABT543A			UNIT
			V_{CC} = 5 V, T_A = 25°C		MIN MAX	
			MIN MAX			
t_w	Pulse duration, LEAB or LEBA low		3.5		3.5	ns
t_{su}	Setup time	Data before LEAB or LEBA↑	High	2.5	2.5	ns
			Low	3	3	
		Data before CEAB or CEBA↑	High	2.5	2.5	
			Low	3	3	
t_h	Hold time	Data after LEAB or LEBA↑		1	1	ns
		Data after CEAB or CEBA↑		1	1	

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

|			SN74ABT543A			UNIT
			V_{CC} = 5 V, T_A = 25°C		MIN MAX	
			MIN MAX			
t_w	Pulse duration, LEAB or LEBA low		3.5		3.5	ns
t_{su}	Setup time	Data before LEAB or LEBA↑	High	3.5	3.5	ns
			Low	3	3	
		Data before CEAB or CEBA↑	High	3.5	3.5	
			Low	3	3	
t_h	Hold time	Data after LEAB or LEBA↑		0.5	0.5	ns
		Data after CEAB or CEBA↑		0.5	0.5	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT543A					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	1.6†	4.4	4.4	1.6†	5.5	ns
t_{PHL}			1.6	4.4	5.1	1.6	6.2	
t_{PLH}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	1.6†	4.1	5.1	1.6†	6.6	ns
t_{PHL}			1.6	4.6	5.4	1.6	6.4	
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	1.4	3.9	4.1	1.4	5.1	ns
t_{PZL}			2	5	4.9	2	5.8	
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	2.5†	5.9	5.8	2.5†	6.9	ns
t_{PLZ}			2.5†	5.5	6.1	2.5†	7.6	
t_{PZH}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	1.4	3.9	4.7	1.4	5.6	ns
t_{PZL}			2	5	5.7	2	6.2	
t_{PHZ}	CEBA or CEAB	A or B	3.2†	5.9	6.5	3.2†	7.3	ns
t_{PLZ}			2.5†	5.5	6.7	2.5†	7.8	

† This data sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT543A					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	1.8†	4.4	5.9	1.8†	6.9	ns
t_{PHL}			1.9	4.4	5.9	1.9	6.9	
t_{PLH}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	1.5†	4.1	5.6	1.5†	6.6	ns
t_{PHL}			2.1	4.6	6.1	2.1	7.1	
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	1.4	3.9	5.4	1.4	6.4	ns
t_{PZL}			2.5	5	6.5	2.5	7.5	
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	2.5†	5.9	7.4	2.5†	8.4	ns
t_{PLZ}			2.5†	5.5	7	2.5†	8	
t_{PZH}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	1.4	3.9	5.4	1.4	6.4	ns
t_{PZL}			2.5	5	6.5	2.5	7.5	
t_{PHZ}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	2.9†	5.9	7.4	2.9†	8.4	ns
t_{PLZ}			2.4†	5.5	7	2.4†	8	

† This data sheet limit may vary among suppliers.

PARAMETER MEASUREMENT INFORMATION
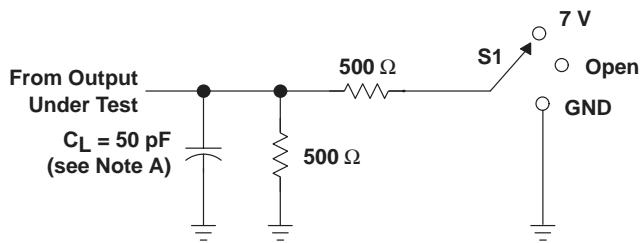
| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT
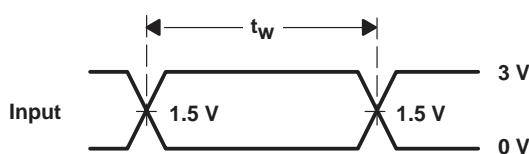
VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
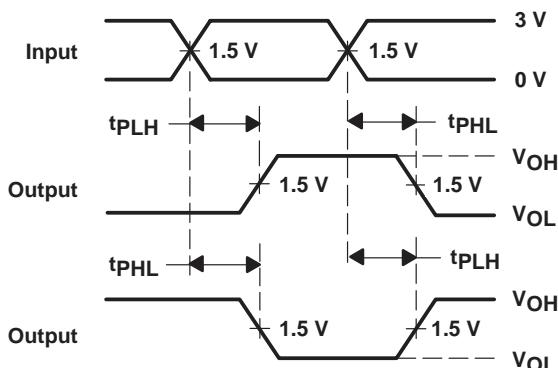
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS
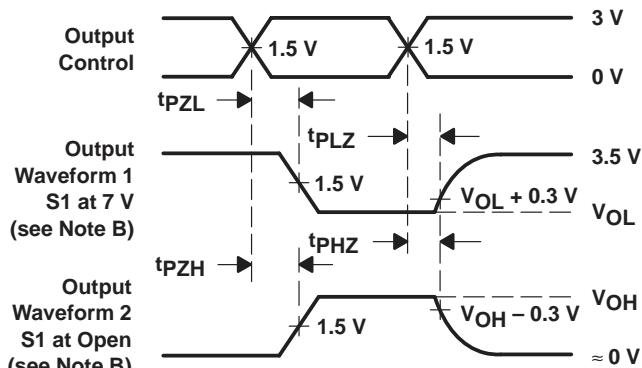
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

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Products ⊿   Applications ⊿   Support ⊿

SN54ABT543A, Octal Registered Transceiver With 3-State Outputs
DEVICE STATUS: ACTIVE

PARAMETER NAME	SN54ABT543A	SN74ABT543A
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.5 to 5.5
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		-32/64
No. of Outputs	8	8
Logic	True	True
Static Current		15.12
th (ns)		0.5
tpd max (ns)		6.2
tsu (ns)		3.5

FEATURES   ▲Back to Top

- State-of-the-Art *EPIC*-II *B*^{TM} BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C
- High-Drive Outputs (-32-mA I_{OH}, 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (NT) and Ceramic (JT) DIPs

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DESCRIPTION   ▲Back to Top

The 'ABT543A octal transceivers contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (LEAB\ or LEBA\) and output-enable (OEAB\ or OEBA\) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (CEAB\) input must be low to enter data from A or to output data from B. If CEAB\ is low and LEAB\ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB\ puts the A latches in the storage mode. With CEAB\ and OEAB\ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the CEBA\, LEBA\, and OEBA\ inputs.

To ensure the high-impedance state during power up or power down, OE\ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT543A is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT543A is characterized for operation from -40°C to 85°C.

TECHNICAL DOCUMENTS   ▲Back to Top

To view the following documents, Acrobat Reader 4.0 is required.

Product Folder: SN54ABT543A, Octal Registered Transceiver With 3-State Outputs

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

Full datasheet in Acrobat PDF: sn54abt543a.pdf (127 KB, Rev.F) (Updated: 05/01/1997)

APPLICATION NOTES

View Application Notes for Digital Logic

- Advanced BiCMOS Technology (ABT) Logic Characterization Information (Rev. B) (SCBA008B - Updated: 06/01/1997)
- Advanced BiCMOS Technology (ABT) Logic Enables Optimal System Design (Rev. A) (SCBA001A - Updated: 03/01/1997)
- Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs (Rev. A) (SCBA012A - Updated: 08/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Family of Curves Demonstrating Output Skews for Advanced BiCMOS Devices (Rev. A) (SCBA006A - Updated: 12/01/1996)
- Implications of Slow or Floating CMOS Inputs (Rev. C) (SCBA004C - Updated: 02/01/1998)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- Power-Up 3-State (PU3S) Circuits in TI Standard Logic Devices (SZZA033 - Updated: 05/10/2002)
- Quad Flatpack No-Lead Logic Packages (Rev. C) (SCBA017C - Updated: 11/22/2002)
- TI IBIS File Creation, Validation, and Distribution Processes (SZZA034 - Updated: 08/29/2002)
- Understanding Advanced Bus-Interface Products Design Guide (SCAA029, 253 KB - Updated: 05/01/1996)
- Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh (Rev. A) (SZZA036A - Updated: 02/27/2003)

MORE LITERATURE

- Enhanced Plastic Portfolio Brochure (SGZB004, 387 KB - Updated: 08/19/2002)
- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB - Updated: 07/28/2000)
- Military Brief (SGYN138, 803 KB - Updated: 10/10/2000)
- Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet (Rev. A) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- Palladium Lead Finish User's Manual (SDYV001, 2041 KB - Updated: 11/01/1996)
- QML Class V Space Products Military Brief (Rev. A) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

- LOGIC Pocket Data Book (SCYD013, 4837 KB - Updated: 12/05/2002)

PRICING/ AVAILABILITY/ PKG

DEVICE INFORMATION Updated Daily									TI INVENTORY STATUS As Of 09:00 AM GMT, 17 Apr 2003			REPORTED DISTRIBUTOR INVENTORY As Of 09:00 AM GMT, 17 Apr 2003		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE | PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY	IN STOCK	IN PROGRESS QTY | DATE	LEAD TIME	DISTRIBUTOR COMPANY | REGION	IN STOCK	PURCHASE
5962-9231402Q3A	ACTIVE	LCCC (FK) | 28	-55 TO 125		View Contents	1KU | 8.08	1	27*	3556 | 20 May	8 WKS	Avnet | Americas	2	BUY NOW
									> 10k | 27 May				
5962-9231402QKA	ACTIVE	CFP (W) | 24	-55 TO 125		View Contents	1KU | 8.58	1	15*	> 10k | 20 May	8 WKS	None Reported View Distributors		
5962-9231402QLA	ACTIVE	CDIP (JT) | 24	-55 TO 125		View Contents	1KU | 4.86	1	89*	> 10k | 20 May	8 WKS	Avnet | Americas	35	BUY NOW
SNJ54ABT543AFK	ACTIVE	LCCC (FK) | 28	-55 TO 125	5962-9231402Q3A	View Contents	1KU | 8.08	1	113*	387 | 12 May	8 WKS	None Reported View Distributors		

Product Folder: SN54ABT543A, Octal Registered Transceiver With 3-State Outputs

										3801 | 20 May					
										> 10k | 27 May					
SNJ54ABT543AJT	ACTIVE	CDIP (JT)	| 24	-55 TO 125	5962-9231402QLA	View Contents	1KU | 4.86	1	88*	> 10k | 20 May	8 WKS	EBV Electronik | Europe	225	BUY NOW
BUY NOW												Avnet-SILICA | Europe	5	BUY NOW
SNJ54ABT543AW	ACTIVE	CFP (W)	| 24	-55 TO 125	5962-9231402QKA	View Contents	1KU | 8.58	1	0*	> 10k | 20 May	8 WKS	None Reported View Distributors		

Table Data Updated on: 4/17/2003