AVR454 Users Guide - ATAVRSB100 - Smart Battery Development Board

Features

- **Evaluation of ATmega406 as a smart battery controller**
- **Cell voltage simulator**
- **Charge/discharge current simulator**
- **18-bit Coulomb Counter ADC for current measurements**
  - **Both regular and accumulation mode**
- **12-bit Voltage ADC for cell voltage measurements**
- **Battery protection in CPU-independent Hardware**
  - **Deep under-voltage, over-current and short circuit protection**
- **SMBus communication interface**
- **Low-power modes**
- **Internal temperature sensor**

1 Introduction

This document describes the ATAVRSB100 (SB100) smart battery development board. The SB100 is designed for evaluation of the Atmel AVR ATmega406, which is designed for smart battery applications. The ATmega406 is designed for battery packs with 2, 3 or 4 Li-Ion cells in series.

The hardware described in this Application Note can be ordered through distribution as ATAVRSB100.

An evaluation firmware for smart battery is available as Application Note AVR453, which can be downloaded from the Atmel web site.

Figure 1-1. The ATAVRSB100 development board

8-bit AVR® Microcontrollers

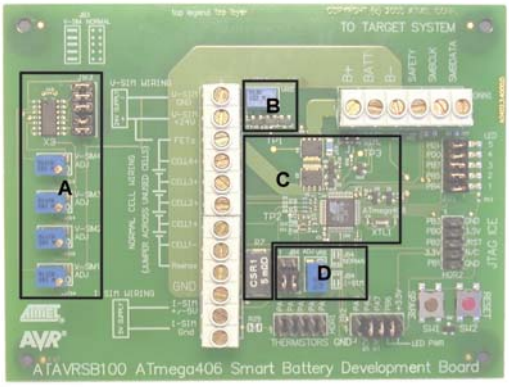
Application Note

Rev. 2598C-AVR-06/06

2 The SB100 Hardware

The SB100 consists of two main areas; the circuitry required for the smart battery implementation and a simulator circuit for demonstrating the ATmega406 smart battery designs capabilities. Figure 2-1 shows the areas on the SB100 board.

Figure 2-1. SB100 with smart battery and simulator circuits highlighted



A – Individual cell voltage simulation

B – Total cell stack voltage simulation

C – smart battery implementation

D – Charge/discharge current simulation

In addition to the circuits that demonstrate the smart Battery features, a number of connectors are available for in-system programming, on-chip debugging, SMBus communication, connection of battery cells and more.

The hardware schematic, assembly drawings and Bill of Materials are found last in this document. A Table of Contents is found on page 19.

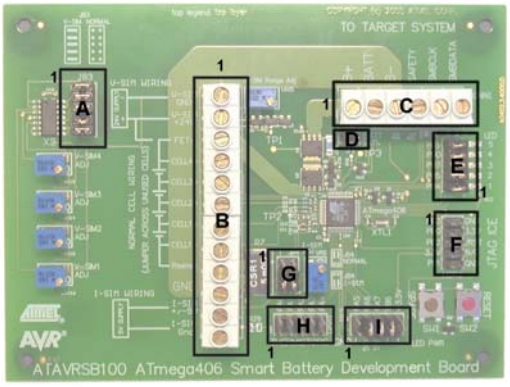
The ATmega406 comes preprogrammed with the evaluation software described in the AVR453 Application Note. It is however recommended to download the latest revision of the firmware from the Atmel website.

WARNING:	Li-Ion batteries must be handled with care as they may pose a safety hazard if treated incorrectly. It is important that the development of smart Battery applications are done by people that are skilled and knowledgeable of correct use and handling of Li-Ion batteries.

2.1 Connecting the SB100

To use the SB100 it needs to be connected to an SMBus host/charger, a battery pack (or a simulated battery pack) and a number of jumpers need to be configured correctly. Further, for programming and debugging it is required to hook up an Atmel JTAGICE mkII. Note that ATmega406 does not support in-system serial programming. Figure 2-2 shows the SB100 board with all connectors highlighted. The various connectors and jumper blocks and are described in detail in the following sections.

Figure 2-2. SB100 with connectors highlighted



A – JB3
B – CONN2
C – CONN1
D – J1
E – JB1
F – HDR2
G – JB4
H – HDR1
I – JB2

2.1.1 Programming and debugging (HDR2)

HDR2 provides access to the JTAG interface of the ATmega406, which is used for programming and debugging using the JTAGICE mkII. The use of JTAGICE mkII is described in the AVR Studio® online Users Guide and on the Atmel web. Note that the older JTAGICE does not work with this board.

If the emulator is not required, the I/O signals present here can be used for other purposes.

Table 2-1. HDR2: JTAG Port

Pin	Name	Direction	Usage
1	PB3 / TCK	I/O	TCK JTAG signal
2	GND		
3	PB0 / TDO	I/O	TDO JTAG signal
4	VTref	Output	+3.3V reference
5	PB2 / TMS	I/O	TMS JTAG signal
6	/RESET	Input	Reset signal
7	Vsupply	Output	+3.3V
8	n/c		
9	PB1 / TDI	I/O	TDI JTAG signal
10	GND		

2.1.2 Cell connector (CONN2) and current sense source (JB4)

CONN2 is used for connecting the battery cells in addition to power supply for the charge/discharge current and cell voltage simulators. Refer to Figure 3-1 for schematics.

Table 2-2. CONN2: Cell connections & Simulation

Pin	Name	Direction	Usage
1	VSIM GND	Input	Cell Voltage Simulator power supply (-)
2	VSIM POS	Input	Cell Voltage Simulator power supply +24V max.
3	FETS	I/O	From power MOSFETs. Connect to most positive cell connection.
4	CELL4+	I/O	Cell connection
5	CELL3+/4-	I/O	Cell connection
6	CELL2+/3-	I/O	Cell connection
7	CELL1+/2-	I/O	Cell connection
8	CELL1-	I/O	Cell connection
9	SENSEHI	I/O	Sense resistor high side
10	SENSELO	I/O	Sense resistor low side; same as B- on CONN1
11	I-SIM+/-	Input	+/-5V from current simulator power supply
12	I-SIM GND	Input	GND from current simulator power supply

JB4 controls whether the Coulomb Counter ADC receives its input from R7 (the high-accuracy 5mΩ current sense resistor), or from the Pack Current Simulator circuitry, which includes VR6.

Table 2-3. JB4: Battery Pack Current Sense Source

Pin	Name	Direction	Usage
1	Rsense		High side of current sense resistor
2	GND		Low side of current sense resistor
3	SENSEHI		Coulomb Counter high input
4	SENSELO		Coulomb Counter low input
5	I-SIM-OUT		Current simulator output voltage
6	GND		Current simulator ground

2.1.3 Wiring for battery cell simulation

Wiring CONN2 for battery simulation is shown in Figure 2-3 together with the required jumper configuration for jumper blocks J1, JB3 and JB4. The correct wiring and jumper settings are also shown on the board silkscreen. Note that the factory setting for the simulator gives a voltage too low for the smart Battery to start properly.

This section only shows the required wiring and jumper settings. Further details on battery voltage and charge/discharge current simulations are given in sections 2.4 and 2.5.

Figure 2-3. CONN2 wiring and jumper settings for battery simulation

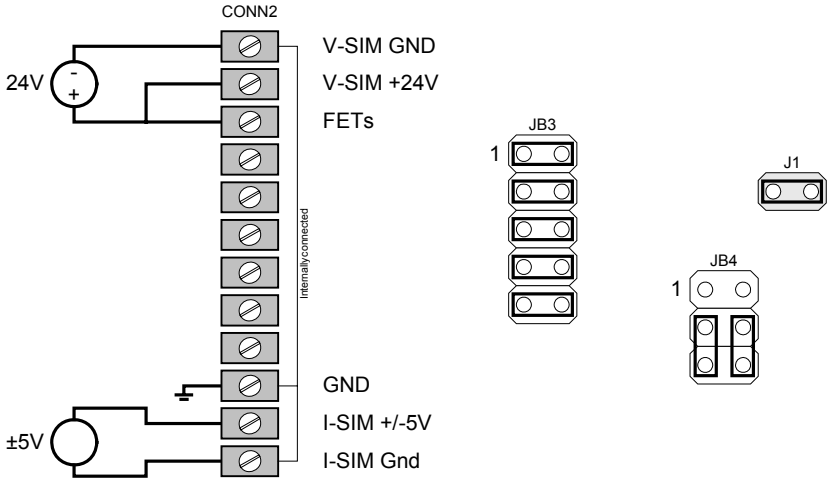


Table 2-4. JB3: Cell voltage simulation jumper block

Pin	Name	Direction	Usage
1	SIM-CELL4+		Short these two pins to connected simulated CELL4+ to smart Battery
2	CELL4+		
3	SIM-CELL3+		Short these two pins to connected simulated CELL3+ to smart Battery
4	CELL3+		
5	SIM-CELL2+		Short these two pins to connected simulated CELL2+ to smart battery
6	CELL2+		
7	SIM-CELL1+		Short these two pins to connected simulated CELL1+ to smart battery
8	CELL1+		
9	SIM-CELL1-		Short these two pins to connected simulated CELL1- to smart battery
10	CELL1-		

2.1.4 Wiring for live Li-Ion battery cells

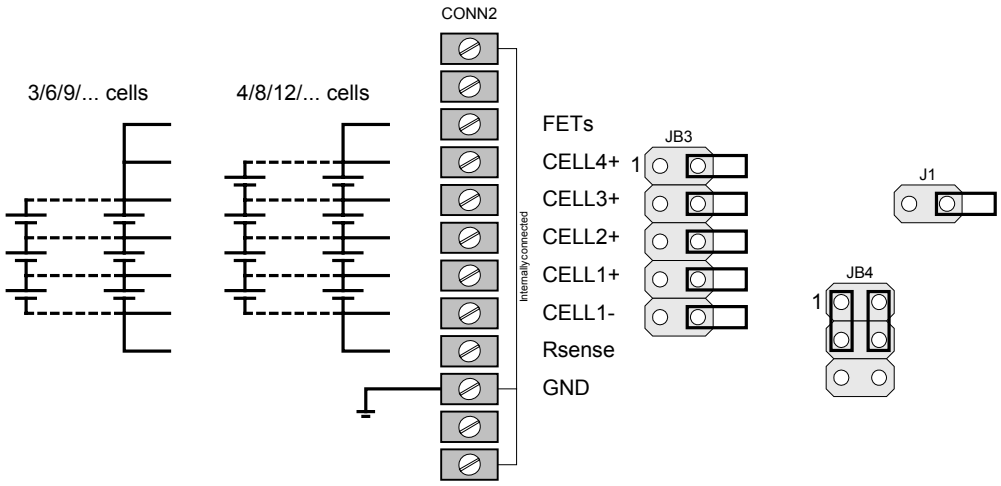
WARNING:	When using live cells, **never** leave the system unattended due to the potential hazards associated with the use of Li-Ion cells. Do not apply high charging or discharging currents to the cells until you have verified that all safety systems, both hardware and software, are functional under the specified conditions.

Normal cell wiring is shown on the SB100 board, labeled as such. The ATmega406 supports from two to four stacked Li-Ion cells. As many cells as required may be connected in parallel. A jumper should always connect CELL1- (CONN2 pin 8) to Sense Resistor High (CONN2 pin 9) to enable the current-sense resistor. Cells should always be connected on the lower positions first. The FET connection (CONN2 pin 3) should be tied to the most positive cell connection (either CELL4+, CELL3+ or CELL2+).

When using live cells, all jumpers should be removed from JB3. Additionally, the sense resistor should be connected to the CCADC inputs by shorting JB4 pins 1-3 and 2-4. It is possible to use the Current Simulator while connected to live cells simply

by changing the jumping on JB4 to pins 3-5 and 4-6. It is not necessary to rewire the CELL1- terminal to bypass the sense resistor, but this can be done if desired.

Figure 2-4. Connecting battery cells to CONN2.



If no charger is used, jumper J1 should be shorted after connecting the cells to wake up the ATmega406 from Power-Off mode.

When using only 2 cells in series, the remaining two cell inputs should be shorted, just as the one cell input is shorted when using only three cells.

2.1.5 Host/charger SMBus Connector (CONN1)

The connections between the SB100 board and a host application or smart charger are shown in Figure 2-5. Note that the Charger Active signal is only used by the charger and SB100 needs at least 8V on this input to wake up from Power-Off mode. If no Charger Active signal is available, jumper J1 could be shorted to use the battery stack voltage for the Charger Active signal instead.

Figure 2-5. Connecting a host or a charger to CONN1

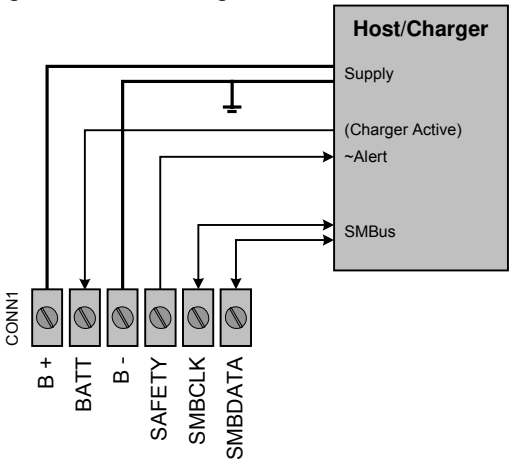


Table 2-5. CONN1: Battery Pack Connections to Host or Charger

Pin	Name	Direction	Usage
1	B+	I/O	Pack main positive high-current terminal
2	BATT	Input	Charger Active signal
3	B-	I/O	Pack main negative high-current terminal
4	SAFETY	Output	Indicates pack safe/unsafe state
5	SMBCLK	I/O	SMBus clock line
6	SMBDATA	I/O	SMBus data line

2.1.5.1 Safety Signal

The PC0 I/O pin is used for the Safety Signal, as it is high-voltage compatible and is also an output-only signal. The signal is impedance controlled. R26 provides a permanent 10K resistance to ground so that whenever the pack is connected, the Host or Charger sees a ‘Normal’ condition. When PC0 is driven low R22 provides a 1K resistance to GND, indicating a ‘Hot’ condition.

Additional I/O pins could be used, along with additional resistance values, to supply all of the Safety Signal conditions indicated in the SMBus specification (see SMBus spec. section 4.4.4 for more details).

2.1.5.2 Charger Active Signal (BATT)

When high voltage is present on the BATT pin and the AVR is in Power-Off mode, a reset to occurs, thereby waking up a ‘sleeping’ pack when a charger is connected. A diode is used to prevent internal battery voltage of the pack from being presented at the pack’s external BATT terminal. BATT is also used to power the internal high-voltage FET driver circuits for the Charge and Precharge FETs. Therefore the charger must supply a voltage equal to B+ on the BATT signal. Note that since BATT is connected via a diode as suggested, the FET pin drivers will only be able to bring the gate to within a diode-drop of the BATT signal when turned off; the gate-source resistors are left to further reduce the FET gate-source voltages to zero.

2.1.6 Test Points

The SB100 board has several test points for development purposes. Figure 2-6 shows their placements on the board.

Figure 2-6. Test point placements

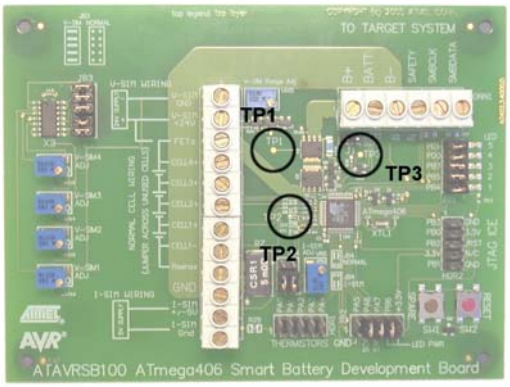


Table 2-6. Test points on SB100

Test Point Name	Description
TP1	Test Point 1 is the junction between the two primary power MOSFET devices, Q3 and Q4, and is provided for testability purposes only.
TP2	Test Point 2 is the Vref output signal. If enabled and calibrated, this should have 1.100VDC present.
TP3	Test Point 3 is the BATT signal, after passing through a dual diode device to allow enabling this signal from either a cell-side or a host-side power source. It is provided for testability purposes only.

2.2 Using the simulator stages

This chapter describes how to calibrate and use the integrated voltage simulator, and also how to use the current simulator.

2.2.1 Calibrating the Cell Simulator

Calibration of the Cell Simulator section is actually very easy due to the design of the circuitry. Since each cell's potentiometer can be independently adjusted without affecting the others, calibration does not require a great deal of back-and-forth adjustment to take place.

Due to component tolerances, the upper range of adjustment will typically exceed what can be tolerated by the ATmega406, namely, 5.5V. Care should therefore be taken not to exceed the ATmega406 voltage ratings during calibration and during development.

For most users it will be helpful to have all four cell simulation potentiometers adjusted to the same setting, with the ability to adjust each cell slightly upward if desired before reaching the upper end of the adjustment. This procedure will establish that setting.

1. Wire up the CONN2 terminal strip for simulation as indicated in Figure 2-3.
2. Install all five jumpers on JB3.
3. Adjust V-SIM1-4 (VR1-4) fully counter-clockwise to their minimum setting. The potentiometers are 12-turn, and one can hear a low click when end settings are reached and every full turn from thereafter.
4. Apply 24.0VDC to the designated V-SIM supply terminals (not to the I-SIM terminals!). Do not exceed 24.5VDC to the board at any time! Ensure that you have a ripple-free DC supply available. Some wall converters that are DC-rated do not include a filter capacitor and only output pulsed DC, which is not acceptable for use.
5. Adjust V-SIM Range Adjust (VR5) fully clockwise. This supplies the maximum current into the simulation pots.
6. Measure across CELL1+/CELL1- terminals while adjusting V-SIM1 clockwise to reach 5.25VDC.
7. Repeat step 6 for cells 2-4.

After calibration, the main power supply voltage can be reduced if so desired, as low as the maximum cell stack voltage plus 2.0VDC. Before making this adjustment, VR5 should be reduced to match the maximum stack voltage. For example, if the maximum cell voltage desired is 4.2VDC, and a four-cell stack is used, adjust VR5 to produce $4.2\mathrm{V} \cdot 4 = 16.8\mathrm{V}$ across the stack (CELL4+ to CELL1-). The power supply can then be reduced from 24V to 18.8V.

When working on packs that use either a 2-cell or a 3-cell stack, the potentiometers for cells 3 and 4 (or just cell4) should be adjusted to their minimum setting. This will reduce the required voltage at the power supply accordingly, and will also accurately reflect the behavior that will be seen in the final design. Note that the `#define` parameters in `cell.h` should be adjusted accordingly to prevent the software from detecting this as an under-voltage condition on cell 3 or cell 4.

2.2.2 Simulating Charging and Discharging

VR5, after calibration, will adjust all cell simulation voltages together. If V-SIM1-4 have been adjusted to match, they will track each other very accurately while VR5 is adjusted.

In most cases, then, adjusting VR5 by itself will be all that is required when simulating charging and discharging. If V-SIM1-4 have been adjusted to match, then it will only be necessary to monitor the total stack voltage and not individual cell voltages.

When monitoring the stack voltage, readings should be taken from the CELL1- terminal to the highest cell's positive terminal. Readings should not be taken from the power supply, as this does not reflect the simulated cell voltages.

Note that VR5 allows the voltage of the stack to be adjusted very low, simulating severely over-discharged cells. While doing this on the board, the ATmega406 is still able to operate, but in a final design the ATmega406 operating voltage would be reduced to the point where the device itself would stop functioning.

2.2.3 Simulating Cell Imbalance

Each cell's adjustment can be brought slightly higher or lower to simulate cell imbalance without affecting the other cells. Note that the adjustment is fairly sensitive, so a light touch on the cell's potentiometer is better. The voltage of any given cell may be monitored at the CELLx terminals on CONN2.

2.2.4 Current Simulation

To use the current simulation circuitry, set the jumpers on JB4 for I-SIM mode as shown in Figure 2-3, and connect a regulated, accurate 5.0VDC supply to the designated I-SIM terminals on CONN2. The polarity of the supply will determine whether you are simulating Charging or Discharging. Specifically, if the I-SIM+/-5V terminal is positive, you will be simulating Charging.

Adjusting VR6 (I-SIM ADJ) will now vary the voltage present at the ATmega406 PPI/PI/NI/NNI terminals. Rotating VR6 clockwise will increase the magnitude of the voltage present, but the polarity will be determined by the wiring of the power supply. Note that the CCADC can tolerate up to +/-0.22V, but is only specified to read in the range of +/-0.15V. Although adjusting VR6 fully may result in a voltage greater than 0.15V, this will not damage the ATmega406 device.

The simulated voltage can be measured at JB4, pins 3 and 4. Note that the amount of current indicated by this voltage will be dependent on the value of the sense resistor you use in your final design.

Since most connected systems are constant-power, when simulating discharge by means of reducing the cell voltage you should also increase the setting of VR6 to simulate higher current.

2.3 Smart battery Circuit

The ATmega406 provides a highly integrated solution that makes it easy to create an SMBus compliant smart battery device with pack capacity monitoring with both hardware and software safety features. Please see the device specification for more details.

2.3.1 Charging and discharging control

The FET transistors Q3 and Q4 provide the ability to disconnect the cells to prevent accidental external short circuits from causing damage. Q5 provides separate control over trickle charging, also referred to as pre-charging, used if the pack is over-discharged, also known as a Deep Under-voltage condition.

2.3.2 Precharge

Q5 and R27 control the Precharge circuit, whose purpose is to provide a mean to supply charging current to an over-discharged pack whose voltage may be too low to operate the ATmega406. The precharge current is limited by R27. R27 is sized so that under maximum precharge current, its power dissipation does not create an unsafe condition.

Generally the amount of precharge current required will depend on how quickly it is desired to bring the cell stack up to a voltage level at which normal charging can occur. This time depends in turn on the cell capacity. Assuming a 4-cell stack and a worst-case discharge voltage of 0V (which should never be seen in practice!), the applied charging voltage could be as high as $4.2\mathrm{V} \cdot 4 = 16.8\mathrm{V}$. To limit precharge current to 10mA, a 1.68kΩ resistor would be required. The power dissipation of this resistor would be 168mW, which would run rather hot (but not unsafely so) if implemented as a 1206-size SMD component. However, given the fact that the cells will likely never be as low as 0V, and assuming a more realistic figure such as 2.0V for an over-discharged cell, the dissipation would be $(16.8\mathrm{V} - 4 \cdot 2.0\mathrm{V})^2 / 1680\Omega = 46\mathrm{mW}$, which is quite reasonable. Different precharge current requirements and number of cells in the stack would require adjustments to this value and possibly to the physical size of the resistor.

2.3.3 Charge and discharge

Power MOSFET devices are present in virtually all Li-Ion battery packs to allow completely disconnecting the cells from the outside world. This is necessary to prevent intentional or accidental over-charge or over-discharge conditions as well as short-circuits of the pack. This is accomplished by placing two FETs (Q3 and Q4) back-to-back, allowing current flow to be stopped in both directions.

The ATmega406 provides active-low drive capability for external P-channel MOSFET devices. If all three FETs are turned off, no current can flow in or out of the pack. If either Q3 or Q4 is turned on, however, current will be allowed to flow in one direction, namely through the internal body diode of the FET that is turned off. Thus, the potential exists for overheating one or more FETs. Thus, the Discharge and Charge FETs are always turned on and off together. Since the current through the Precharge FET is limited, if that FET is on while the Discharge FET is off there will be very little heat produced by the body diode of the Discharge FET.

The PVT pin is required to be connected to the high side of the battery stack to perform its primary function, that of sensing Deep Under-voltage of the stack. Additionally, this pin is the high-side power supply for the Discharge FET driver. This arrangement creates a prerequisite that the Discharge FET to be placed closest to

the cells. Correspondingly, the Charge (and optional Precharge) FET must be positioned at the pack's main terminals. The BATT pin is therefore used to provide the high-side power supply to the Charge and Precharge FET drivers, since the BATT pin must be connected on the host/charger side of the circuit.

The Charge and Discharge FETs must be able to handle the maximum current produced or absorbed by the pack. As such, attention must be paid to their characteristics, particularly their power dissipation and current capability. The Precharge FET handles much lower current than the Charge FET, and therefore is not as critical. (This is also the reason that a low-cost FET with relatively high RdsON can be used) The Discharge FET is implemented as a separate P-channel device to allow it to dissipate power at the same time as the Charge FET, since they typically are on at the same time.

Assuming a current of 4A to be an appropriate maximum, the power dissipation of a 60mΩ FET will be 240mW. With a typical SO-8 package device used as the Discharge FET, this will yield a die temperature increase of about 12°C over ambient, which is quite acceptable. For the Charge and Precharge FETs, a dual device can be used. With an on-resistance of 35mΩ, a 4A current will yield a dissipation of 140mW in the TSSOP-8 package, with a resulting die temperature increase above ambient of 17.5°C, which is also an acceptable figure.

2.3.4 Coulomb Counter and current measurement

The PI and NI pins are the input to the Coulomb Counter ADC. Since this is a very high sensitivity input, care has been taken in the layout to ensure that leakage from other voltage sources is minimized. The layout of the ATAVRSB100 board includes GND traces, which act as leakage absorbers. It is highly recommended to not use No-Clean flux when manufacturing production boards, as such leaves a residue that may be conductive. As with all differential inputs, the same resistance value should be used for both sides of the input filter.

For best results, the sense resistor and the input filter circuitry are grouped tightly and placed as close to the ATmega406 device as possible.

2.3.5 Battery protection circuits/built-in hardware

The PPI and NNI inputs receive the voltage from the sense resistor unfiltered. This allows for quick response to short-circuit situations. No capacitance should be added to these pins. The input resistors here should also be the same value, as is standard practice on differential inputs. Increasing the value of these resistors above 1K should be avoided.

The PVT pin serves as the Deep Under-voltage sense input.

2.4 Cell voltage simulator

The ATAVRSB100 includes circuitry to accurately simulate cell voltages. Wiring details for V-SIM are shown on the SB100 board, near CONN2 pin 1. When using V-SIM mode, ensure that no external power is connected to the B+ and B- terminals on CONN1.

A constant current source supplies a series chain of four potentiometers. Since the current is regulated, adjusting any one of the potentiometers results only in a corresponding change in voltage across that potentiometer; the voltage across the others is not affected. (These signals are buffered before being presented to the CELLx inputs, and can be seen directly by measuring on the appropriate terminals of

CONN2.) Thus all cells can be set up for the same voltage, or individually varied to simulate cell imbalance conditions. The constant current source is also adjustable, permitting all cells to increase or decrease in voltage while maintaining balance between them.

Adjusting VR1-4 clockwise increases the voltage for the corresponding cell. Likewise, adjusting VR5 clockwise increases the current flow and thus the voltage of the entire cell stack. Adjusting VR5 to its maximum clockwise setting provides maximum current, limited to produce approximately 5.5VDC on each cell. Due to component tolerances, it may be necessary to avoid using the maximum possible setting of VR5 so as not to exceed 5.5VDC on any cell input. Note that the factory setting for VR1-5 gives a cell stack voltage too low for the smart battery to start properly.

For optimum adjustment range, set VR1-4 to their maximum clockwise setting, and adjust VR5 so that about 5.25V is present on one of the cell connections. Next, measure the simulated cell voltages at CONN2 and determine which of the simulated cells has the lowest voltage. Adjust the other three remaining cells to match it. The system is now calibrated. VR5 can now be used to adjust the voltage on all cells simultaneously.

To configure the ATAVRSB100 for cell voltage simulation, all five jumpers of J3 must be installed. This ties the outputs of the buffered voltage divider stages to the cell inputs. Additionally an external power supply must be connected to CONN2 pin 1 (GND) and CONN2 pin 2 (positive). The voltage supplied should be the maximum pack voltage plus about 2.0V. Example: a 4-cell stack is to be simulated, where the maximum voltage on each cell is 4.20V. The power supply should be set for $4 \cdot 4.20\text{V} + 2.0\text{V} = 18.8\text{V}$.

WARNING: Do not exceed 24V! Doing so will damage the ATAVRSB100 kit.

Note that if cell 3 and/or cell 4 are not required, the corresponding potentiometers VR3 and/or VR4 can be adjusted to their minimum setting, yielding zero volts.

2.5 Current simulation

The ATAVRSB100 includes a mechanism to simulate pack current. R21 and VR6 form an adjustable voltage divider that will produce 0.000 to 0.150VDC. By connecting a separate 5V regulated supply to CONN2 pin 11 and CONN2 pin 12 (as shown on the SB100 board), and also shorting JB4 pin 3 and 5, and JB4 pin 4 and 6, this adjustable voltage is connected to the Coulomb Counter analog inputs of the ATmega406 device. By controlling the polarity of the external 5V supply, you can simulate either charging (CONN2 pin 11 = -5V), or discharging (CONN2 pin 11 = P.S.+5V). Note that CONN2 pin 12 is internally connected to GND.

2.6 SMBus interface

The SMBus circuitry includes zener diodes and current limiting resistors to prevent ESD from damaging the ATmega406. Increasing the resistance of R23 and R24 may result in non-compliance with the SMBus specification. For proper operation of the TWI Bus Connect/Disconnect Interrupt circuitry, pull-down resistors (2M-ohm) are included to force both SCL and SDA signals low when the pack is disconnected.

For Master Mode operation on SMBus, it is required to monitor the bus for activity before starting a transmission. PA6, as one possibility, can be configured to detect activity on the SMBCLK line through the Pin-Change capability of the ATmega406

device. This is jumpable directly on JB2 pins 3 and 4. Any other line that supports the Pin-Change functionality could also be used.

2.7 General Settings and Functionality

2.7.1 Factory default settings

As supplied from the factory, the ATAVRSB100 Development Kit is set up for simulation of both cell voltages and pack current. The jumpers come configured as shown in Table 2-7.

Table 2-7. Jumper settings on the SB100.

Jumper	Description
J1	Jumper present but not installed; used to provide BATT signal from cell side to simulate the presence of a charger without requiring connectivity to a Host system.
JB1	All five jumpers are installed to provide LED connectivity.
JB2	• Short pin 3 and 4 to connect PA6 to SMBCLK, which is required for Master-mode SMBus operation. • Short pin 5 and 6 to connect PA7 to Switch SW1, which is used for activating LED function via button. • Short pin 7 and 8 to connect PB6 to LEDs (LED1:5), to adjust LED power and intensity via OC0A PWM function.
JB3	All five jumpers are installed (short pin 1 to pin 2, pin 3 to pin 4 and so on) to enable cell voltage simulation.
JB4	Default connection to use simulator shunt for current measurement: • Short pin 3 and 5 to connect SENSEHI line to Pack Current Simulation (adjustable shunt resistance) VR6. • Short pin 4 and 6 to connect SENSELOW to GND (on connector CONN2). To use the R7 shunt resistor, typically when using actual battery: • Short pin 1 and 3 to connect SENSEHI line to high side of R7 • Short pin 2 and 4 to connect SENSELO line to low side of R7
HDR1	Short pin 1 and 2 to connect PA0, which is ADC input, to all thermistors.

2.7.2 Switches and LEDs

The SB100 board includes five LEDs that can be used for any purpose, but are typically used as charge indicators. Additionally a pushbutton (SW1) is available for activating this display function. JB1 provides the ability to isolate the I/O signals that have been designated as LED control lines, if desired. When jumped, individual LEDs are controlled by driving the associated I/O signal low. The JB1 pins are described in Table 2-8 below.

The source voltage for the LEDs can come either from the 3.3V supply, or from PB6. PB6 may be configured to act either as a standard I/O signal, enabling the LEDs when driven high, or may optionally present the OC0A PWM output. Thus, OC0A may be used to provide brightness control for the LEDs automatically in hardware. Note that the PWM will power the LEDs during the high portion of the output signal.

It is highly recommended that the LEDs be lit one at a time, rather than enabled all together, in order to reduce power supply current since the internal regulator of the ATmega406 is limited. This solution is implemented in the OC0A Compare Match

interrupt service routine. This approach also allows the use of a single current-limiting resistor, as only one LED is enabled at a time.

Table 2-8. JB1: LED enable jumper block

Pin	Name	Direction	Usage
1	LED1-K		
2	PB4	Output	LED1 enable, active-low
3	LED2-K		
4	PB5	Output	LED2 enable, active-low
5	LED3-K		
6	PB7	Output	LED3 enable, active-low
7	LED4-K		
8	PD0	Output	LED4 enable, active-low
9	LED5-K		
10	PD1	Output	LED5 enable, active-low

JB2 provides access to several I/O signals as well as extra signals used in the software implementation provided by Atmel (specifically the SMBCLK signal and the SPARE pushbutton). Additionally, power for the LEDs can be selected here to come either directly from 3.3V or from PB6 (OC0A PWM output).

Table 2-9. JB2: Miscellaneous signals jumper block

Pin	Name	Direction	Usage
1	GND		
2	PA5	I/O	Unused
3	SMBCLK	I/O	Tied to PA6 for SMBus idle detection
4	PA6	Input	Tied to SMBCLK for SMBus idle detection
5	SW1	Output	Spare switch to activate Capacity Indicator LEDs
6	PA7	Input	SW1 pushbutton input
7	LED_PWR		Common positive feed to all LEDs
8	PB6	Output	PWM to LEDs
9	LED_PWR		Common positive feed to all LEDs
10	+3.3V		Steady supply to LEDs

2.7.3 External Thermistors

Using HDR1 (described in Table 2-10 below), SB100 provides control and measurement for up to four external thermistors. PA0-3 are inputs to the VADC with a range of 0 – 1.100V, while PA4 has a range of 0 – 5.500V. Thus, for best accuracy and lowest power, one of the inputs PA0-3 should be used to read external thermistors. Using the Vref output of 1.100V to power the thermistor circuitry ensures that the maximum ADC range is available without concern for circuit tolerances, as would be the case if 3.3V were used.

In practice, PA0 is shorted to the common bus - the odd-numbered pins of HDR1 - while PA1-4 connect to individual thermistors. The other side of all thermistors ties to the bus. The PAx VADC inputs have a relatively low input impedance of about 100K.

Thus, it is better to use lower resistance thermistors to reduce errors. Figure 2-7 shows how to connect external thermistors to HDR1.

Since the input impedance of the VADC will affect the reading, PA0 is used both for normal readings and to provide a ‘calibration’ reading. Specifically, PA0 is selected as a VADC input and a conversion is performed, while PA1-4 are configured as digital inputs without pull-up resistors enabled. Since the PA0 pin provides an impedance to GND, the voltage on the PA0 pin, and the thermistor common bus, will not be 1.100V, but will reflect the voltage divider that is created by R25 and the VADC input impedance. The conversion result can be used to calculate the exact input impedance of the VADC, since R25 is a known fixed resistance. Any thermal influence or device-to-device variance of the input impedance can also be determined.

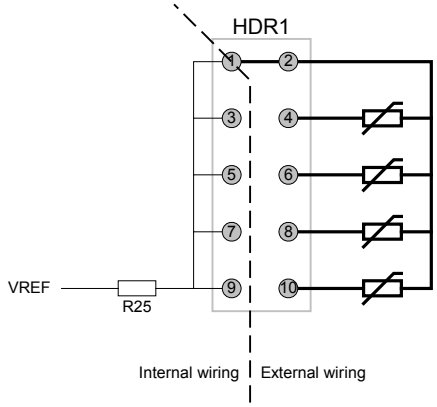
To read any of the four thermistors, its I/O line is driven low, thus forming a voltage divider between R25 and the selected thermistor. A VADC conversion may optionally be performed on that I/O signal to determine any offset above GND that may exist. A conversion is also performed on PA0, thus reading the bus voltage. Since R25 is a known value, the thermistor’s resistance may now be calculated, remembering that the input impedance of the VADC itself is in parallel with the thermistor.

It is possible to have more than four external thermistors, since each thermistor simply requires being driven low when enabled and being high impedance when not enabled.

Table 2-10. HDR1: Thermistor connections

Pin	Name	Direction	Usage
1	ThermBUS		
2	PA0	Input	Thermistor VADC input
3	ThermBUS		
4	PA1		Thermistor #1 control signal
5	ThermBUS		
6	PA2		Thermistor #2 control signal
7	ThermBUS		
8	PA3		Thermistor #3 control signal
9	ThermBUS		
10	PA4		Thermistor #4 control signal

Figure 2-7. External thermistor connection



3 Appendix – Additional hardware documentation

Figure 3-1. Schematic

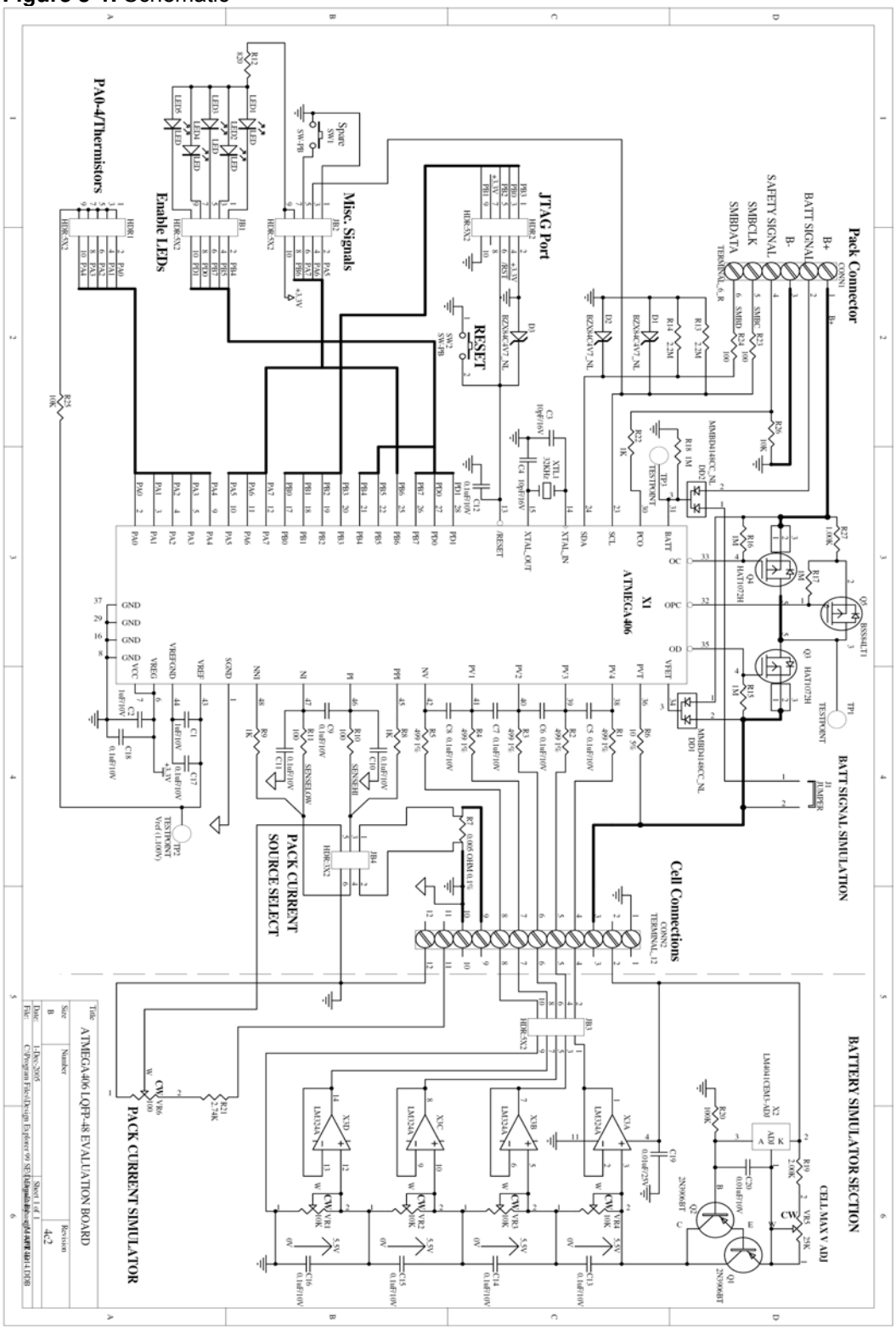


Figure 3-2. Assembly drawing

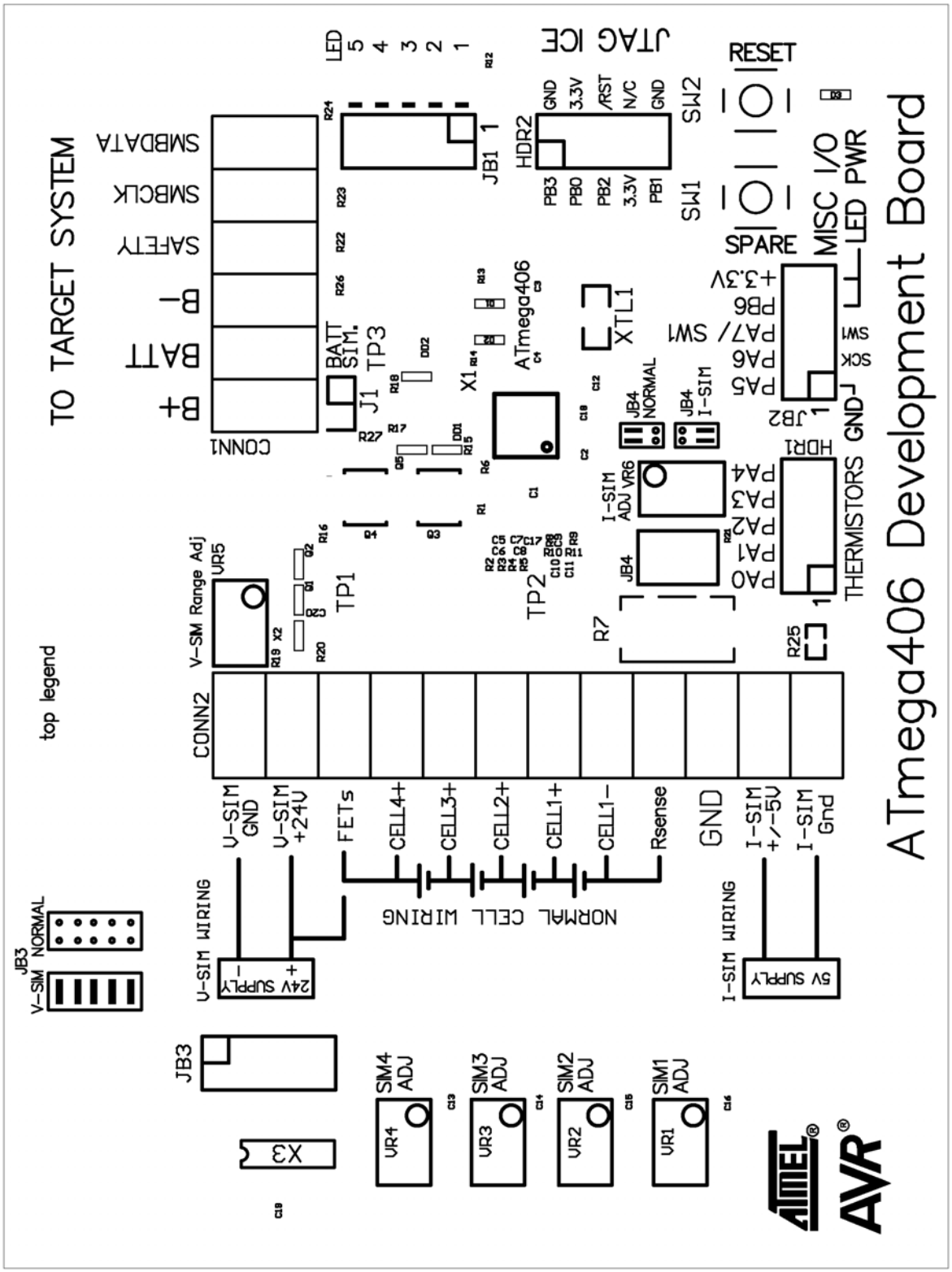


Table 3-1. Bill of Materials

Qty	Part Type	Designator	Description	Footprint
2	1uF/10V	C1,C2	+80%/-20% CERAMIC CAPACITOR X7R	0603
2	10pF/10V	C3,C4	+/-5% CERAMIC CAPACITOR C0G	0402
14	0.1uF/10V	C5-C18	+/-10% X5R CERAMIC	0402
2	0.01uF/25V	C19,C20	X7R CERAMIC	0402
5	499 1%	R1-R5		0402
1	10 5%	R6		0402
1	RW1S0CKR005DT	R7	5mΩ 0.5% 4-terminal current sense resistor	non-std
2	1K 1%	R8,R9		0402
2	100 1%	R10,R11		0402
1	820 5%	R12		0402
2	2.2M 5%	R13,R14		0402
4	1M 5%	R15-R18		0402
1	2.0K 1%	R19		0402
1	100K 5%	R20		0402
1	2.74K 1%	R21		0402
1	1K 1%	R22		0402
2	100 5% or 1%	R23,R24		0603
1	10K 1%	R25		0603
1	10K 5%	R26		0402
1	1K 1%	R27		1206
4	3266W-1-103_LF	VR1-VR4	Top-adjust 1/4" Cermet pot, sealed, 3266W series, 10K	through-hole
1	3266W-1-253_LF	VR5	Top-adjust 1/4" Cermet pot, sealed,3266W series, 25K	through-hole
1	3266W-1-101_LF	VR6	Top-adjust 1/4" Cermet pot, sealed,3266W series, 100	through-hole
3	BZX84C4V7_NL	D1-D3	4.7V ZENER DIODE	SOT-23A
2	MMBD4148CC_NL	DD1,DD2	DUAL DIODE, COMMON CATHODE	SOT-23A
5	SML-LX0603SRW-TR	LED1-LED5	RED, HIGH EFFICIENCY	0603
2	MMBT3906	Q1,Q2	PNP SMALL SIGNAL TRANSISTOR	SOT-23A
2	HAT1072H	Q3,Q4	P-CHANNEL POWER MOSFET	LFPAK
1	BSS84LT1G	Q5	P-CHANNEL MOSFET	SOT-23A
1	ATMEGA406-1AAU	X1	ATMEGA406 Rev E	LQFP-48
1	LM4041CEM3-ADJ	X2	ADJUSTABLE 1.24V SHUNT REG	SOT-23A
1	LM324AM	X3	QUAD OP-AMP 32V SMD	14-SOP
1	Q13FC1450000614	XTL1	XTAL, 32KHz, SMD, FC145 pkg	
5	HDR:5X2	HDR1,HDR2, JB1-JB3	DUAL-ROW 5x2 HEADER, 0.1" CENTER	HDR:5X2
1	HDR:3X2	JB4	DUAL-ROW 3x2 HEADER, 0.1" CENTER	HDR:3X2
1	HDR:2x1	J1	2-PIN 0.100" HEADER	HDR:2x1
16	SHORTING JUMPER		0.100" SHORTING JUMPER	n/a
1	SW-PB	SW1	PUSHBUTTON, SMT, BROWN OR BLACK	PB6MM
1	SW-PB	SW2	PUSHBUTTON, SMT, RED,	PB6MM
3	999332UL	CONN1,CONN2, CONN3	LM 5.00/6/90 5.0MM SCREW TERMINAL, 90' STACKABLE	through-hole
1	A0402.3.4000D	PCB	PCB-ATAVRSB100-D	n/a
0	alt. Src to R7 above	R7	Alternate Source: # CSR1TTER005D	same as R7

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