Features

- **Single 3.3V ± 10% Supply**
- **Fast Read Access Time – 200 ns**
- **Automatic Page Write Operation**
  - **Internal Address and Data Latches for 128 Bytes**
  - **Internal Control Timer**
- **Fast Write Cycle Time**
  - **Page Write Cycle Time – 10 ms Maximum**
  - **1 to 128-Byte Page Write Operation**
- **Low Power Dissipation**
  - **15 mA Active Current**
  - **20 µA CMOS Standby Current**
- **Hardware and Software Data Protection**
- **$\overline{\text{DATA}}$ Polling for End of Write Detection**
- **High Reliability CMOS Technology**
  - **Endurance: 100,000K Cycles**
  - **Data Retention: 10 Years**
- **JEDEC Approved Byte-Wide Pinout**
- **Commercial, Industrial and Automotive Temperature Ranges**
- **Green (Pb/Halide-free) Packaging Option**

1-Megabit (128K x 8) Low Voltage Paged Parallel EEPROMs

AT28LV010

1. Description

The AT28LV010 is a high-performance 3-volt only Electrically Erasable and Programmable Read-Only Memory. Its 1 megabit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation of just 54 mW. When the device is deselected, the CMOS standby current is less than 20 µA.

The AT28LV010 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128 bytes simultaneously. During a write cycle, the address and 1 to 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

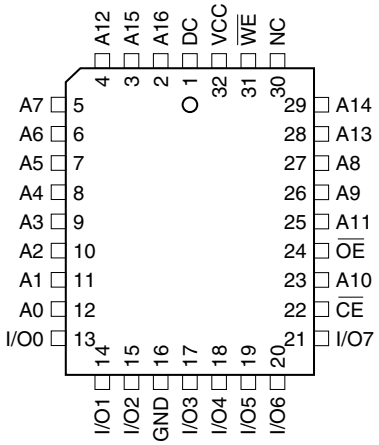
Atmel's 28LV010 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. Software data protection is implemented to guard against inadvertent writes. The device also includes an extra 128 bytes of EEPROM for device identification or tracking.

0395C–PEEPR–04/05

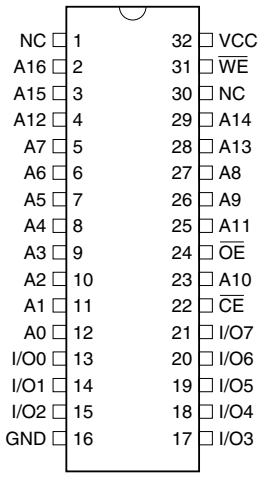
2. Pin Configurations

Pin Name	Function
A0 - A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

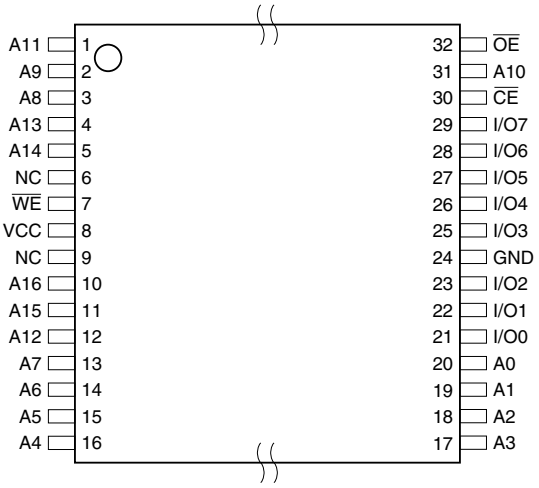
2.1 32-lead PLCC Top View



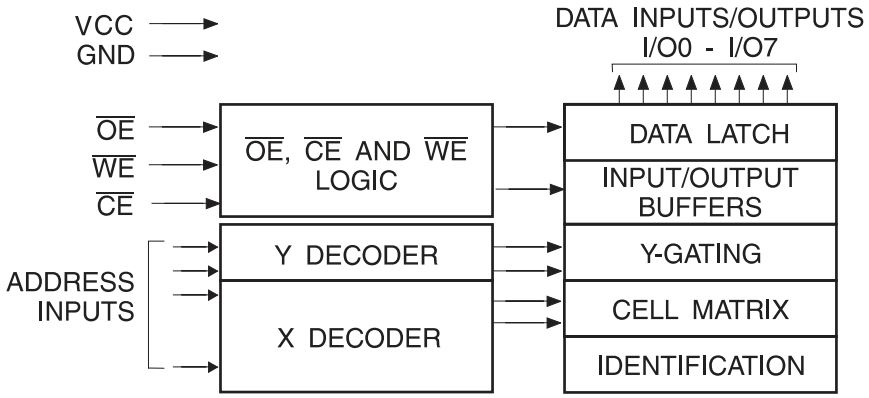
2.2 32-lead PDIP Top View



2.3 32-lead TSOP Top View



3. Block Diagram



4. Device Operation

4.1 Read

The AT28LV010 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

4.2 Write

The write operation of the AT28LV010 allows 1 to 128 bytes of data to be written into the device during a single internal programming period. Each write operation must be preceded by the software data protection (SDP) command sequence. This sequence is a series of three unique write command operations that enable the internal write circuitry. The command sequence and the data to be written must conform to the software protected write cycle timing. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last and data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28LV010 will cease accepting data and commence the internal programming operation. If more than one data byte is to be written during a single programming operation, they must reside on the same page as defined by the state of the A7 - A16 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A7 - A16 must be the same.

The A0 to A6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

4.3 $\overline{\text{DATA}}$ Polling

The AT28LV010 features $\overline{\text{DATA}}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{\text{DATA}}$ Polling may begin at anytime during the write cycle.

4.4 Toggle Bit

In addition to $\overline{\text{DATA}}$ Polling the AT28LV010 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

4.5 Data Protection

If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

4.5.1 Hardware Protection

Hardware features protect against inadvertent writes to the AT28LV010 in the following ways: (a) V_{CC} power-on delay – once V_{CC} has reached 2.0V (typical) the device will automatically time out 5 ms (typical) before allowing a write; (b) write inhibit – holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits write cycles; and (c) noise filter – pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a write cycle.

4.5.2 Software Data Protection

The AT28LV010 incorporates the industry standard software data protection (SDP) function. Unlike standard 5-volt only EEPROM's, the AT28LV010 has SDP enabled at all times. Therefore, all write operations must be preceded by the SDP command sequence.

The data in the 3-byte command sequence is not written to the device; the addresses in the command sequence can be utilized just like any other location in the device. Any attempt to write to the device without the 3-byte sequence will start the internal timers. No data will be written to the device. However, for the duration of t_{WC}, read operations will effectively be polling operations.

5. DC and AC Operating Range

		AT28LV010-20	AT28LV010-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
	Automotive	-40°C - 125°C	
V_{CC} Power Supply		3.3V ± 5%	3.3V ± 10%

6. Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.

7. Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

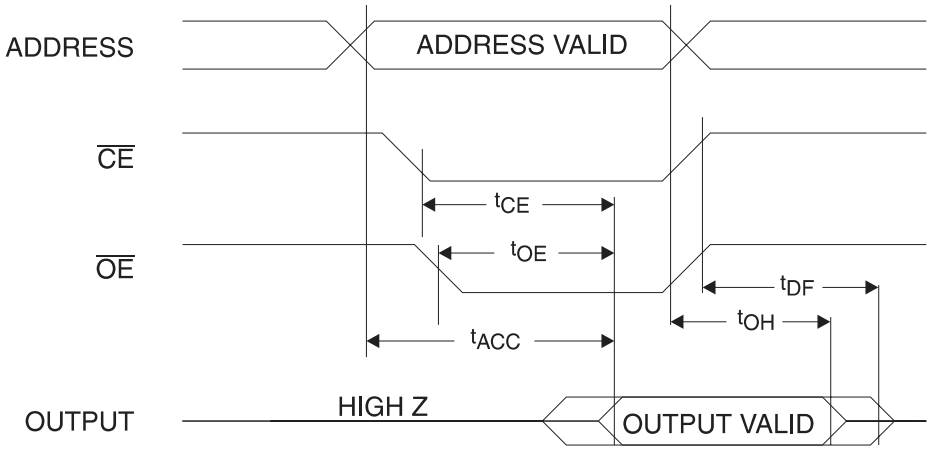
8. DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			1	µA
I_{SB}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V	Com.		20	µA
			Ind.		50	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V			15	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 3.0V			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 A; V_{CC} = 3.0V		2.4		V

9. AC Read Characteristics

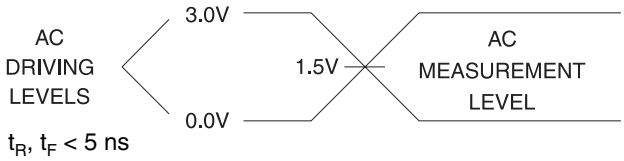
Symbol	Parameter	AT28LV010-20		AT28LV010-25		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		200		250	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		200		250	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	80	0	100	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, Whichever Occurred First	0		0		ns

10. AC Read Waveforms[1][2][3][4]

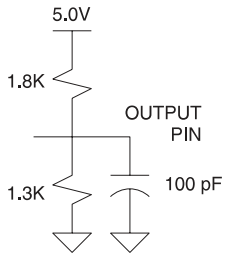


Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

11. Input Test Waveforms and Measurement Level



12. Output Test Load



13. Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

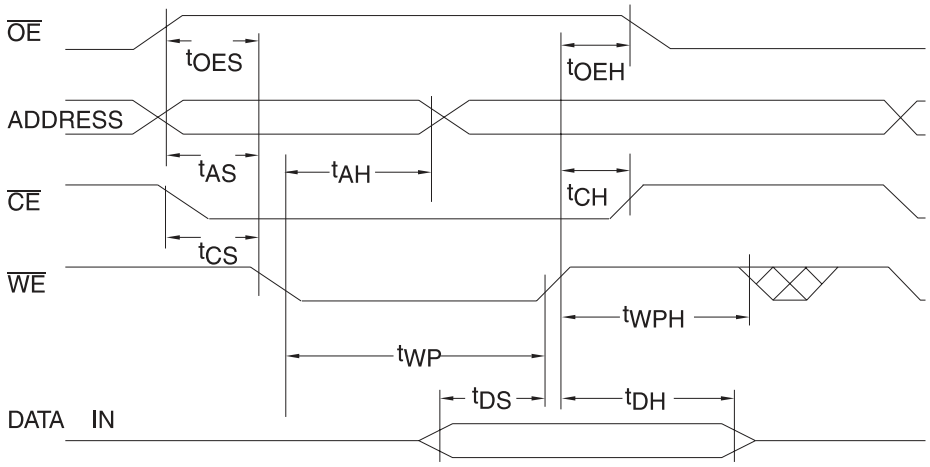
14. AC Write Characteristics[1]

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns

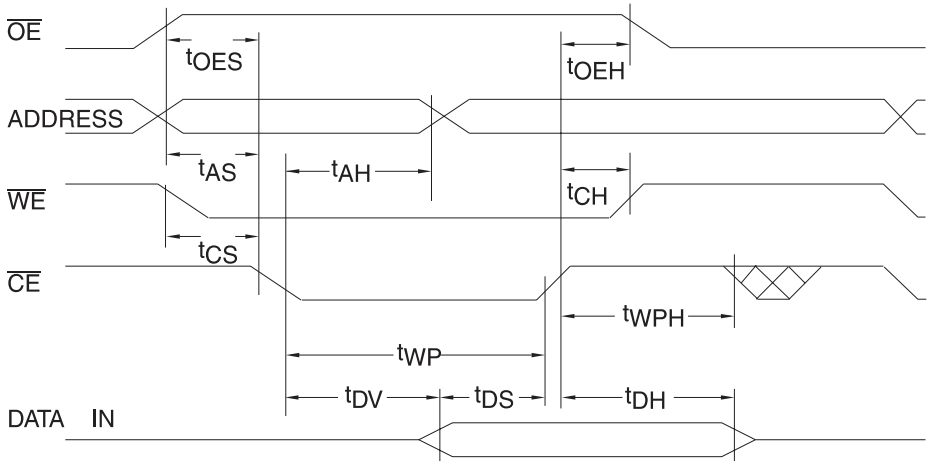
Note: 1. All write operations must be preceded by the SDP command sequence.

15. AC Write Waveforms

15.1 $\overline{WE}$ Controlled



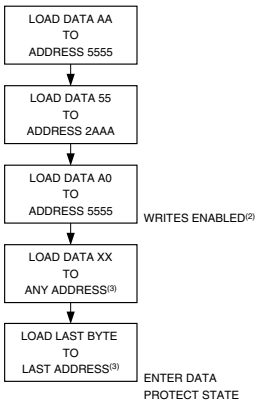
15.2 $\overline{CE}$ Controlled



16. Software Protected Write Characteristics

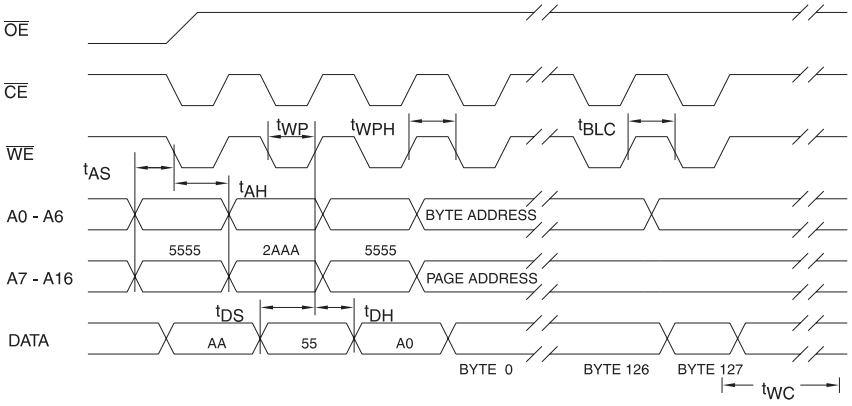
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	200		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

17. Programming Algorithm



Notes: 1. Data Format: I/O7 - I/O0 (Hex); Address Format: A14 - A0 (Hex).
2. Data protect state will be re-activated at the end of program cycle.
3. 1 to 128 bytes of data are loaded.

18. Software Protected Program Cycle Waveforms[(1)(2)(3)]



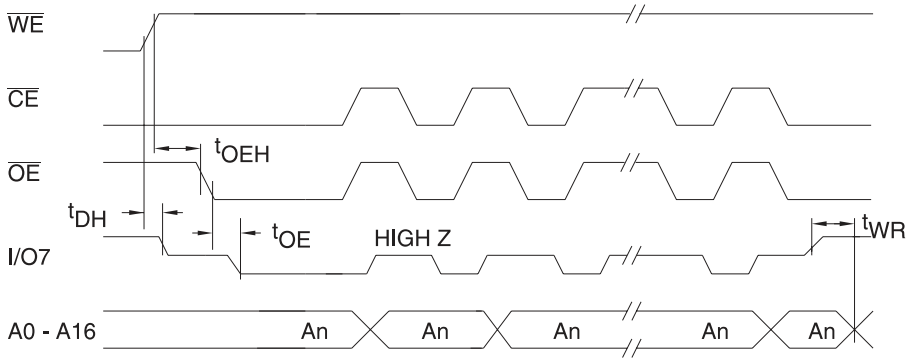
Notes: 1. A0 - A14 must conform to the addressing sequence for the first three bytes as shown above.
2. After the command sequence has been issued and a page write operation follows, the page address inputs (A7 - A16) must be the same for each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
3. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

19. $\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics

20. $\overline{\text{Data}}$ Polling Waveforms

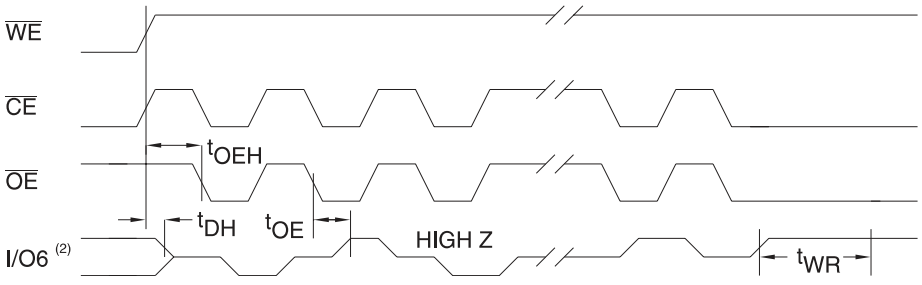


21. Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics

22. Toggle Bit Waveforms



Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

23. Ordering Information[1]

23.1 Standard Package

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	15	0.02	AT28LV010-20JC AT28LV010-20PC AT28LV010-20TC	32J 32P6 32T	Commercial (0° to 70°C)
	15	0.05	AT28LV010-20JI AT28LV010-20PI AT28LV010-20TI	32J 32P6 32T	Industrial (-40° to 85°C)
	15	0.05	AT28LV010-20TA	32T	Automotive (-40° to 125°C)
250	15	0.02	AT28LV010-25JC AT28LV010-25PC AT28LV010-25TC	32J 32P6 32T	Commercial (0° to 70°C)
	15	0.05	AT28LV010-25JI AT28LV010-25PI AT28LV010-25TI	32J 32P6 32T	Industrial (-40° to 85°C)

Note: 1. See “Valid Part Numbers” below.

23.2 Green Package Option (Pb/Halide-free)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	15	0.05	AT28LV010-20JU AT28LV010-20TU	32J 32T	Industrial (-40° to 85°C)

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
32P6	32-Lead, 0.600” Wide, Plastic Dual Inline Package (PDIP)
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)

24. Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

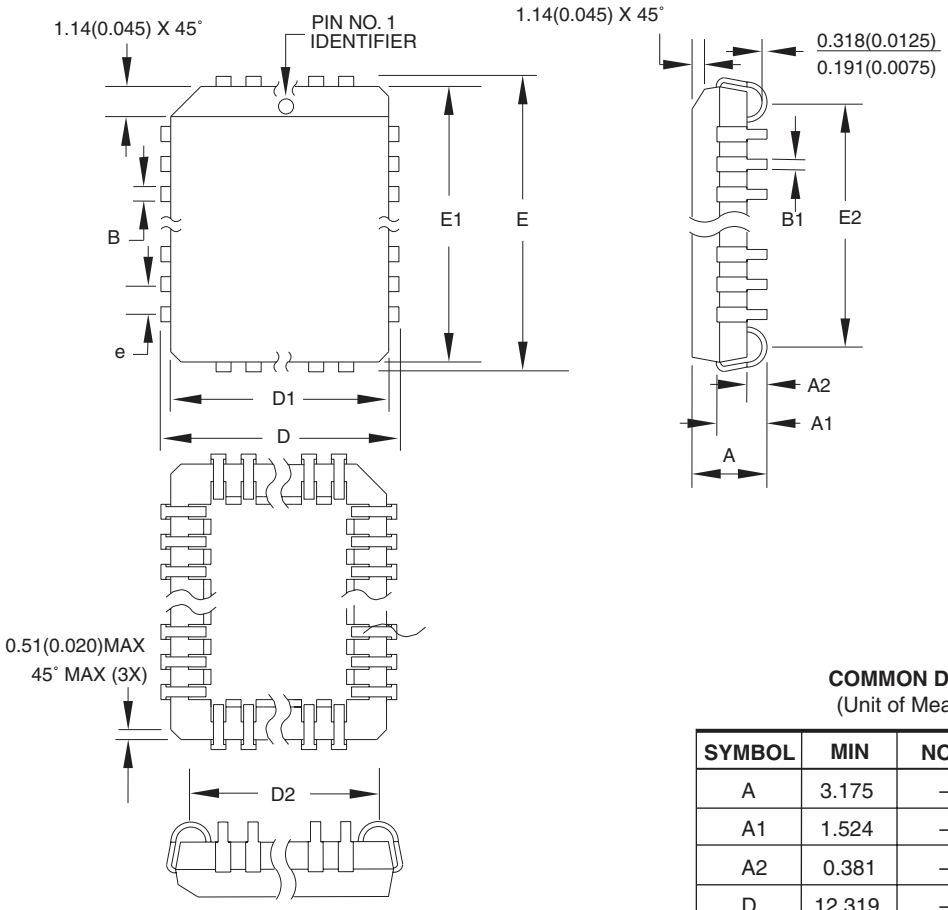
Device Numbers	Speed	Package and Temperature Combinations
AT28LV010	20	JC, JI, JU, PC, PI, TC, TI, TU
AT28LV010	25	JC, JI, PC, PI, TC, TI

25. Die Products

Reference Section: Parallel EEPROM Die Products

26. Packaging Information

26.1 32J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

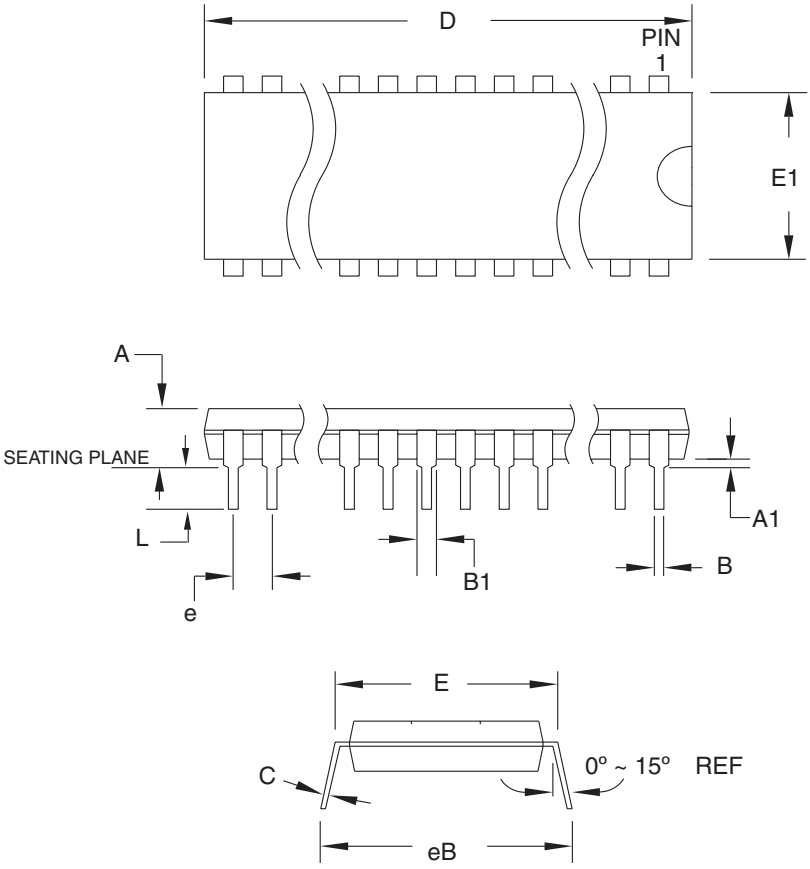
SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32J**, 32-lead, Plastic J-leaded Chip Carrier (PLCC)	32J	B

26.2 32P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

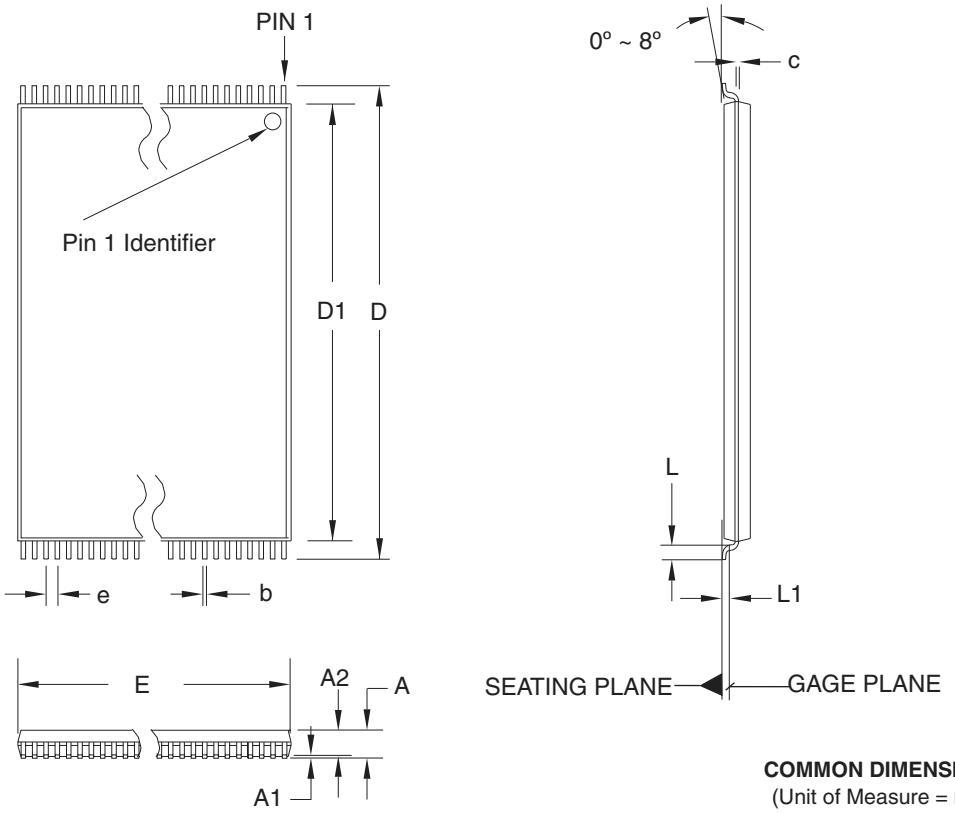
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	41.783	–	42.291	Note 1
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 1
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Note: 1. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32P6**, 32-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	32P6	B

26.3 32T – TSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	19.80	20.00	20.20	
D1	18.30	18.40	18.50	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.50 BASIC			

Notes:
1. This package conforms to JEDEC reference MO-142, Variation BD.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

10/18/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32T**, 32-lead (8 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP)	32T	B

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