Preferred Device

# **Power MOSFET 16 Amps, 400 Volts**

# N-Channel TO-247

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage-blocking capability without degrading performance over time. In addition, this advanced Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I<sub>DSS</sub> and V<sub>DS(on)</sub> Specified at Elevated Temperature
- Isolated Mounting Hole Reduces Mounting Hardware

### **MAXIMUM RATINGS** (T<sub>C</sub> = 25°C unless otherwise noted)

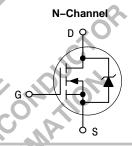
| Rating  | Symbol                              | Value           | Unit          |
|---|-------------------------------------|-----------------|---------------|
| Drain-Source Voltage  | V <sub>DSS</sub>                    | 400             | Vdc           |
| Drain–Gate Voltage ( $R_{GS} = 1.0 \text{ M}\Omega$ )   | $V_{DGR}$                           | 400             | Vdc           |
| Gate–Source Voltage  – Continuous  – Non–Repetitive (t <sub>p</sub> ≤ 10 ms)  | V <sub>GS</sub><br>V <sub>GSM</sub> | ± 20<br>± 40    | Vdc<br>Vpk    |
| $ \begin{array}{cccc} \text{Drain Current} & -\text{ Continuous} \\ & -\text{ Continuous } @ \ 100^{\circ}\text{C} \\ & -\text{ Single Pulse } (t_{p} \leq 10 \ \mu\text{s}) \\ \end{array} $     | I <sub>D</sub><br>I <sub>DM</sub>   | 16<br>9.0<br>56 | Adc<br>Apk    |
| Total Power Dissipation Derate above 25°C   | Pb                                  | 180<br>1.4      | Watts<br>W/°C |
| Operating and Storage Temperature Range   | T <sub>J</sub> , T <sub>stg</sub>   | -55 to<br>150   | °C            |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J = 25^{\circ}C$ ( $V_{DD} = 100 \text{ Vdc}, V_{GS} = 10 \text{ Vdc},$ $I_L = 16 \text{ Apk}, L = 6.8 \text{ mH}, R_G = 25 \Omega$ ) | E <sub>AS</sub>                     | 870             | mJ            |
| Thermal Resistance – Junction to Case – Junction to Ambient   | $R_{	heta JC} \ R_{	heta JA}$       | 0.70<br>40      | °C/W          |
| Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds  | TL                                  | 260             | °C            |



## ON Semiconductor

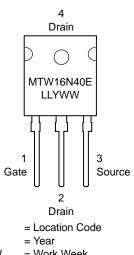
http://onsemi.com

# 16 AMPERES **400 VOLTS** $R_{DS(on)} = 240 \text{ m}\Omega$





MARKING DIAGRAM **& PIN ASSIGNMENT** 



WW = Work Week

LL

### ORDERING INFORMATION

| Device    | Package | Shipping      |
|-----------|---------|---------------|
| MTW16N40E | TO-247  | 30 Units/Rail |

Preferred devices are recommended choices for future use and best overall value.

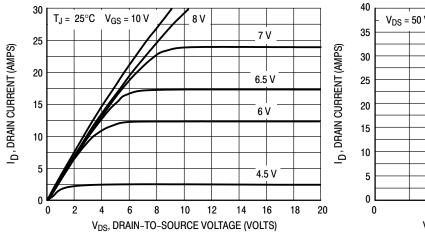
### **ELECTRICAL CHARACTERISTICS** (T<sub>.J</sub> = 25°C unless otherwise noted)

| Zero Gate Voltage Drain Current $(V_{DS} = 400  \text{Vdc}, V_{GS} = 0  \text{Vdc})$ $-$ 0.25 $-$ 1.0 mAdc $(V_{DS} = 400  \text{Vdc}, V_{GS} = 0  \text{Vdc})$ $-$ 1.0 mAdc $(V_{DS} = 320  \text{Vdc}, V_{GS} = 0  \text{Vdc}, V_{DS} = 0)$ $-$ 100 nAdc DN CHARACTERISTICS (Note 1.)  Gate Threshold Voltage $(V_{DS} = V_{GS}, I_D = 0.25  \text{mAdc})$ $-$ 2.0 3.0 4.0 mV/°C Temperature Coefficient (Negative) $-$ 7.0 - mV/°C Static Drain–Source On–Resistance $(V_{GS} = 10  \text{Vdc}, I_D = 8.0  \text{Adc})$ $-$ 0.225 0.24 Ohm Drain–Source On–Voltage $(V_{GS} = 10  \text{Vdc})$ $-$ 4.8 $(I_D = 16  \text{Adc})$ $-$ 4.8 $(I_D = 8.0  \text{Adc}, T_J = 125  \text{°C})$ $-$ 4.8 Terms of transconductance $(V_{DS} = 15  \text{Vdc}, I_D = 8.0  \text{Adc})$ $-$ mhos   | Cha   | Characteristic  |                      | Min      | Тур      | Max      | Unit         |
|--|---|---|----------------------|----------|----------|----------|--------------|
| (V <sub>OS</sub> = 0 Vdc, l <sub>0</sub> = 250 µAdc)         - 420         - 70         vdc           Zero Gate Voltage Drain Current (V <sub>OS</sub> = 400 Vdc, V <sub>OS</sub> = 0 Vdc)         ISSS         - 70         - 100         mAdc           (V <sub>OS</sub> = 320 Vdc, V <sub>OS</sub> = 0 Vdc, V <sub>OS</sub> = 0 Vdc, V <sub>OS</sub> = 0 Vdc, V <sub>OS</sub> = 20 Vdc, V <sub>OS</sub> = 0 Vdc, V <sub>OS</sub> = 10 Vdc, V <sub>OS</sub> = 10 Vdc, V <sub>OS</sub> = 0 Vdc, V <sub>OS</sub> = 0 Vdc, V <sub>OS</sub> = 10 Vdc, V <sub>OS</sub> = 0   | OFF CHARACTERISTICS   |   |                      |          |          |          |              |
| (V <sub>DS</sub> = 400 Vdc, V <sub>QS</sub> = 0 Vdc) (V <sub>DS</sub> = 25 Vdc, V <sub>DS</sub> = 0)   V <sub>QS</sub>   V <sub>QS</sub> | Drain-to-Source Breakdown Voltage<br>(V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) |   | V <sub>(BR)DSS</sub> | 400<br>- | -<br>420 | <u>-</u> | Vdc<br>mV/°C |
| Characteristics (Note 1.)   Sate Trieshold Voltage (Vos = Vos ), 10   2.0   3.0   4.0   M/C (Vos = Vos ), 10   2.0   3.0   4.0   M/C (Vos = Vos ), 10   2.0   3.0   4.0   M/C (Vos = Vos ), 10   2.0   M/C (Vos = Vos ), 10   2.0   M/C (Vos = Vos ), 10   M/C (Vos = Vos ), 10   M/C (Vos )   M  | $(V_{DS} = 400 \text{ Vdc}, V_{GS} = 0 \text{ Vdc})$                                      | Γ <sub>J</sub> = 125°C)                                 | I <sub>DSS</sub>     | -<br>-   | _<br>_   |          | mAdc         |
| Gate Threshold Voltage   | Gate-Body Leakage Current (V <sub>G</sub>   | $_{S} = \pm 20 \text{ Vdc}, V_{DS} = 0)$                | I <sub>GSS</sub>     | _        | _        | 100      | nAdc         |
| (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 0.25 mAdc)   Tompratruc Coefficient (Negative)   C - 7.0   - 7.0   mV/rC   | ON CHARACTERISTICS (Note 1.)  |   |                      |          |          |          |              |
| Drain-Source On-Voltage (V <sub>GS</sub> = 10 Vdc) (I <sub>D</sub> = 16 Adc) (I <sub>D</sub> = 16 Adc) (I <sub>D</sub> = 15 Vdc, I <sub>D</sub> = 8.0 Adc)   Sept.   | $(V_{DS} = V_{GS}, I_{D} = 0.25 \text{ mAdc})$  | ive)  | $V_{GS(th)}$         | 2.0      |          |          | Vdc<br>mV/°C |
| (I <sub>D</sub> = 16 Adc)<br>(I <sub>D</sub> = 8.0 Adc, T <sub>J</sub> = 125°C)         — — — — 4.8<br>4.3           Forward Transconductance (V <sub>DS</sub> = 15 Vdc, I <sub>D</sub> = 8.0 Adc)         g <sub>FS</sub> 8.0         10         — mhos           DVNAMIC CHARACTERISTICS           Input Capacitance         (V <sub>DS</sub> = 25 Vdc, V <sub>QS</sub> = 0 Vdc, G = 1.0 MHz)         C <sub>iss</sub> — 2570         3600         pF           Output Capacitance         (V <sub>DS</sub> = 25 Vdc, V <sub>QS</sub> = 0 Vdc, G = 1.0 MHz)         C <sub>iss</sub> — 82         164           SWITCHING CHARACTERISTICS (Note 2.)           Turn-On Delay Time         (V <sub>DD</sub> = 200 Vdc, I <sub>D</sub> = 16 Adc, V <sub>QS</sub> = 10 Vdc, R <sub>G</sub> = 9.1 Ω)         t <sub>d</sub> (on)         — 29         50         ns           Rise Time         (V <sub>DD</sub> = 200 Vdc, I <sub>D</sub> = 16 Adc, V <sub>QS</sub> = 10 Vdc, R <sub>G</sub> = 9.1 Ω)         t <sub>d</sub> (off)         — 76         170           Gate Charge         (V <sub>DS</sub> = 320 Vdc, I <sub>D</sub> = 16 Adc, V <sub>QS</sub> = 0 Vdc)         Q <sub>T</sub> — 66         93         nc           (Soe Figure 8)         (I <sub>S</sub> = 16 Adc, V <sub>QS</sub> = 0 Vdc)         V <sub>SD</sub> — 10         1.6         — 0.9         — 0.9         — 0.9         — 0.9         — 0.9         — 0.9         — 0.9         — 0.9         — 0.9         — 0.9         — 0.9         — 0.9         — 0.9         — 0.9 <td>Static Drain-Source On-Resistar</td> <td>ce (V<sub>GS</sub> = 10 Vdc, I<sub>D</sub> = 8.0 Adc)</td> <td>R<sub>DS(on)</sub></td> <td>_</td> <td>0.225</td> <td>0.24</td> <td>Ohm</td>  | Static Drain-Source On-Resistar   | ce (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 8.0 Adc) | R <sub>DS(on)</sub>  | _        | 0.225    | 0.24     | Ohm          |
| DynAMic Characteristics   Input Capacitance   (VDS = 25 Vdc, VGS = 0 Vdc, f = 1.0 MHz)   Coss   C  | $(I_D = 16 \text{ Adc})$  |   | V <sub>DS(on)</sub>  |          | -<br>-   |          | Vdc          |
| Input Capacitance  | Forward Transconductance (V <sub>DS</sub>   | = 15 Vdc, I <sub>D</sub> = 8.0 Adc)                     | 9FS                  | 8.0      | 8.0 10 - |          | mhos         |
| Output Capacitance   (V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)   C <sub>Oss</sub>   - 330   460   | DYNAMIC CHARACTERISTICS   |   |                      |          |          |          | •            |
| Reverse Transfer Capacitance   f = 1.0 MHz    Coss   -   82   164  | Input Capacitance   |   | C <sub>iss</sub>     | _        | 2570     | 3600     | pF           |
| Reverse Transfer Capacitance   Crss   - 82   164   | Output Capacitance  |   | C <sub>oss</sub>     | _        | 330      | 460      |              |
| $ \frac{\text{Turn-On Delay Time}}{\text{Rise Time}} = \frac{\text{(V}_{DD} = 200  Vdc,  I_{D} = 16  Adc,  V_{GS} = 10  Vdc,  R_{G} = 9.1  \Omega)}{\text{Turn-Off Delay Time}} = \frac{\text{(V}_{DD} = 200  Vdc,  I_{D} = 16  Adc,  V_{GS} = 10  Vdc,  R_{G} = 9.1  \Omega)}{\text{tr}} = \frac{\text{td}(\text{off})}{\text{tr}} = \frac{1}{1000  \text{Tr}} = 1$   | Reverse Transfer Capacitance  | 1 = 1.5 (vii 12)  | C <sub>rss</sub>     | _        | 82       | 164      |              |
| $ \frac{\text{Rise Time}}{\text{Turn-Off Delay Time}} = \frac{(V_{DD} = 200  \text{Vdc},  I_D = 16  \text{Adc},  V_{GS} = 10  \text{Vdc},  R_G = 9.1  \Omega)}{\text{V}_{GS} = 10  \text{Vdc}},  \frac{t_f}{t_g} = \frac{-}{.057} = \frac{62}{.057} = \frac{70}{.057} = \frac{170}{.057} =$   | SWITCHING CHARACTERISTICS   | (Note 2.)   |                      |          |          |          |              |
| $ \frac{\text{Turn-Off Delay Time}}{\text{Fall Time}} = \frac{\text{V}_{\text{GS}} = 10  \text{Vdc},}{\text{R}_{\text{G}} = 9.1  \Omega} + \frac{1}{\text{td}_{\text{(off)}}} + \frac{7}{\text{c}} + \frac{7}{\text{c}} + \frac{170}{\text{c}} + 17$  | Turn-On Delay Time  |   | t <sub>d(on)</sub>   | _        | 29       | 50       | ns           |
| $ \begin{array}{ c c c c c c } \hline \text{Turn-Off Delay Time} & R_G = 9.1  \Omega) & t_{d(off)} & - & 76 & 170 \\ \hline \text{Fall Time} & t_f & - & 57 & 95 \\ \hline \\ \text{Gate Charge} \\ \text{(See Figure 8)} & Q_T & - & 66 & 93 & nC \\ \hline \\ \text{(VDS} = 320  \text{Vdc},  l_D = 16  \text{Adc},  \\ \hline \\ \text{V}_{GS} = 10  \text{Vdc}) & Q_1 & - & 17 & - \\ \hline \\ Q_2 & - & 31 & - & \\ \hline \\ Q_3 & - & 30 & - & \\ \hline \\ \text{SOURCE-DRAIN DIODE CHARACTERISTICS} \\ \hline \\ \text{Forward On-Voltage (Note 1.)} & (l_S = 16  \text{Adc},  \text{V}_{GS} = 0  \text{Vdc}) & V_{SD} & - & 1.0 & 1.6 & \\ \hline \\ \text{(I}_S = 16  \text{Adc},  \text{V}_{GS} = 0  \text{Vdc},  T_J = 125^{\circ}\text{C}) & - & 340 & - & ns \\ \hline \\ \text{Reverse Recovery Time} & t_{fr} & - & 340 & - & ns \\ \hline \\ \text{(See Figure 9)} & t_{l_S} & - & 228 & - & \\ \hline \\ \text{Reverse Recovery Stored} & t_{l_S} & - & 112 & - & \\ \hline \\ \text{Charge} & & - & 4.3 & - & \mu C \\ \hline \\ \text{Internal Drain Inductance} & L_D & - & 5.0 & - & nH \\ \hline \\ \text{Internal Source Inductance} & L_S & - & 13 & - & nH \\ \hline \\ \hline \end{array} $   | Rise Time   |   | t <sub>r</sub>       | _        | 62       | 70       |              |
|  | Turn-Off Delay Time   |   | t <sub>d(off)</sub>  | _        | 76       | 170      |              |
| $(See \ Figure \ 8) \\ (V_{DS} = 320 \ Vdc, \ I_{D} = 16 \ Adc, \ V_{GS} = 10 \ Vdc) \\ \hline (V_{DS} = 320 \ Vdc, \ I_{D} = 16 \ Adc, \ V_{GS} = 10 \ Vdc) \\ \hline (Q_{2} \qquad - \qquad 31 \qquad - \qquad 30 \qquad -$   | Fall Time   |   | t <sub>f</sub>       | _        | 57       | 95       |              |
| $V_{GS} = 10 \text{ Vdc}) \\ \hline Q_2 & - & 31 & - \\ \hline Q_3 & - & 30 & - \\ \hline \\ \textbf{SOURCE-DRAIN DIODE CHARACTERISTICS} \\ \hline Forward On-Voltage (Note 1.) \\ \hline (I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc}) \\ (I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } T_J = 125^{\circ}\text{C}) \\ \hline \\ Reverse Recovery Time \\ (See Figure 9) \\ \hline \\ Reverse Recovery Stored \\ Charge \\ \hline \\ \textbf{NTERNAL PACKAGE INDUCTANCE} \\ \hline Internal Drain Inductance \\ (Measured from the drain lead 0.25" from package to center of die) \\ \hline \\ \textbf{NTERNAL Source Inductance} \\ \hline \\ \textbf{L}_S & - & 13 & - & \text{nH} \\ \hline \\ \textbf{NTERNAL Package Inductance} \\ \hline \\ \textbf{L}_S & - & 13 & - & \text{nH} \\ \hline \\ \textbf{NTERNAL Package Inductance} \\ \hline \\ \textbf{L}_S & - & 13 & - & \text{nH} \\ \hline \\ \textbf{NTERNAL Package Inductance} \\ \hline \\ \textbf{L}_S & - & 13 & - & \text{nH} \\ \hline \\ \textbf{NTERNAL Package Inductance} \\ \hline \\ \textbf{L}_S & - & 13 & - & \text{nH} \\ \hline \\ \textbf{NTERNAL Package Inductance} \\ \hline \\ \textbf{L}_S & - & 13 & - & \text{nH} \\ \hline \\ \textbf{NTERNAL Package Inductance} \\ \hline \\ \textbf{L}_S & - & 13 & - & \text{nH} \\ \hline \\ \textbf{NTERNAL Package Inductance} \\ \hline \\ \textbf{L}_S & - & 13 & - & \text{nH} \\ \hline \\ \textbf{NTERNAL Package Inductance} \\ \hline \\ \textbf{L}_S & - & 13 & - & \text{nH} \\ \hline \\ \textbf{NTERNAL Package Inductance} \\ \hline \\ \textbf{L}_S & - & 13 & - & \text{nH} \\ \hline \\ \textbf{NTERNAL Package Inductance} \\ \hline \\ \textbf{L}_S & - & 13 & - & \text{nH} \\ \hline \\ \textbf{NTERNAL Package Inductance} \\ \hline \\ \textbf{L}_S & - & 13 & - & \text{nH} \\ \hline \\ \textbf{NTERNAL Package Inductance} \\ \hline \\ \textbf{L}_S & - & 13 & - & \text{nH} \\ \hline \\ \textbf{NTERNAL Package Inductance} \\ \hline \\ \textbf{L}_S & - & 13 & - & \text{nH} \\ \hline \\ \textbf{NTERNAL Package Inductance} \\ \hline \\ \textbf{L}_S & - & 13 & - & \text{nH} \\ \hline \\ \textbf{NTERNAL Package Inductance} \\ \hline \\ \textbf{L}_S & - & 13 & - & \text{nH} \\ \hline \\ \textbf{NTERNAL Package Inductance} \\ \hline \\ \textbf{L}_S & - & 13 & - & \text{nH} \\ \hline \\ \textbf{NTERNAL Package Inductance} \\ \hline \\ \textbf{L}_S & - & 13 & - & \text{nH} \\ \hline \\ \textbf{NTERNAL Package Inductance} \\ \hline \\ \textbf{L}_S & - & 13 & - & \text{nH} \\ \hline \\ \textbf{NTERNAL Package Inductance} \\ \hline \\ \textbf{L}_S & - & 13 & - & \text{nH} \\ \hline \\ \textbf{NTERNAL Package Inductance} \\ \hline \\ \textbf{L}_S & - & 13 & - & \text{nH} \\ \hline \\ \textbf{NTERNAL Package Inductance} \\ \hline \\ \textbf{L}_S & - & 13 & - & \text{nH} \\ \hline \\ \textbf{NTERNAL Package Inductance} \\ \hline $  |   |   | Q <sub>T</sub>       | -        | 66       | 93       | nC           |
|  |   |   | Q <sub>1</sub>       | _        | 17       | -        |              |
| Forward On–Voltage (Note 1.) $ \begin{pmatrix} (I_S = 16 \text{ Adc, V}_{GS} = 0 \text{ Vdc}) \\ (I_S = 16 \text{ Adc, V}_{GS} = 0 \text{ Vdc, T}_J = 125^{\circ}\text{C}) \end{pmatrix} \qquad \begin{pmatrix} V_{SD} \\ - \\ 0.9 \end{pmatrix} \qquad \begin{pmatrix} 1.0 \\ 0.9 \end{pmatrix} \qquad \begin{pmatrix} 1.6 \\ - \\ - \\ 0.9 \end{pmatrix} \qquad \begin{pmatrix} 1.6 \\ - \\ - \\ - \\ - \end{pmatrix} \qquad \begin{pmatrix} 1.6 \\ - \\ - \\ - \\ - \end{pmatrix} \qquad \begin{pmatrix} 1.6 \\ - \\ - \\ - \\ - \end{pmatrix} \qquad \begin{pmatrix} 1.6 \\ - \\ - \\ - \\ - \\ - \end{pmatrix} \qquad \begin{pmatrix} 1.6 \\ - \\ - \\ - \\ - \end{pmatrix} \qquad \begin{pmatrix} 1.6 \\ - \\ - \\ - \\ - \\ - \end{pmatrix} \qquad \begin{pmatrix} 1.6 \\ - \\ - \\ - \\ - \\ - \end{pmatrix} \qquad \begin{pmatrix} 1.6 \\ - \\ - \\ - \\ - \\ - \\ - \end{pmatrix} \qquad \begin{pmatrix} 1.6 \\ - \\ - \\ - \\ - \\ - \\ - \\ - \\ - \end{pmatrix} \qquad \begin{pmatrix} 1.6 \\ - \\ - \\ - \\ - \\ - \\ - \\ - \\ - \\ - \\ $   |   | V <sub>GS</sub> = 10 V <sub>dC</sub> )                  | Q <sub>2</sub>       | -        | 31       | -        |              |
| Forward On–Voltage (Note 1.) $ \begin{pmatrix} (I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc}) \\ (I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } T_J = 125^{\circ}\text{C}) \end{pmatrix} \qquad \begin{array}{c} - & 1.0 & 1.6 \\ - & 0.9 & - \end{array} \end{pmatrix} $ Reverse Recovery Time (See Figure 9) $ \begin{pmatrix} (I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & 100 \text{ A}/\mu\text{S} \end{pmatrix} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & 100 \text{ A}/\mu\text{S} \end{pmatrix} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & 112 & - \end{cases} $ Reverse Recovery Stored Charge $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 100 \text{ A}/\mu\text{S} \end{pmatrix} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 112 & - \end{cases} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 112 & - \end{cases} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 112 & - \end{cases} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 112 & - \end{cases} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 112 & - \end{cases} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 112 & - \end{cases} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 112 & - \end{cases} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 112 & - \end{cases} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 112 & - \end{cases} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 112 & - \end{cases} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 112 & - \end{cases} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 112 & - \end{cases} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 112 & - \end{cases} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 112 & - \end{cases} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 12 & - \end{cases} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 12 & - \end{cases} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 12 & - \end{cases} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 12 & - \end{cases} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 12 & - \end{cases} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 12 & - \end{cases} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 12 & - \end{cases} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = 0 \text{ Vdc, } \\ - & I_S = 12 & - \end{cases} $ $ \begin{pmatrix} I_S = 16 \text{ Adc, } V_{GS} = $  |   |   | Q <sub>3</sub>       | -        | 30       | _        |              |
|  | SOURCE-DRAIN DIODE CHARAG   | CTERISTICS  |                      |          |          |          |              |
| $ (I_S = 16 \text{ Adc, V}_{GS} = 0 \text{ Vdc, } \\ dI_S/dt = 100 \text{ A/}\mu\text{s}) $ $ t_a                                  $   | Forward On-Voltage (Note 1.)  |   | V <sub>SD</sub>      | _<br>_   |          | 1.6<br>- | Vdc          |
|  |   |   | t <sub>rr</sub>      | _        | 340      | -        | ns           |
| Reverse Recovery Stored Charge   |   |   | t <sub>a</sub>       | _        | 228      | _        | -            |
| Reverse Recovery Stored Charge $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$  |   |   | t <sub>b</sub>       | _        | 112      | _        | 1            |
| Internal Drain Inductance (Measured from the drain lead 0.25" from package to center of die)  Internal Source Inductance   |   | everse Recovery Stored                                  |                      | -        | 4.3      | -        | μС           |
| (Measured from the drain lead 0.25" from package to center of die)  Internal Source Inductance  L <sub>S</sub> - 13 - nH   | NTERNAL PACKAGE INDUCTAN  | CE  |                      |          |          |          |              |
|  |   |   | L <sub>D</sub>       | -        | 5.0      | -        | nH           |
|  |   |   | L <sub>S</sub>       | _        | 13       | -        | nH           |

<sup>1.</sup> Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

<sup>2.</sup> Switching characteristics are independent of operating junction temperature.

#### TYPICAL ELECTRICAL CHARACTERISTICS



40 35 30 25 20 15 10 5 0 25°C

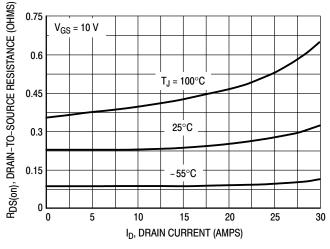
100°C

T<sub>J</sub> = -55°C

0 0 2 4 6 8 V<sub>GS</sub>, GATE-TO-SOURCE VOLTAGE (VOLTS)

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



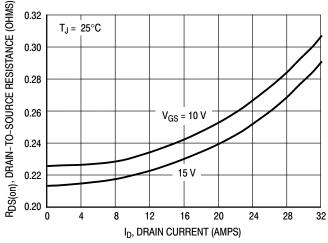
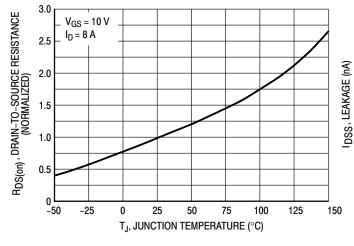


Figure 3. On–Resistance versus Drain Current and Temperature

Figure 4. On–Resistance versus Drain Current and Gate Voltage





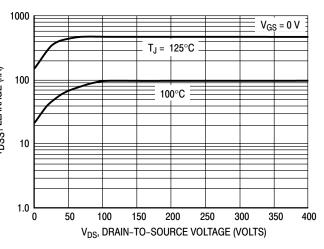


Figure 6. Drain-To-Source Leakage Current versus Voltage

#### POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ( $\Delta t$ ) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ( $I_{G(AV)}$ ) can be made from a rudimentary analysis of the drive circuit so that

$$t = Q/I_{G(AV)}$$

During the rise and fall time interval when switching a resistive load,  $V_{GS}$  remains virtually constant at a level known as the plateau voltage,  $V_{SGP}$ . Therefore, rise and fall times may be approximated by the following:

$$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$$

 $t_f = Q_2 \times R_G/V_{GSP}$ 

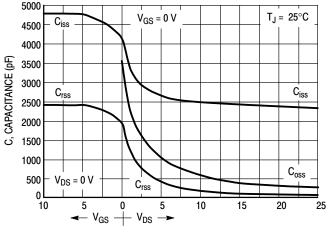
where

 $V_{GG}$  = the gate drive voltage, which varies from zero to  $V_{GG}$   $R_G$  = the gate drive resistance

and  $Q_2$  and  $V_{\mbox{\footnotesize GSP}}$  are read from the gate charge curve.

During the turn—on and turn—off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$$\begin{aligned} t_{d(on)} &= R_G \ C_{iss} \ In \ [V_{GG}/(V_{GG} - V_{GSP})] \\ t_{d(off)} &= R_G \ C_{iss} \ In \ (V_{GG}/V_{GSP}) \end{aligned}$$



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 7a. Capacitance Variation

The capacitance ( $C_{iss}$ ) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating  $t_{d(on)}$  and is read at a voltage corresponding to the on–state when calculating  $t_{d(off)}$ .

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

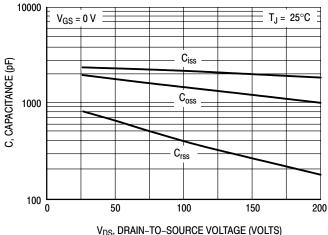


Figure 7b. High Voltage Capacitance
Variation

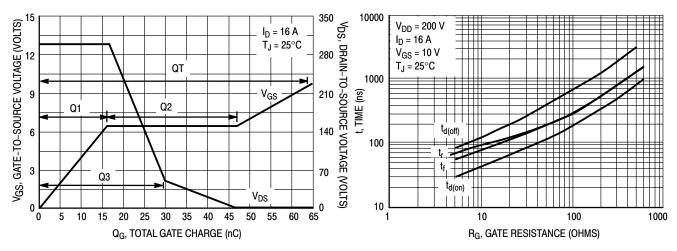


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

Figure 9. Resistive Switching Time Variation versus Gate Resistance

#### DRAIN-TO-SOURCE DIODE CHARACTERISTICS

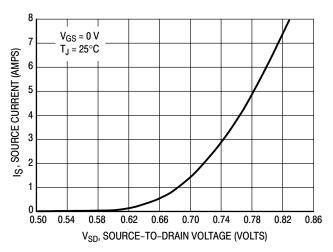


Figure 10. Diode Forward Voltage versus Current

### SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain—to—source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ( $T_{\rm C}$ ) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance—General Data and Its Use."

Switching between the off-state and the on-state may traverse any load line provided neither rated peak current ( $I_{DM}$ ) nor rated voltage ( $V_{DSS}$ ) is exceeded and the transition time ( $t_r$ , $t_f$ ) do not exceed 10  $\mu$ s. In addition the total power averaged over a complete switching cycle must not exceed ( $T_{J(MAX)} - T_C$ )/( $R_{\theta JC}$ ).

A Power MOSFET designated E-FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ( $I_{DM}$ ), the energy rating is specified at rated continuous current ( $I_{D}$ ), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous  $I_{D}$  can safely be assumed to equal the values indicated.

#### SAFE OPERATING AREA

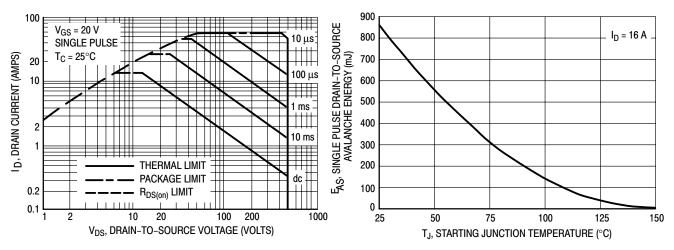


Figure 11. Maximum Rated Forward Biased Safe Operating Area

Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

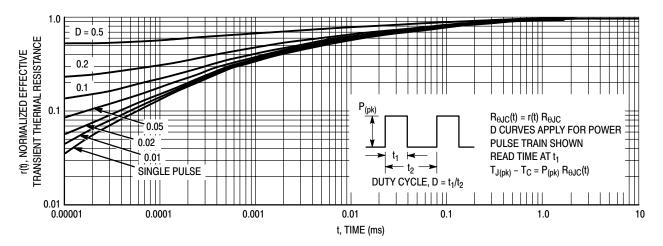


Figure 13. Thermal Response

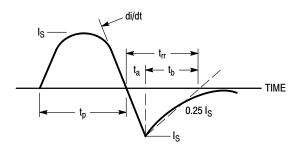
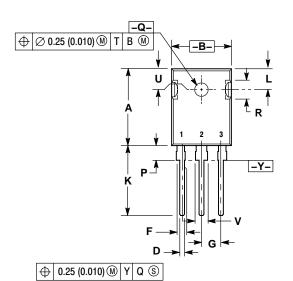
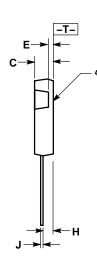


Figure 14. Diode Reverse Recovery Waveform

## **PACKAGE DIMENSIONS**

TO-247 CASE 340K-01 ISSUE C





- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.

|     | MILLIMETERS |              | INCHES    |           |  |
|-----|-------------|--------------|-----------|-----------|--|
| DIM | MIN         | MAX          | MIN       | MAX       |  |
| Α   | 19.7        | 20.3         | 0.776     | 0.799     |  |
| В   | 15.3        | 15.9         | 0.602     | 0.626     |  |
| U   | 4.7         | 5.3          | 0.185     | 0.209     |  |
| D   | 1.0         | 1.4          | 0.039     | 0.055     |  |
| Е   | 1.27 REF    |              | 0.050 REF |           |  |
| F   | 2.0         | 2.4          | 0.079     | 0.094     |  |
| G   | 5.5         | 3SC 0.216 BS |           | BSC       |  |
| H   | 2.2         | 2.6          | 0.087     | 0.102     |  |
| J   | 0.4         | 0.8          | 0.016     | 0.031     |  |
| K   | 14.2        | 14.8         | 0.559     | 0.583     |  |
| L   | 5.5 NOM     |              | 0.217 NOM |           |  |
| P   | 3.7         | 4.3          | 0.146     | 0.169     |  |
| ø   | 3.55        | 3.65         | 0.140     | 0.144     |  |
| R   | 5.0 NOM     |              | 0.197     | 0.197 NOM |  |
| J   | 5.5 BSC     |              | 0.217 BSC |           |  |
| ٧   | 3.0         | 3 4          | 0 118     | 0 134     |  |

- STYLE 1: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN

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