SINGLE CHANNEL 0.7V DIFFERENTIAL-TO-LVTTL TRANSCEIVER

ICS85120611

General Description

The ICS8512061I is a transceiver which can interchange data across multipoint data bus structures.

The device has an LVTTL driver and one HCSL receiver driver. It translates between LVTTL signals and HCSL signals.

Features

- One HCSL output pair and one LVCMOS/LVTTL output
- One single-ended LVCMOS/LVTTL signal input
- LVTTL I/O signal: up to 250MHz
- HCSL interface pins in high impedance state when the device is powered down
- Power-up and power-down glitch-free
- Additive Phase Jitter, RMS: 0.23ps (typical)
- Full 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Applications

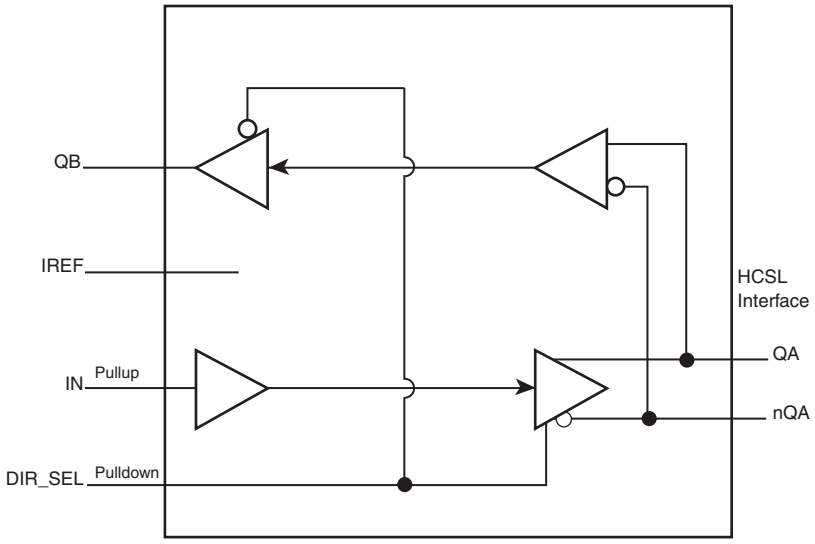
Backplane Transmission

Telecommunication System

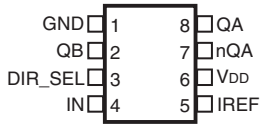
Data Communications

ATCA Clock Distribution

Block Diagram



Pin Assignment



ICS8512061I
8 Lead TSSOP
4.40mm x 3.0mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	GND	Power		Power supply ground.
2	QB	Output		Single-ended output. LVCMOS/LVTTL interface levels.
3	DIR_SEL	Input	Pulldown	HCSL receiver and driver direction select pin. When HIGH, selects the IN-to-QA/nQA path. When LOW, selects the QA/nQA-to-QB path. LVCMOS/LVTTL interface levels.
4	IN	Input	Pullup	Single-ended signal input. LVCMOS/LVTTL interface levels.
5	IREF	Input		An external fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode QA/nQA outputs.
6	V_{DD}	Power		Power supply pin.
7, 8	nQA, QA	Output		Differential transceiver pair. HCSL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4		pF
C_{PD}	Power Dissipation		V_{DD} = 3.6V		8		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	QB			20		Ω

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	129.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.0	3.3	3.6	V
I_{DD}	Power Supply Current				20	mA

Table 3B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	IN	V_{DD} = V_{IN} = 3.6V			5	µA
		DIR_SEL	V_{DD} = V_{IN} = 3.6V			150	µA
I_{IL}	Input Low Current	IN	V_{DD} = 3.6V, V_{IN} = 0V	-150			µA
		DIR_SEL	V_{DD} = 3.6V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1	QB	V_{DD} = 3.6V	2.6			V
V_{OL}	Output Low Voltage; NOTE 1	QB	V_{DD} = 3.6V			0.5	V

NOTE: Outputs terminated with 50Ω to V_{DD}/2. See Parameter Measurement Information Section, *Output Load Test Circuit diagram.*

Table 3C. Differential DC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{PP}	Peak-to-Peak Voltage; NOTE 1	DIR_SEL = 0	0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2	DIR_SEL = 0	GND + 0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

AC Electrical Characteristics

Table 4A. LVTTL (QB) Output Mode, Receiver AC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay, NOTE 1	QA/nQA to QB	1.7		2.5	ns
*t*jit	Buffer Additive Phase Jitter, RMS	100MHz, Integration Range: 12kHz – 20MHz		0.23		ps
t_R/t_F	Output Rise/Fall Time	20% - 80%	200		700	ps
odc	Output Duty Cycle		40		60	%

NOTE 1: Measured from V_{DD}/2 input cross point to the output at V_{DD}/2.

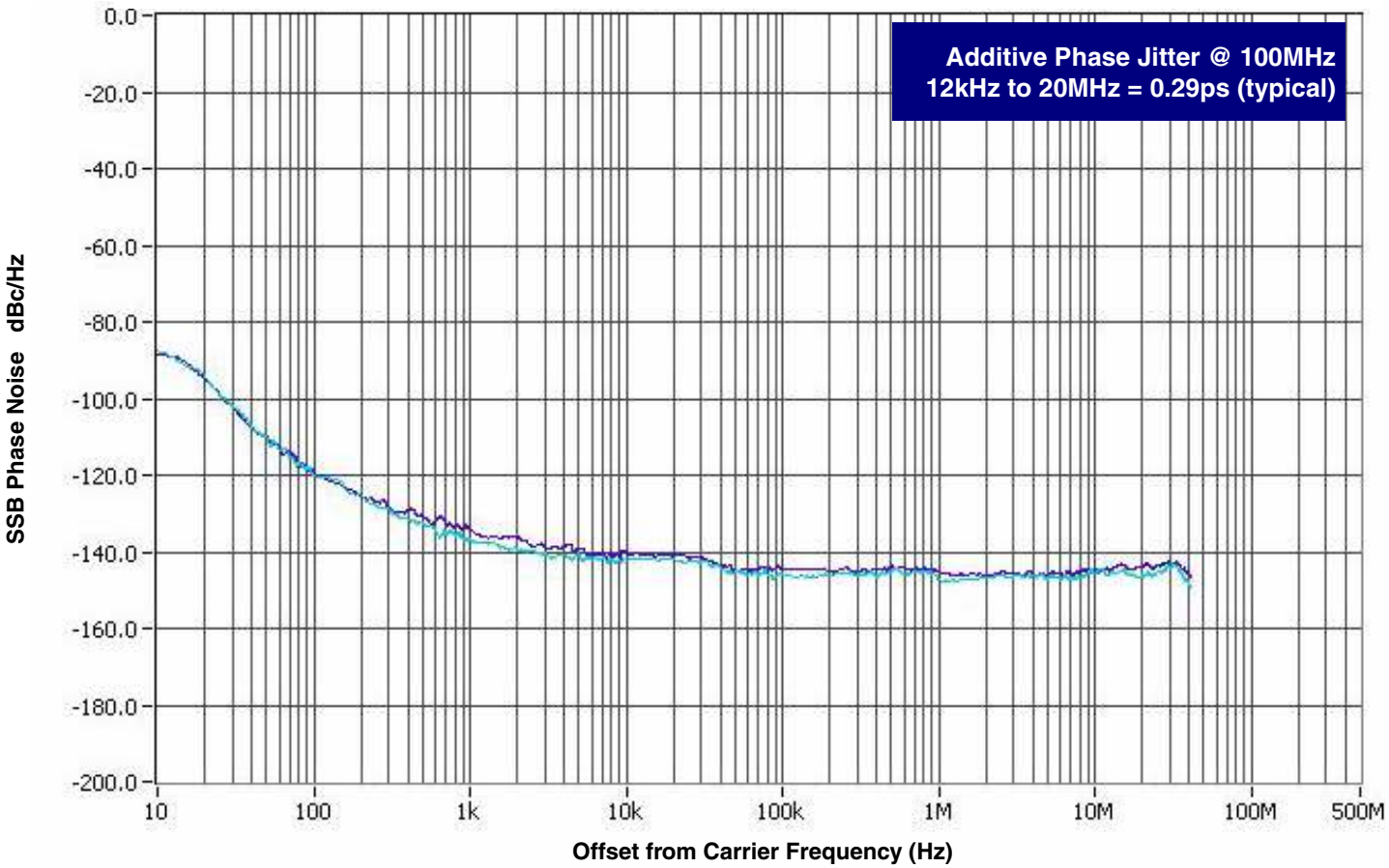
Table 4B. HCSL (QA/nQA) AC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
$t$jit	Buffer Additive Phase Jitter, RMS	100MHz, Integration Range: 12kHz – 20MHz		0.29		ps
t_{PD}	Propagation Delay, NOTE 1	IN to QA/nQA	1.1		1.7	ns
Rise Edge Rate	Rising Edge Rate; NOTE 2, 3		0.6		4.0	V/ns
Fall Edge Rate	Falling Edge Rate; NOTE 2, 3		0.6		4.0	V/ns
V_{rb}	Ringback Voltage; NOTE 2, 4		-100		100	V
V_{MAX}	Absolute Max Output Voltage; NOTE 5, 6				1150	mV
V_{MIN}	Absolute Min Output Voltage; NOTE 5, 7		-300			mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 5, 8, 9		250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 5, 8, 10				140	mV
odc	Output Duty Cycle; NOTE 11		45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from $V_{DD}/2$ input cross point to the differential output crossing point.
NOTE 2: Measurement taken from differential waveform.
NOTE 3: Measurement from -150mV to +150mV on the differential waveform (derived from QA minus nQA). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.
NOTE 4: T_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100 differential range. See Parameter Measurement Information Section.
NOTE 5: Measurement taken from single-ended waveform.
NOTE 6: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 7: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
NOTE 8: Measured at crossing point where the instantaneous voltage value of the rising edge of QA equals the Falling edge of nQA. See Parameter Measurement Information Section
NOTE 9: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Parameter Measurement Information Section.
NOTE 10: Defined as the total variation of all crossing voltage of Rising QA and Falling nQA. This is the maximum allowed variance in the V_{CROSS} for any particular system. See Parameter Measurement Information Section.
NOTE 11: Input duty cycle must be 50%.

Additive Phase Jitter (HCSL)

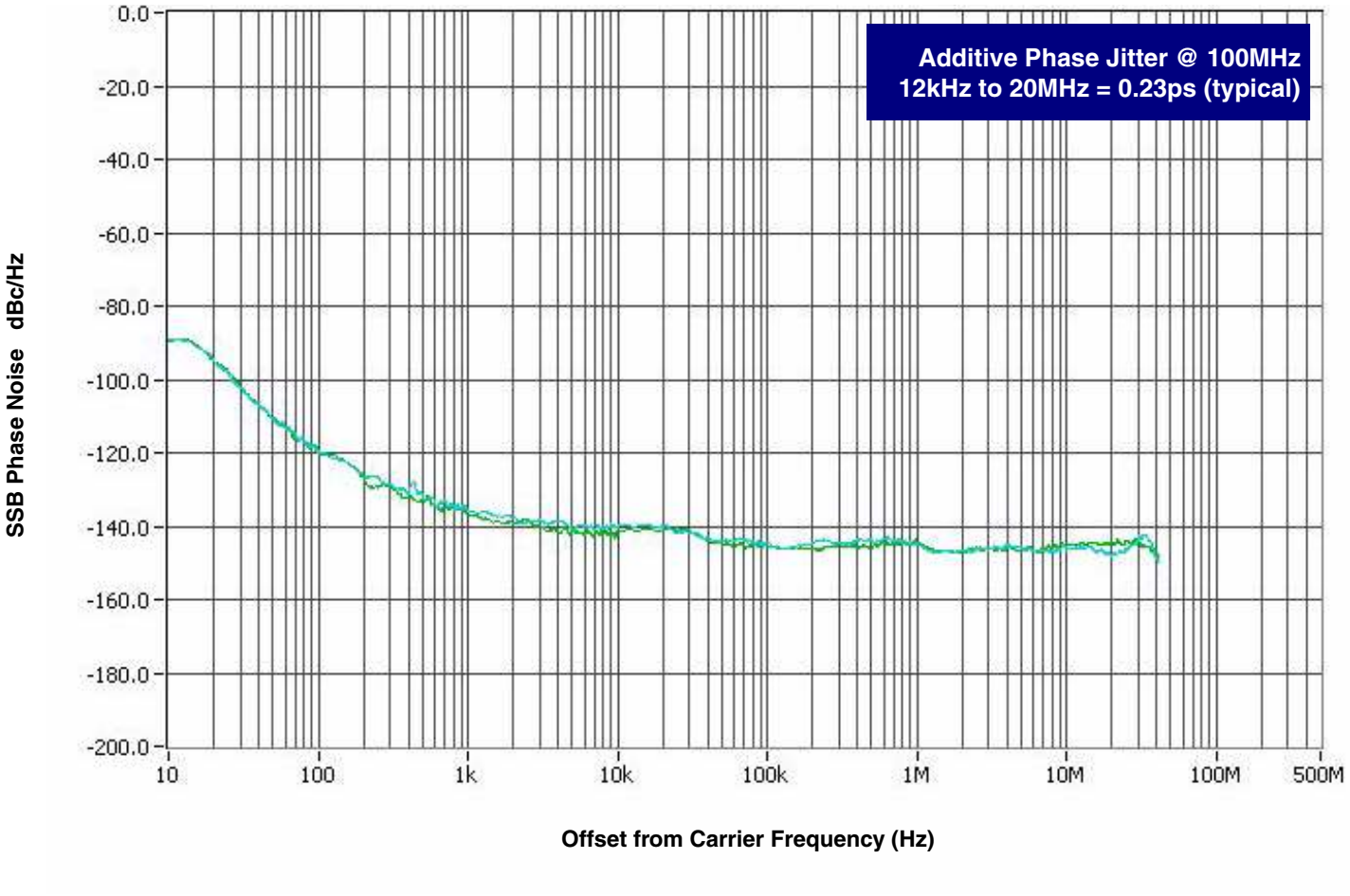
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

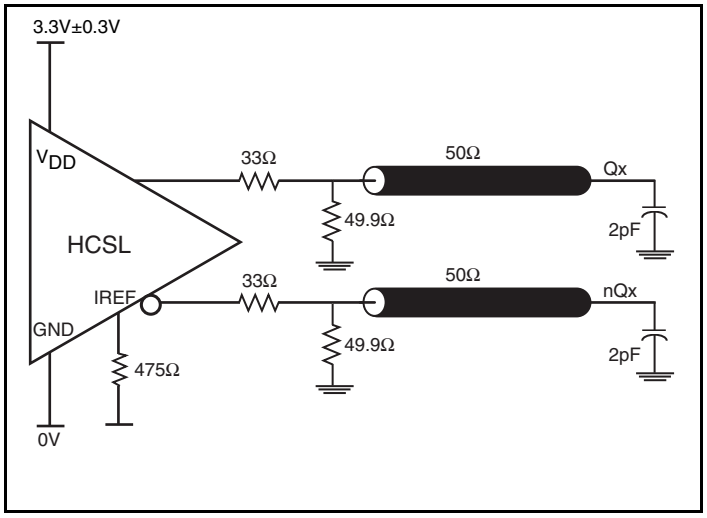
Additive Phase Jitter (LVCMOS)

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

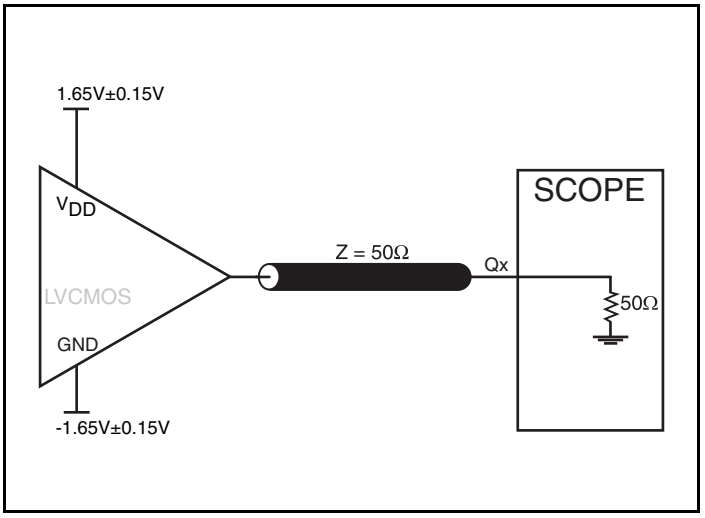


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

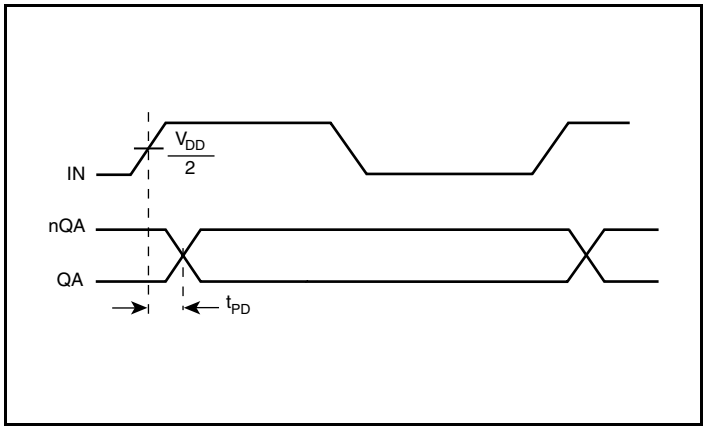
Parameter Measurement Information



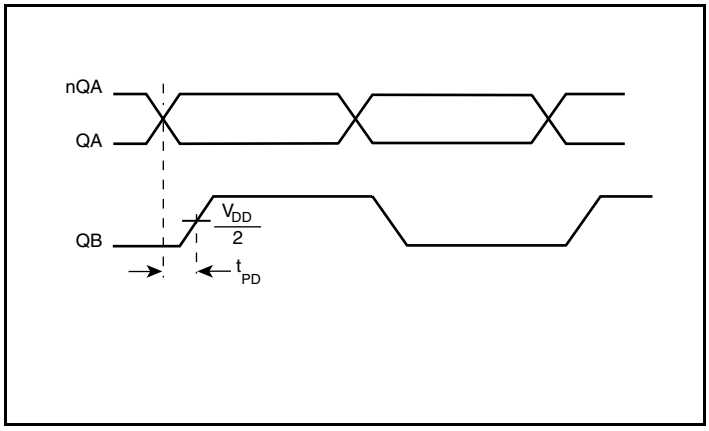
3.3V HCSL Output Load AC Test Circuit



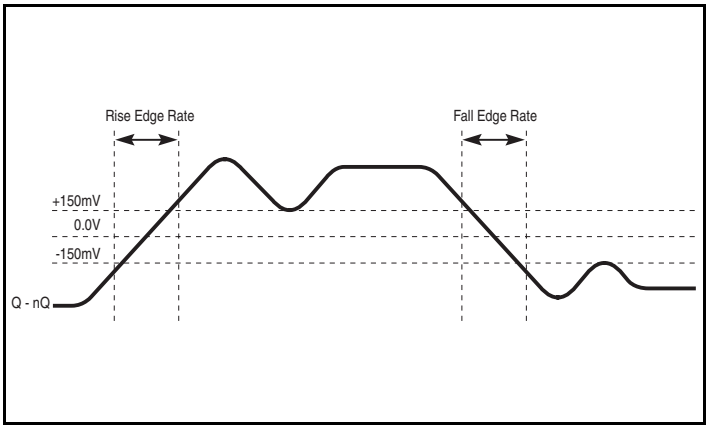
3.3V LVCMOS Output Load AC Test Circuit



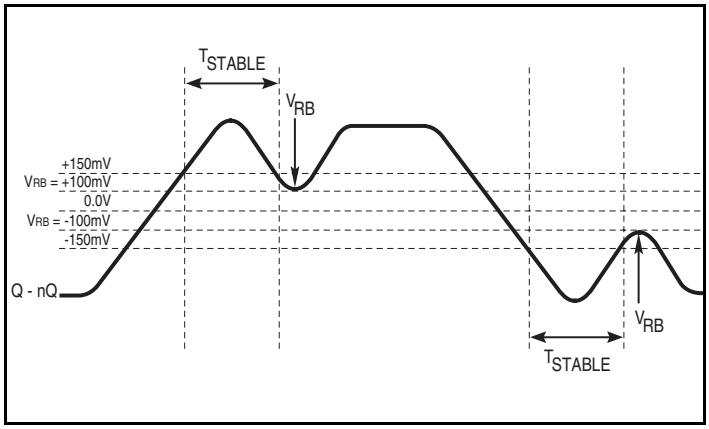
Differential Propagation Delay



LVCMOS Propagation Delay

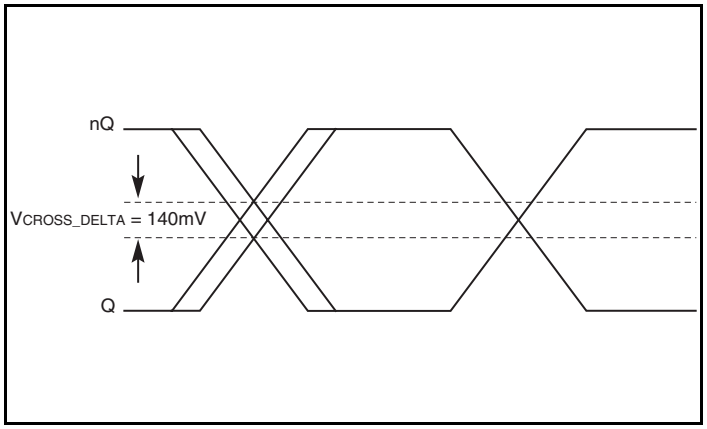


Differential Measurement Points for Rise/Fall Time

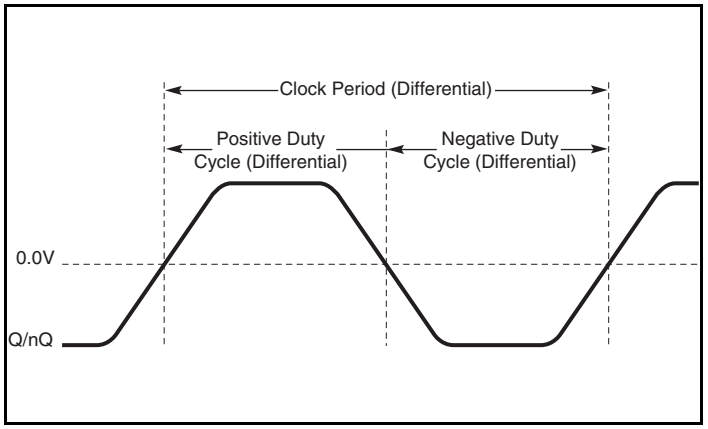


Differential Measurement Points for Ringback

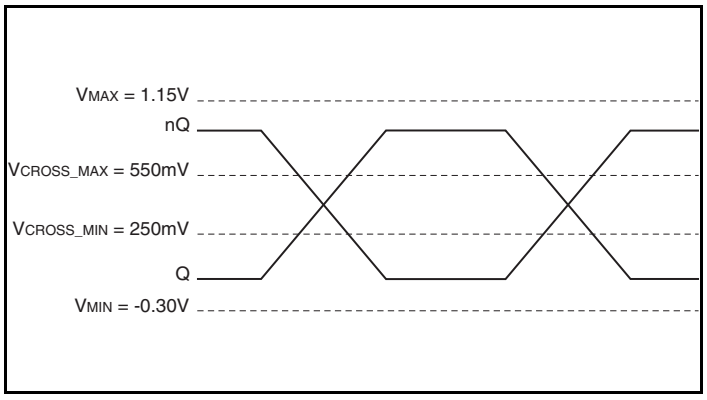
Parameter Measurement Information, continued



Single-ended Measurement Points for Delta Cross Point



Differential Measurement Points for Duty Cycle/Period



Single-ended Measurement Points for Absolute Cross Point/Swing

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins has internal pull-ups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVCMOSOutput

All unused LVCMOS output can be left floating. There should be no trace attached.

Recommended Termination

Figure 1A is the recommended termination for applications which require the receiver and driver to be on a separate PCB. All traces should be 50Ω impedance.

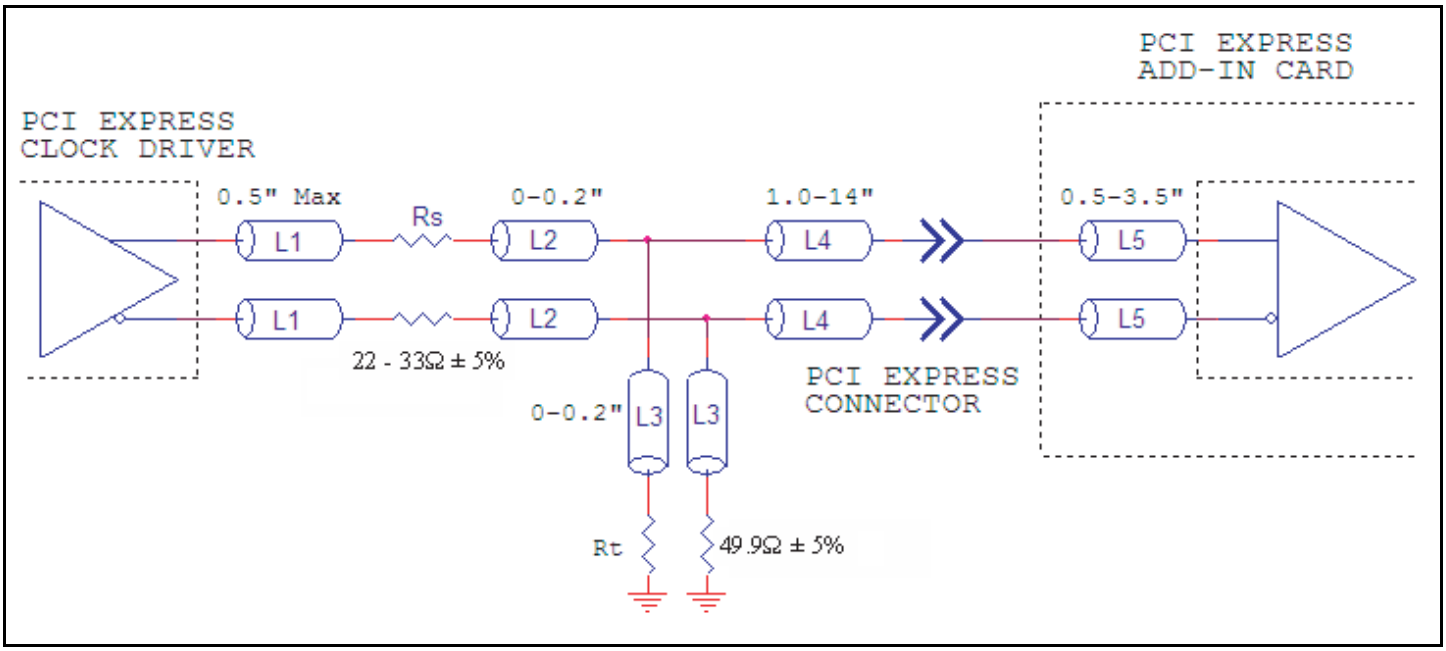


Figure 1A. Recommended Termination

Figure 1B is the recommended termination for applications which require a point to point connection and contain the driver and receiver on the same PCB. All traces should all be 50Ω impedance.

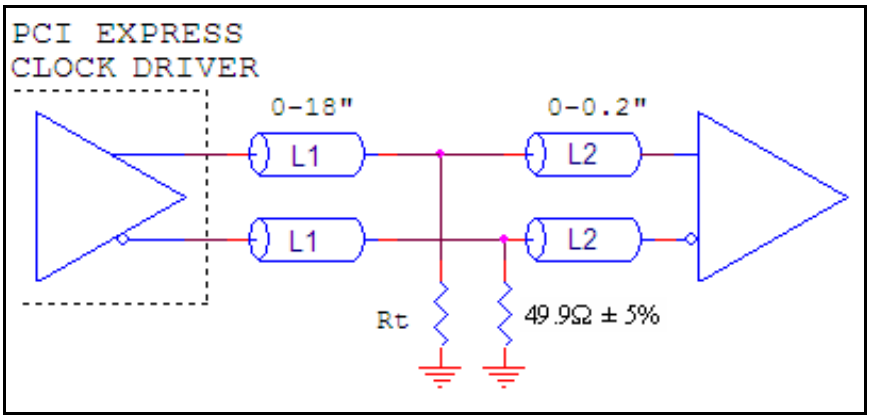


Figure 1B. Recommended Termination

Power Considerations (HCSL Outputs)

This section provides information on power dissipation and junction temperature for the ICS8512061I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8512061I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 0.3V = 3.6V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX}= 3.6V *20mA = **72mW**
- Power (outputs)$_{MAX}$ = **46.8mW/Loaded Output pair**

Total Power$_{\_MAX}$ = 72mW + 46.8mW = **118.8mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 129.5°C/W per Table 5A below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.119W * 129.5°C/W = 100.4°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 5A. Thermal Resistance θ_{JA} for 8 Lead TSSOP, Forced Convection

θ_{JA} **vs. Air Flow**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5	123.5

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 2.*

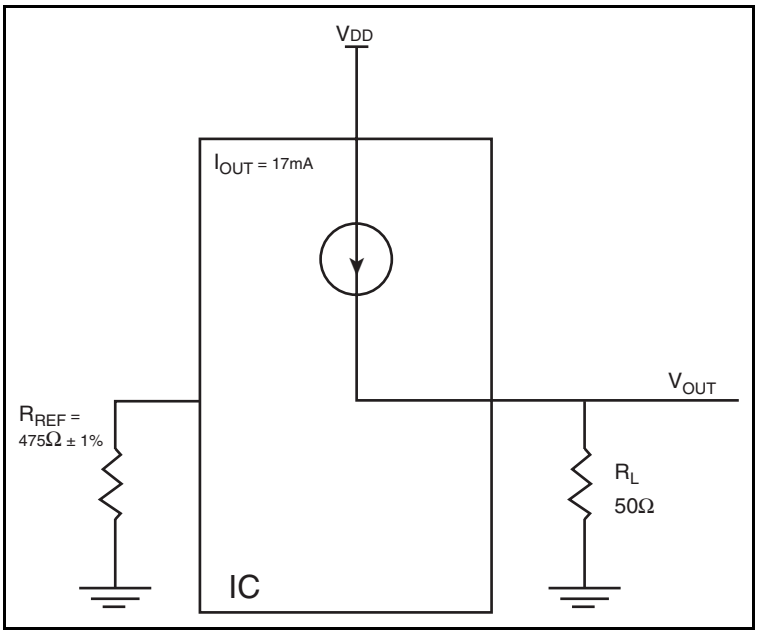


Figure 2. HCSL Driver Circuit and Termination

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DD_MAX}.

Power $= (V_{DD\_MAX} - V_{OUT}) * I_{OUT}$, since $V_{OUT} - I_{OUT} * R_L$

$= (V_{DD\_MAX} - I_{OUT} * R_L) * I_{OUT}$

$= (3.6V - 17mA * 50\Omega) * 17mA$

Total Power Dissipation per output pair = **46.8mW**

Power Considerations (LVCMOS Outputs)

This section provides information on power dissipation and junction temperature for the ICS8512061I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8512061I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 0.3V = 3.6V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$= 3.6V *20mA = **72mW**
- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{DD}/2$
  Output Current $I_{OUT} = V_{DD\_MAX} / [2 * (50Ω + R_{OUT})]$ = 3.6V / [2 * (50Ω + 20Ω)] = **25.7mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power $(R_{OUT}) = R_{OUT} * (I_{OUT})^2$ = 20Ω * (25.7mA)^2 = **13.2mW per output**

Dynamic Power Dissipation at 250MHz

Power (250MHz) = C_{PD} * Frequency * $(V_{DD})^2$ = 8pF * 250MHz * (3.6V)^2 = **25.9mW per output**

Total Power

= Power $(core)_{MAX}$ + Power (R_{OUT}) + Power (250MHz)
= 72mW + 13.2mW + 25.9mW
= 111.1mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 129.5°C/W per Table 5B below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.111W *129.5°C/W = 99.4°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 5B. Thermal Resistance θ_{JA} for 8 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5	123.5

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 8 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5	123.5

Transistor Count

The transistor count for ICS8512061I is: 294

Package Outline and Package Dimensions

Package Outline - G Suffix for 8 Lead TSSOP

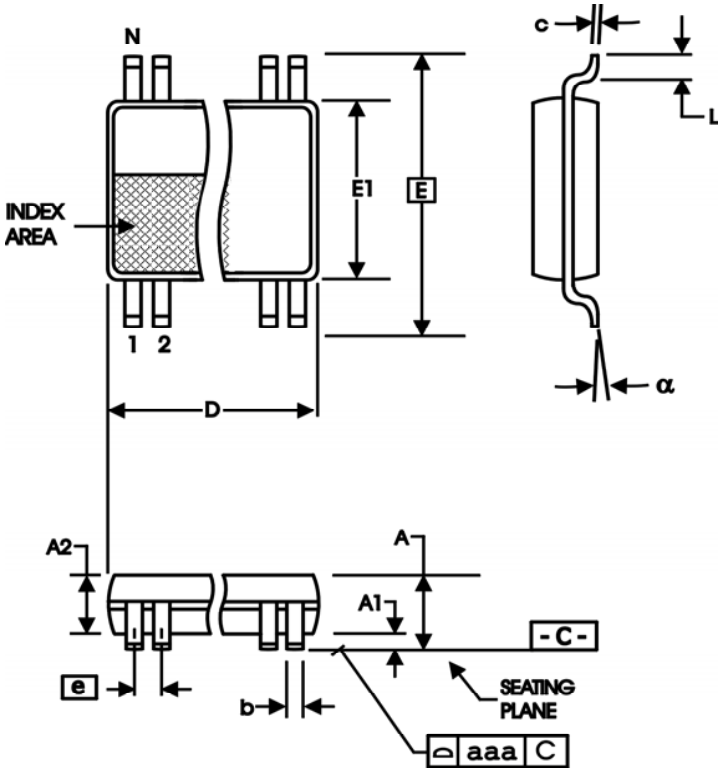


Table 7. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	8	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8512061AGILF	61AIL	“Lead-Free” 8 Lead TSSOP	Tube	-40°C to 85°C
8512061AGILFT	61AIL	“Lead-Free” 8 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T3C	3	Added Differential DC Characteristics Table.	11/19/08

Contact Information:

www.IDT.com

Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

Technical Support
netcom@idt.com
+480-763-2056

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800-345-7015 (inside USA)
+408-284-8200 (outside USA)