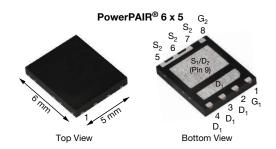
Vishay Siliconix

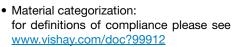
# **Dual N-Channel 30 V (D-S) MOSFET**



PRODUCT SUMMARY								
	CHANNEL-1	CHANNEL-2						
V <sub>DS</sub> (V)	30	30						
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10 \text{ V}$	0.0120	0.0064						
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5 \text{ V}$	0.0145	0.0083						
Q <sub>g</sub> typ. (nC)	6.8	21						
I <sub>D</sub> (A) <sup>a</sup>	16	16						
Configuration	Dual							

#### **FEATURES**

- TrenchFET® power MOSFET
- 100 % R<sub>g</sub> and UIS tested

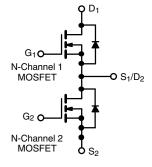




ROHS COMPLIANT HALOGEN FREE

#### **APPLICATIONS**

- Notebook system power
- POL
- Synchronous buck converter



ORDERING INFORMATION	
Package	PowerPAIR 6 x 5
Lead (Pb)-free and halogen-free	SiZ902DT-T1-GE3

PARAMETER	SYMBOL	CHANNEL-1	CHANNEL-2	UNIT	
Drain-source voltage		V <sub>DS</sub>	30	30	V
Gate-source voltage		V <sub>GS</sub>	± 20	± 20	v
	T <sub>C</sub> = 25 °C		16 <sup>a</sup>	16 a	
Continues during surrout (T. 150 °C)	T <sub>C</sub> = 70 °C		16 <sup>a</sup>	16 <sup>a</sup>	
Continuous drain current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	14.3 b, c	16 <sup>a, b, c</sup>	
	T <sub>A</sub> = 70 °C		11.4 <sup>b, c</sup>	16 <sup>a, b, c</sup>	_
Pulsed drain current (t = 300 μs)		I <sub>DM</sub>	50	80	A .
Oction and the design of the second	T <sub>C</sub> = 25 °C		16 a	16 <sup>a</sup>	
Continuous source-drain diode current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	3.4 b, c	4.1 b, c	
Single pulse avalanche current	1 0111	I <sub>AS</sub>	18	30	
Single pulse avalanche energy	<del></del>		16	45	mJ
	T <sub>C</sub> = 25 °C		29	66	
Mandan and a sure disciplation	T <sub>C</sub> = 70 °C		18	42	14/
Maximum power dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	4.2 b, c	5 b, c	W
	T <sub>A</sub> = 70 °C		2.7 b, c	3.2 b, c	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to	°C	
Soldering recommendations (peak temper		260			

THERMAL RESISTANCE RATINGS									
PARAMETER		SYMBOL	CHAN	NEL-1	CHAN	NEL-2	UNIT		
		STIVIDUL	TYP.	MAX.	TYP.	MAX.	UNIT		
Maximum junction-to-ambient b, f	t ≤ 10 s	R <sub>thJA</sub>	24	30	20	25	°C/W		
Maximum junction-to-case (drain)	Steady state	R <sub>thJC</sub>	3.4	4.3	1.5	1.9	C/VV		

#### Notes

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 10 s
- d. See solder profile (<a href="www.vishay.com/doc?73257">www.vishay.com/doc?73257</a>). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- f. Maximum under steady state conditions is 65 °C/W for channel-1 and 57 °C/W for channel-2



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ARAMETER SYMBOL TEST CONDITIONS					TYP.	MAX.	UNIT	
Static								
Drain-source breakdown voltage	V	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	Ch-1	30	-	-	V	
Drain-source breakdown voltage	$V_{DS}$	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	Ch-2	30	-	-	V	
V <sub>DS</sub> temperature coefficient	AV /T		Ch-1	-	33	-		
VDS temperature coemicient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 250 μA	Ch-2	1	33	-	mV/°0	
V <sub>GS(th)</sub> temperature coefficient	$\Delta V_{GS(th)}/T_J$	10 – 200 μΑ	Ch-1	ı	-5	-	IIIV/ C	
VGS(th) temperature coefficient	△VGS(th)/ 1J		Ch-2	-	-4.6	-		
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	Ch-1	1	-	2.2	V	
date source in esticia voltage	▼GS(tn)	V <sub>DS</sub> = V <sub>GS</sub> , i <sub>D</sub> = 200 μ/ (	Ch-2	1	-	2.2	•	
Sate-source leakage $I_{GSS}$ $V_{DS} = 0 \text{ V}, V_{GS} = 0 \text{ V}$	$V_{DS} = 0 \text{ V}, V_{GS} = +20 \text{ V}$	Ch-1	-	=	± 100	nA		
and source roundge	1655	105 - 5 V, VGS - 125 V	Ch-2	-	-	± 100		
		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$	Ch-1	-	-	1		
Zero gate voltage drain current	I <sub>DSS</sub>		Ch-2	-	-	1	μA	
_oro gate veriage aram carrent	.033	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	Ch-1	-	-	5	μ/.	
		103 00 1, 103 0 1, 1, 00 0	Ch-2	-	-	5		
On-state drain current <sup>b</sup>	ID(an)	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	Ch-1	20	=	-	A	
	I <sub>D(on)</sub>		Ch-2	20	-	-		
Drain-source on-state resistance <sup>b</sup>	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, I_D = 13.8 \text{ A}$	Ch-1	-	0.0100	0.0120	Ω	
		$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	Ch-2	-	0.0053	0.0064		
		$V_{GS} = 4.5 \text{ V}, I_D = 12.6 \text{ A}$	Ch-1	-	0.0120	0.0145		
		$V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$	Ch-2	-	0.0068	0.0083		
Forward transconductance b	Q.	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 13.8 A		-	47	-	s	
Torward transconductance	9 <sub>fs</sub>	$V_{DS} = 10 \text{ V}, I_D = 20 \text{ A}$	Ch-2	-	63	-	0	
Dynamic <sup>a</sup>			r		T	ı	1	
Input capacitance	C <sub>iss</sub>	Channel-1	Ch-1	-	790	-		
	- 155	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	Ch-2	-	2600	-	_	
Output capacitance	C <sub>oss</sub>		Ch-1	-	190	-	pF	
	Ooss	Channel-2	Ch-2	-	485	-	ρ.	
Reverse transfer capacitance	C <sub>rss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	Ch-1	-	76	-		
	0155		Ch-2	-	215	-		
		$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 13.8 \text{ A}$	Ch-1	-	14	21		
Total gate charge	$Q_g$	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	Ch-2	-	43	65		
Total gate charge	₩g	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 13.8 \text{ A}$	Ch-1	-	6.8	11		
		$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$	Ch-2	-	21	32	nC	
Gate-source charge	Q <sub>gs</sub>	Channel-1	Ch-1	-	2.6	-		
		$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 13.8 \text{ A}$	Ch-2	-	8.1	-		
0		Channel-2	Ch-1	-	1.9	-		
Gate-drain charge	$Q_{gd}$	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A		-	6.5	-	1	
Gate resistance	$R_g$	£ 4.441	Ch-1	0.4	2	-	_	
		f = 1 MHz	Ch-2	0.3	1.5	-	Ω	



www.vishay.com

# Vishay Siliconix

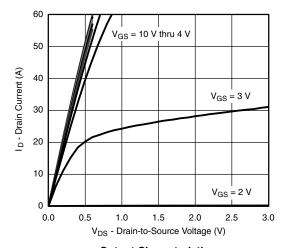
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Dynamic <sup>a</sup>							
Turn-on delay time	<b>+</b> >		Ch-1	-	15	30	
Turr-on delay time	t <sub>d(on)</sub>	Channel-1 $V_{DD} = 15 \text{ V}, R_{L} = 1.5 \Omega,$	Ch-2	-	23	50	
Rise time	t <sub>r</sub>	$V_{DD} = 13 \text{ V, } R_L = 1.3 \Omega,$ $I_D \cong 10 \text{ A, } V_{GEN} = 4.5 \text{ V, } R_q = 1 \Omega$	Ch-1	-	12	20	
THIS LITTE	-r	b v aliv v g	Ch-2	-	20	40	
Turn-off delay time	t <sub>d(off)</sub>	Channel-2	Ch-1	-	20	40	
Turn on delay lime	<b>-</b> a(on)	$V_{DD} = 15 \text{ V}, R_{L} = 1.5 \Omega,$	Ch-2	-	35	70	
Fall time	t <sub>f</sub>	$I_D\cong 10$ A, $V_{GEN}=4.5$ V, $R_g=1~\Omega$	Ch-1	-	10	20	
T dir dirito	4		Ch-2	-	10	20	ns
Turn-on delay time	t <sub>d(on)</sub>		Ch-1	-	10	20	
Tam on dolay amo	-a(on)	Channel-1 $V_{DD} = 15 \text{ V}, R_{L} = 1.5 \Omega,$	Ch-2	-	22	25	
Rise time	t <sub>r</sub>	$I_D \cong 10 \text{ A}, N_C = 1.3 \Omega$ $I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_q = 1 \Omega$	Ch-1	-	12	20	
11100 11110	4	D / GEN / g	Ch-2	-	10	20	
Turn-off delay time	t <sub>d(off)</sub>	Channel-2	Ch-1	-	20 40	40	
Turn on delay time	<b>ч</b> а(оп)	$V_{DD} = 15 \text{ V}, R_{L} = 1.5 \Omega,$	Ch-2	-	35	70	
Fall time	t <sub>f</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	Ch-1	-	10	20	
Tun time	4		Ch-2	-	10	20	
<b>Drain-Source Body Diode Characteri</b>	stics						
Continuous source-drain diode current	Is	T <sub>C</sub> = 25 °C	Ch-1	-	-	16	A
Communication and Communications	'5		Ch-2	-	-	16	
Pulse diode forward current <sup>a</sup>	I <sub>SM</sub>		Ch-1	-	-	50	
Talse aloge forward current	IOIVI		Ch-2	-	-	80	
Body diode voltage	$V_{SD}$	$I_S = 10 \text{ A}, V_{GS} = 0 \text{ V}$	Ch-1	-	0.85	1.2	V
	- 30		Ch-2	-	0.8	1.2	_
Body diode reverse recovery time	t <sub>rr</sub>		Ch-1	-	20	40	ns
Dody aloue reverse receivery time	٠rr	Channel-1 I <sub>F</sub> = 10 A, di/dt = 100 A/μs,	Ch-2	-	25	50	110
Body diode reverse recovery charge	Q <sub>rr</sub>	$T_{ij} = 25  ^{\circ}\text{C}$	Ch-1	-	10	20	nC
Dody aloue foreign recovery charge	ζ <sub>II</sub>	ů	Ch-2	-	13	25	
Reverse recovery fall time	t <sub>a</sub>	Channel-2	Ch-1	-	11	-	
	*a	$I_F = 10 \text{ A, di/dt} = 100 \text{ A/}\mu\text{s,}$	Ch-2	-	12	-	ns
Reverse recovery rise time	t <sub>b</sub>	T <sub>J</sub> = 25 °C		-	9	-	] "10
Tievered todovery floo timo	٠b			-	13	-	

#### Notes

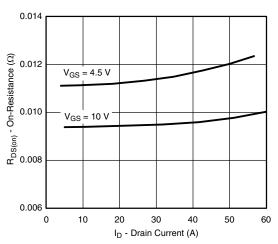
- a. Guaranteed by design, not subject to production testing
- b. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

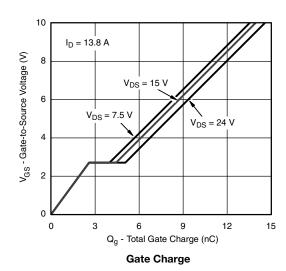


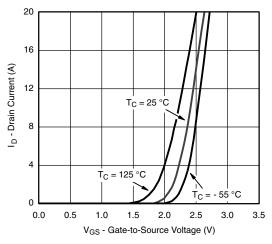


#### **Output Characteristics**

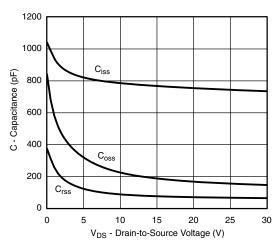


On-Resistance vs. Drain Current

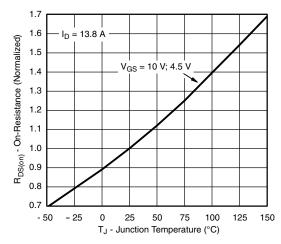




**Transfer Characteristics** 

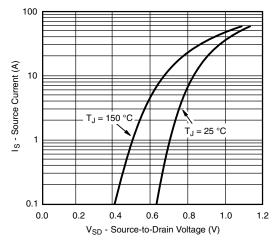


#### Capacitance

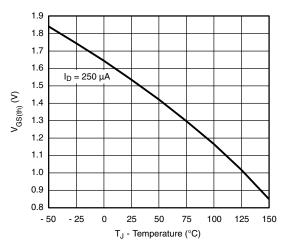


On-Resistance vs. Junction Temperature

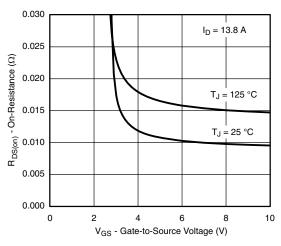




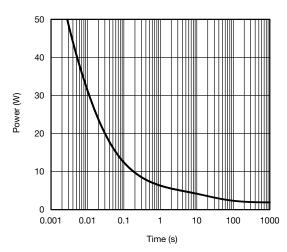
#### Source-Drain Diode Forward Voltage



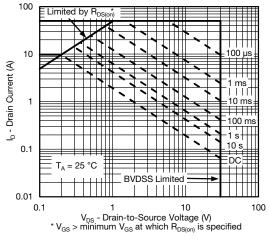
**Threshold Voltage** 



On-Resistance vs. Gate-to-Source Voltage

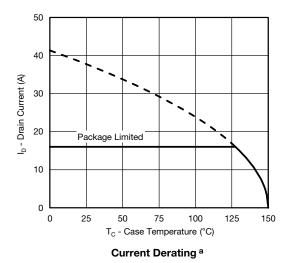


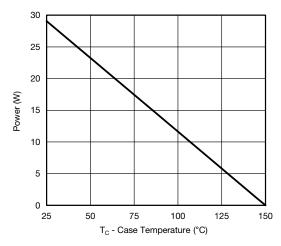
Single Pulse Power



Safe Operating Area, Junction-to-Ambient



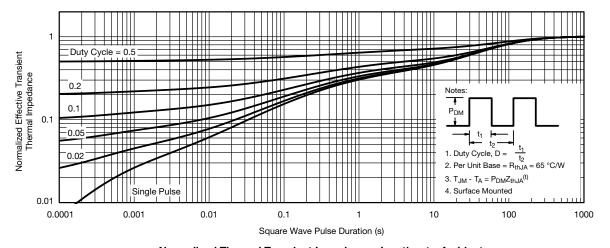




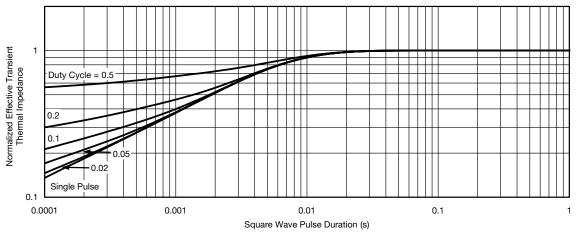
Power, Junction-to-Case

a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



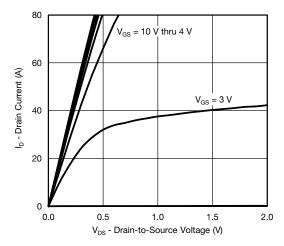


Normalized Thermal Transient Impedance, Junction-to-Ambient

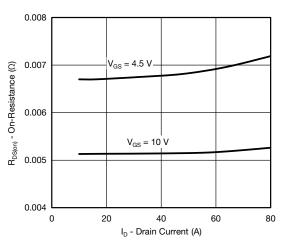


Normalized Thermal Transient Impedance, Junction-to-Case

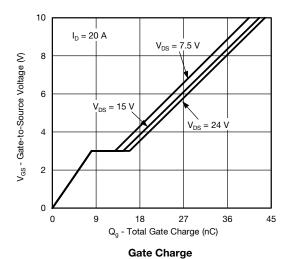




#### **Output Characteristics**

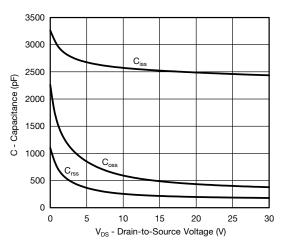


On-Resistance vs. Drain Current

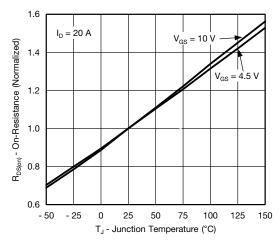


20 16 I<sub>D</sub> - Drain Current (A) 12 = 25 8 T<sub>C</sub> = 125 °C 55 °C 0.0 0.5 1.0 2.0 3.0 1.5 2.5 V<sub>GS</sub> - Gate-to-Source Voltage (V)

**Transfer Characteristics** 

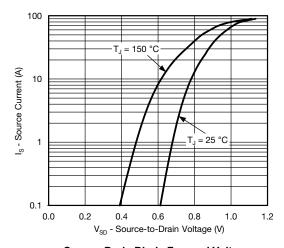


Capacitance

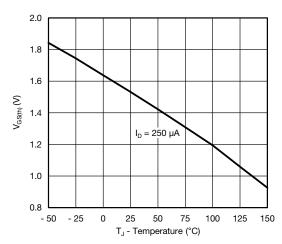


On-Resistance vs. Junction Temperature

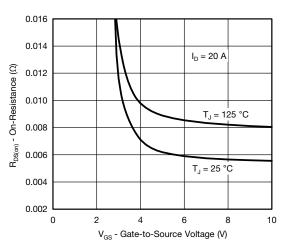




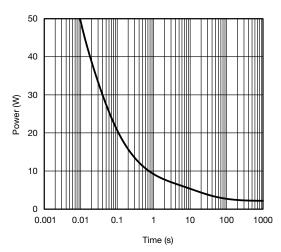
#### Source-Drain Diode Forward Voltage



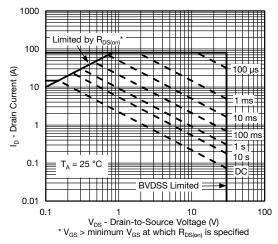
**Threshold Voltage** 



On-Resistance vs. Gate-to-Source Voltage



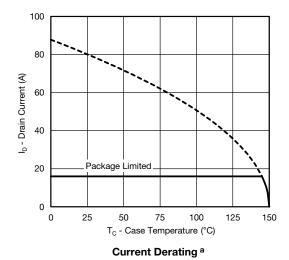
Single Pulse Power

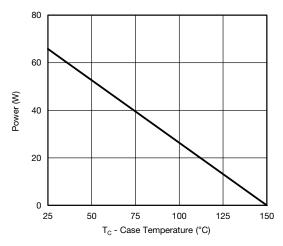


Safe Operating Area, Junction-to-Ambient

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# CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



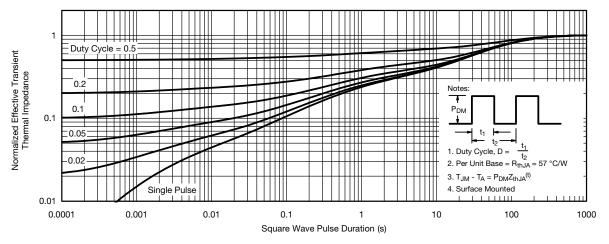


Power, Junction-to-Case

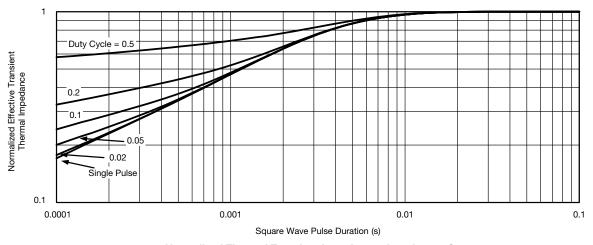
#### Note

a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient

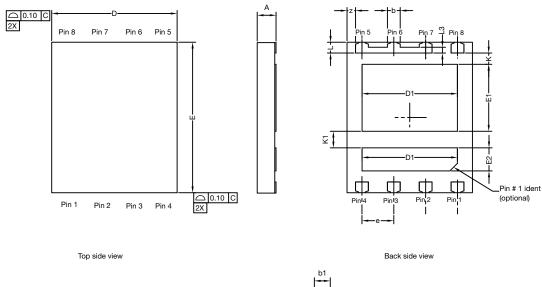


Normalized Thermal Transient Impedance, Junction-to-Case

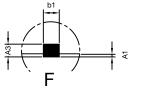
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?63465">www.vishay.com/ppg?63465</a>.



# PowerPAIR® 6 x 5 Case Outline





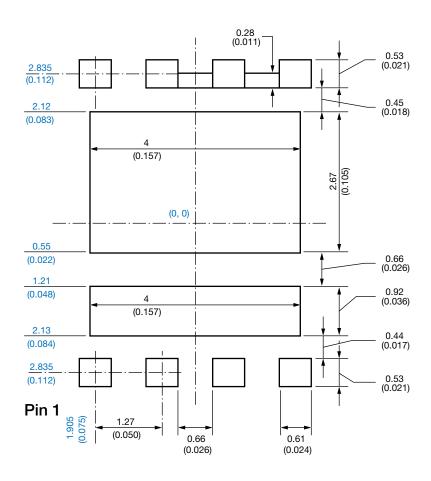


	MILLIMETERS			INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
А	0.70	0.75	0.80	0.028	0.030	0.032	
A1	0.00	-	0.10	0.000	-	0.004	
A3	0.15	0.20	0.25	0.006	0.007	0.009	
b	0.43	0.51	0.61	0.017	0.020	0.024	
b1		0.25 BSC			0.010 BSC		
D	4.90	5.00	5.10	0.192	0.196	0.200	
D1	3.75	3.80	3.85	0.148	0.150	0.152	
E	5.90	6.00	6.10	0.232	0.236	0.240	
E1 Option AA (for W/B)	2.62	2.67	2.72	0.103	0.105	0.107	
E1 Option AB (for BWL)	2.42	2.47	2.52	0.095	0.097	0.099	
E2	0.87	0.92	0.97	0.034	0.036	0.038	
е		1.27 BSC			0.050 BSC		
K Option AA (for W/B)	0.45 typ.				0.018 typ.		
K Option AB (for BWL)		0.65 typ.			0.025 typ.		
K1		0.66 typ.			0.025 typ.		
L	0.33	0.43	0.53	0.013	0.017	0.020	
L3	0.23 BSC 0.009 BSC						
Z	0.34 BSC 0.013 BSC						
ECN: T14-0782-Rev. C, 22-Dec- DWG: 6005	-14						

Revision: 22-Dec-14 1 Document Number: 63656



# Recommended Minimum PAD for PowerPAIR® 6 x 5



Dimensions in millimeters (inch)

#### Note

• Linear dimensions are in black, the same information is provided in ordinate dimensions which are in blue.



# **Legal Disclaimer Notice**

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