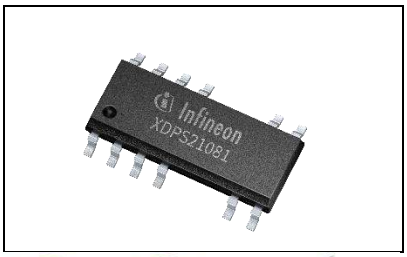
Forced Quasi Resonant ZVS Flyback controller

Based on FW: REV 1.0



Product Highlights

- Integrated 600 V startup cell for fast startup and direct bus voltage sensing
- Multi-mode operation with forced quasi resonant (FQR) Zero Voltage Switching (ZVS) mode
- DCM operation guaranteed
- Adaptive current limitation for variable Vout
- Supports low no load input power to meet stringent regulatory standard
- One pin UART interface for configuration

Features

- Low line QR, high line FQR ZVS
- Configurable ZVS enabled line voltage
- Low side ZVS MOSFET gate control
- ZVS optimization per variable Vout
- Built-in protection modes
- Brown-in and brownout detection via integrated HV startup cell
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Applications

- High density adapter/charger

Product Validation

- Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

The XDPS21081 is a digital PWM controller for high density adapter applications based on Forced Quasi-resonant ZVS flyback topology. It provides low line QR and high line FQR ZVS operation. A wide feature set is provided in a DSO-12 package and requires only a minimum of external components. An integrated ASSP digital engine provides advanced algorithms for multi-mode operation and protection features. A forced quasi resonant ZVS operation support optimized high density adapter system dimensioning. In addition a one-time-programmable (OTP) unit is integrated to provide a selective set of configurable parameters, which can be matched to a dedicated system design.

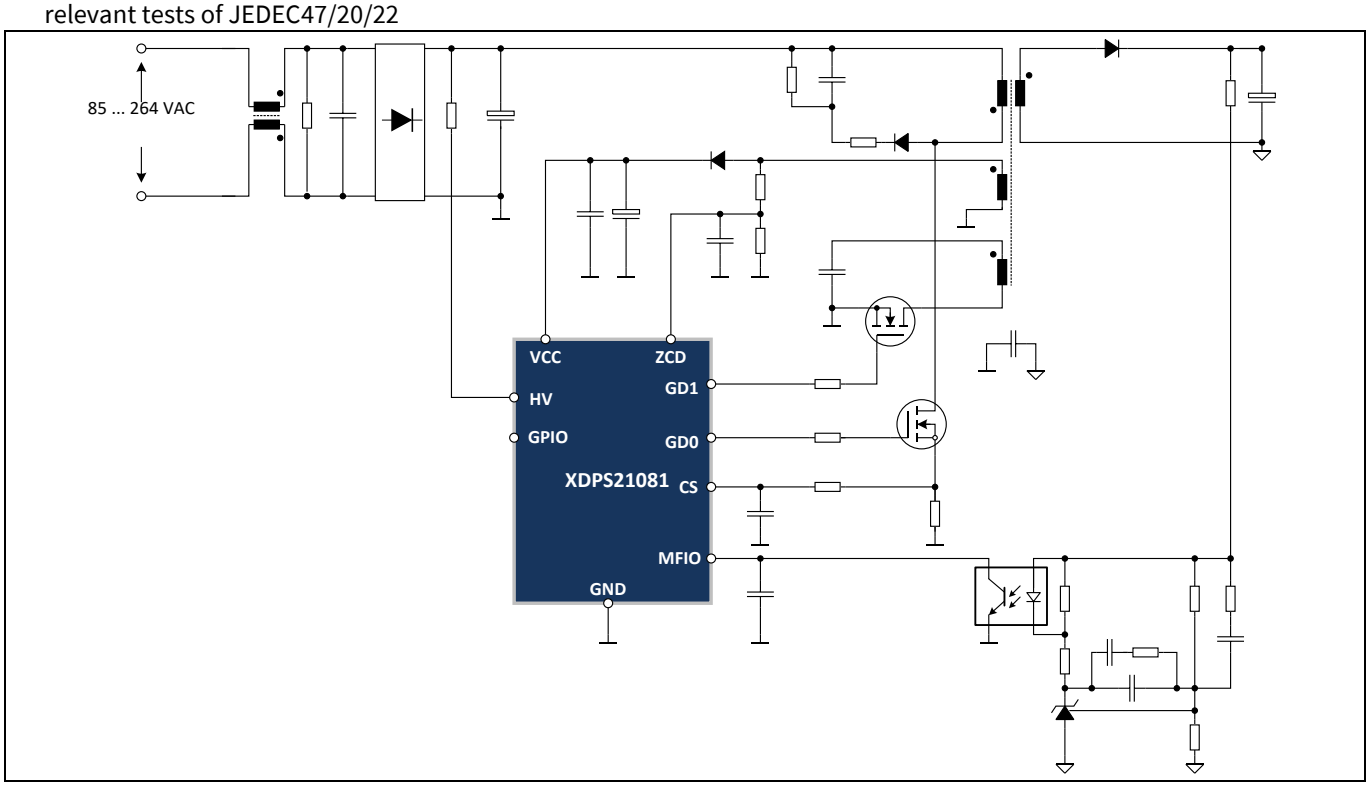


Figure 1 Typical application

Marking	Package	FW Revision	SP Ordering Code
XDPS21081	PG-DSO-12	REV 1.0	SP005415076

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1 Pin Configuration and Functionality

The pin configuration is shown in Figure 2 and the functions are described in Table 1.

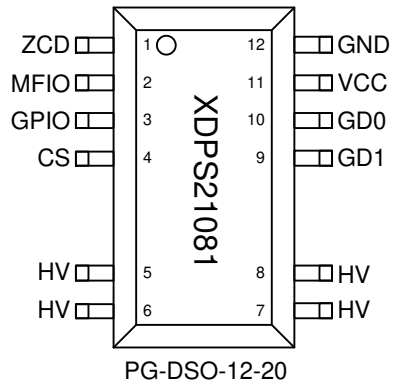

Figure 2 Pin Configuration of XDPS21081

Table 1 Pin Definitions and Functions

Symbol	Pin	Type	Function
ZCD	1	I	**Zero Crossing Detection** ZCD pin is connected to an auxiliary winding for zero crossing detection and positive pin voltage measurement.
MFIO	2	I	**Multi-Functional Input Output** MFIO pin is connected to an optocoupler that provides an amplified error signal for the PWM mode operation.
GPIO	3	IO	**Digital General Purpose Input Output** GPIO pin provides an UART interface until brown-in. It is switched to weak pull down mode and disabled UART function during normal operation.
CS	4	I	**Current Sense** CS pin is connected via a resistor in series to an external shunt resistor and the source of the power MOSFET.
HV	5, 6, 7, 8	I	**High Voltage Input** HV pin is connected to the rectified bulk voltage. An internally connected 600 V HV startup-cell is used for initial VCC charge. Furthermore brown-in and brownout detection is provided.
GD1	9	I	**FQR ZVS Signal Gate Driver Output** GD1 pin provides a gate driver pulse signal to initiate the forced quasi resonant ZVS mode operation.
GD0	10	O	**Gate Driver Output** Output for directly driving the main power MOSFET.
VCC	11	I	**Positive Voltage Supply** IC power supply.
GND	12	O	**Power and Signal Ground**

2 Representative Block Diagram

Figure 3 shows a simplified top level block diagram of the IC functionality.

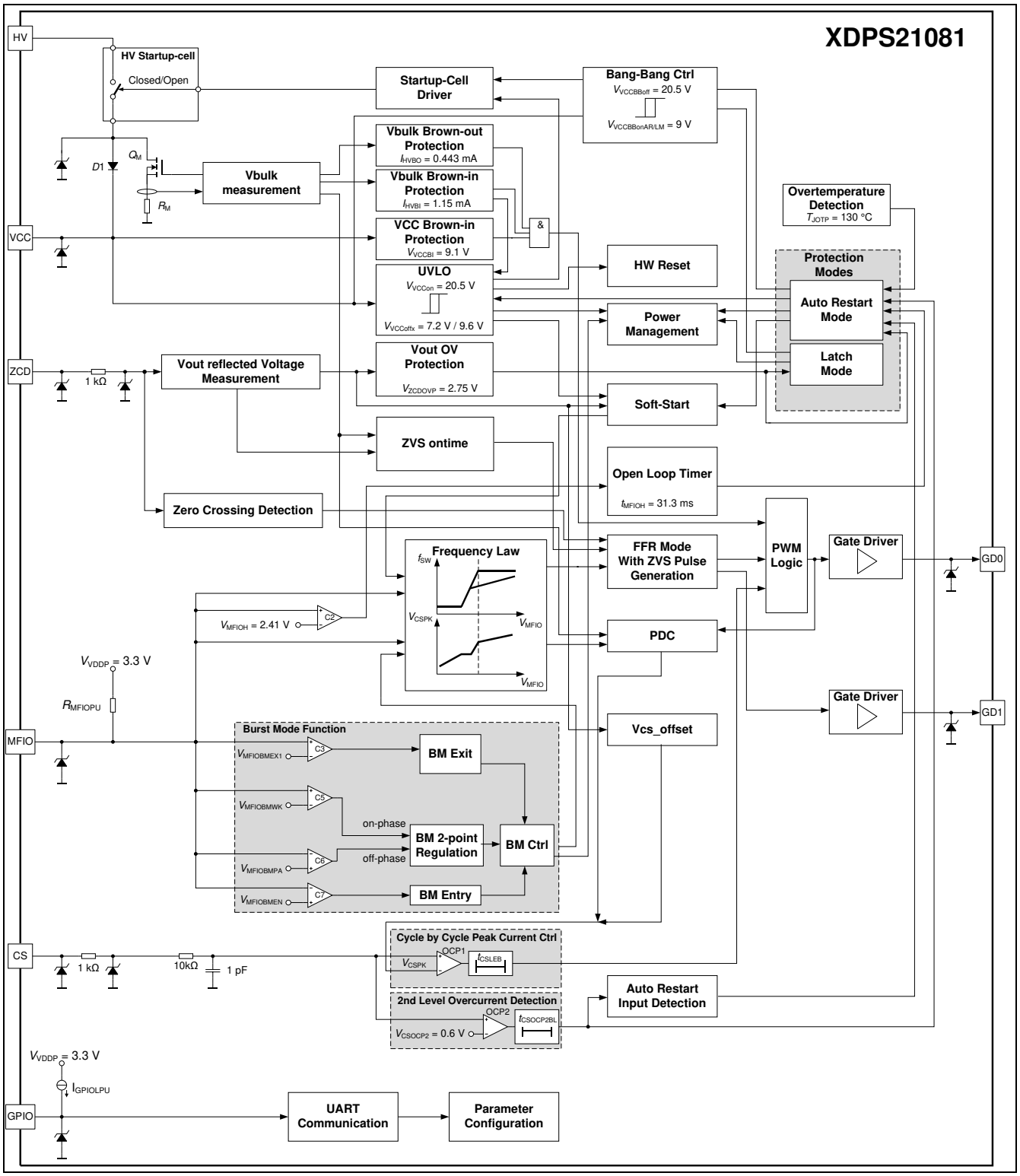

Figure 3 Representative Block Diagram of XDPS21081

3 Introduction

The XDPS21081 is a digital AC/DC current-mode controller for high density adapter applications. The IC provides a configurable multi-mode operation controlled by the feedback signal from the secondary side control loop. The multi-mode operation supports different operation modes like Quasi-resonant (QR) mode, FQR ZVS mode, (see chapter 4.2.12) or burst mode, frequency reduction mode depending on line and load conditions. With supporting those modes high power density designs can be dressed in a very flexible manner.

An embedded application specific digital core provides advanced algorithms for the multi-mode operation and a variety of protection features. Special analog and mixed-signal peripherals are integrated to support the requirements for low stand-by power.

The IC supports highest design flexibility in the application by means of an advanced set of configurable parameters and state machines, which supports very dedicated system dimensioning. The configuration can be done via a single pin UART interface at GPIO pin that supports in-circuit configuration. Chapter 5 contains the parameter default configuration setting for XDPS21081 and the correlated specific firmware version. Furthermore, it provides a mapping table for the defined FW symbols and the correlated data sheet parameters. Each listed parameter is specified in the electrical characteristics Chapter 6.

The following functional description in Chapter 4 is based on the default parameter setting in the configuration Chapter 5.

Chapter 7.1 provides information about the package outline and dimensions.

An appendix Chapter 9 provides additional information about specific electrical characteristics or test conditions.

The reference Chapter 10 provides an overview about correlated documents.

4 Functional Description

The functional description gives an overview about the integrated functions and features and their relationship. The mentioned parameters and equations are based on typical values at T_A = 25 °C. The correlated minimal and maximal values are shown in the electrical characteristics in Chapter 6.

The functional description is grouped in following sections:

Power supply management (Chapter 4.1)
Control features (Chapter 4.2)
Protection features (Chapter 4.3)

4.1 Power supply management

The power supply management ensures a reliable and robust IC operation. Depending on the operation mode of the control IC, the power supply management unit runs in different ways for VCC supply and for brown-in monitoring, which are described in the sequel:

- VCC capacitor charge-up and startup sequence (see Chapter 4.1.1)
- Brown-in monitoring (Chapter 4.1.2)
- Brown-out protection response (Chapter 4.1.3)
- During burst mode (QBM) operation (Chapter 4.1.4)
- Bang-bang mode during latch mode (LM) operation (Chapter 4.1.5.1)
- Bang-bang mode during auto-restart mode (ARM) operation (Chapter 4.1.5.2)

4.1.1 VCC capacitor charge-up and startup sequence

There are two main functions supported at HV pin by a resistor R_{HV} connected to the bulk capacitor (see Figure 5). They are the VCC capacitor charge-up, and the bulk voltage monitoring (see Chapter 4.1.2).

At beginning of a cold startup, the depletion startup cell is on. Once the AC line voltage is applied and charging the bulk capacitor, a current flows through the external resistor R_{HV} into HV pin. Via the integrated diode D1, that current may charge up the external VCC capacitor (see Figure 5). Once VCC voltage exceeds the threshold V_{VCCon} = 20.5 V, the startup cell is turned off, the control IC is enabled and the firmware boot sequence follows which takes about 1.2 ms. Both bulk voltage brown-in and VCC brown-in condition (see Chapter 4.3.4) are checked continuously. Once they both are above the brown-in level, respectively, the first GD0 pulse according to the soft-start control will be generated earliest after the 1.2 ms boot sequence time. The voltage V_{VCC} drops until the supply via the auxiliary winding (V_{VCCSS}) takes over the VCC supply (see Figure 4). For a proper system startup and operation, the supply voltage V_{VCC} must be always above the VCC off-threshold V_{VCCoff}=7.2 V (see Chapter 4.3.3).

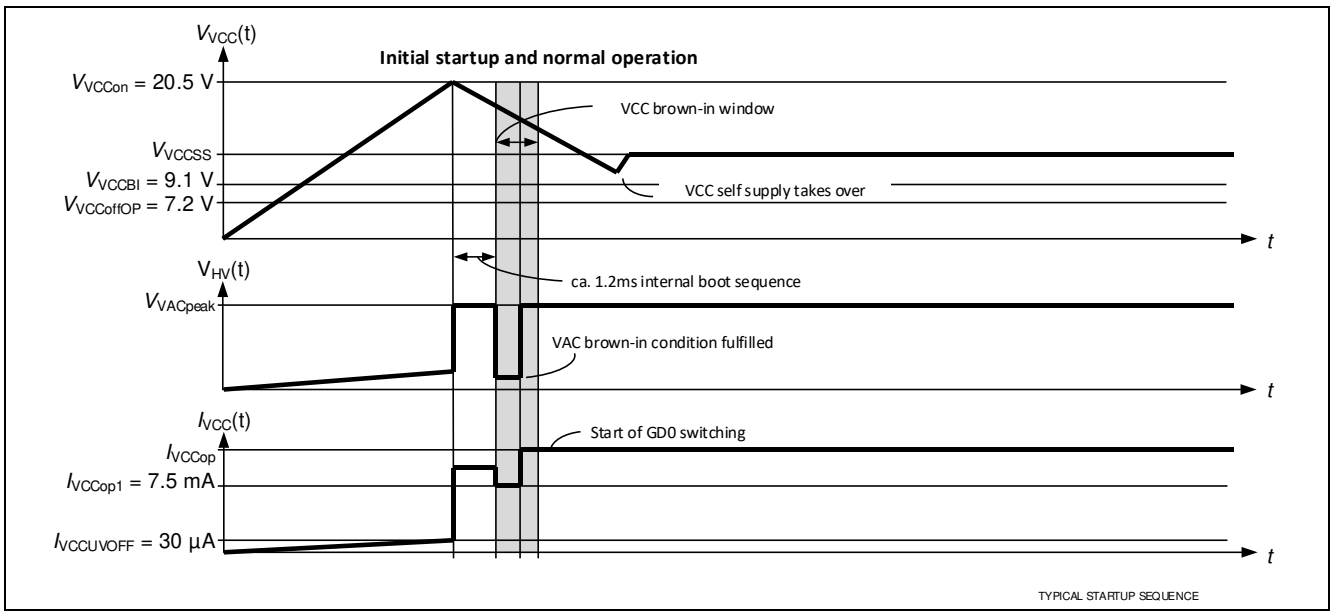

Figure 4 Typical startup sequence

4.1.2 Brown-in monitoring

Once the IC is activated, brown-in monitoring is enabled for input brown-in protection (see Chapter 4.3.4) by measuring the current at HV pin through the internal shunt resistor R_M (see Chapter 4.2.2). If the input brown-in is not detected before VCC falls below V_{VCCBI}, the startup cell measurement unit remains enabled until VCC falls down to V_{VCCoff}.

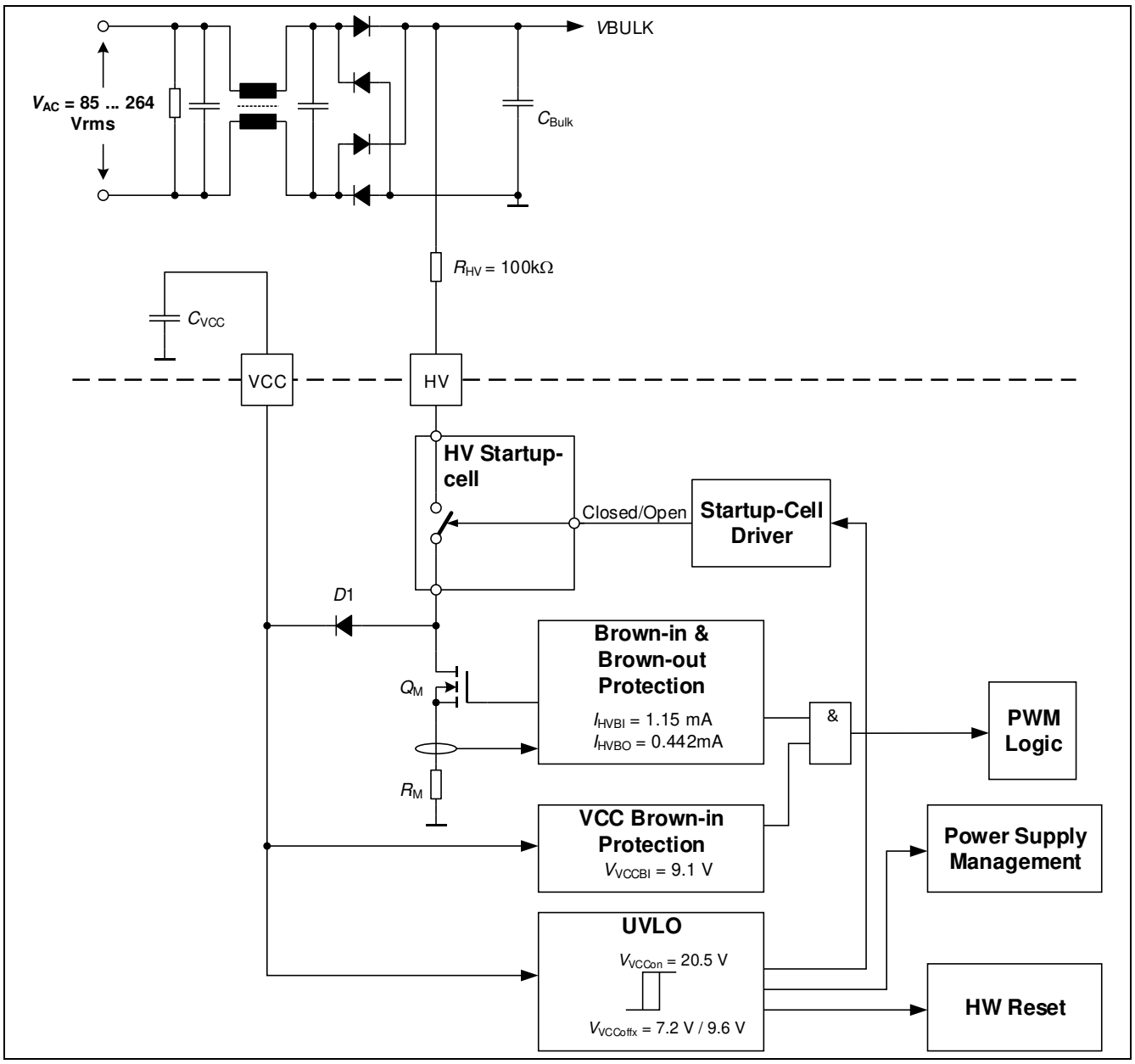

Figure 5 High voltage brown-in sensing and VCC startup at HV pin

4.1.3 Brown-out protection

In case of brown-out (see Chapter 4.3.5), the IC stops gate driver switching. Brown-out detection is also performed via the HV pin as for brown-in detection. Here an under-voltage detection of the bulk voltage V_{Bulk} is provided to support brown-out protection. The measured current I_{HV} is compared with the bulk under-voltage detection threshold I_{HVBO} = 0.443 mA.

4.1.4 During burst mode operation

After the control IC enters quiet burst mode, the IC enters repeatedly a sleep mode, in which the IC current consumption is reduced to $I_{VCCquBM2}$ = 460 µA. Waking up from and entering this sleep mode (pause) is controlled by the feedback voltage at MFIO pin V_{MFIO} via the internal comparators C5 and C6 (see Figure 6 and Chapter 4.2.910).

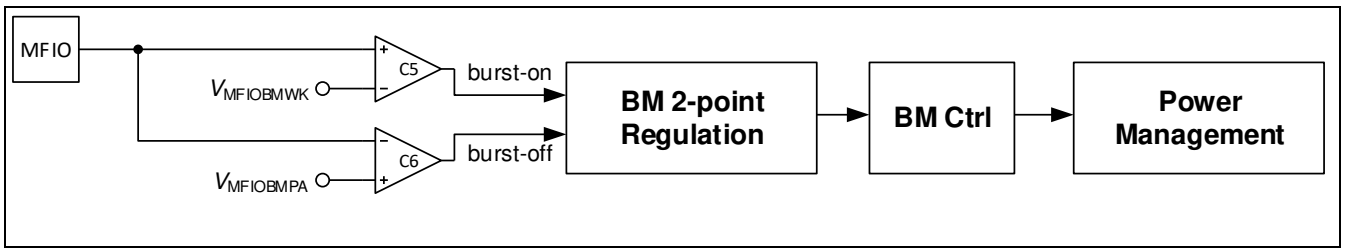

Figure 6 Burst mode control

For the system dimensioning, it should be ensured that the voltage V_{VCC} should be always well above the threshold V_{VCCoff}, including the burst-off phase. Figure 7 shows a typical burst mode operation signal for VCC and correlated current consumption.

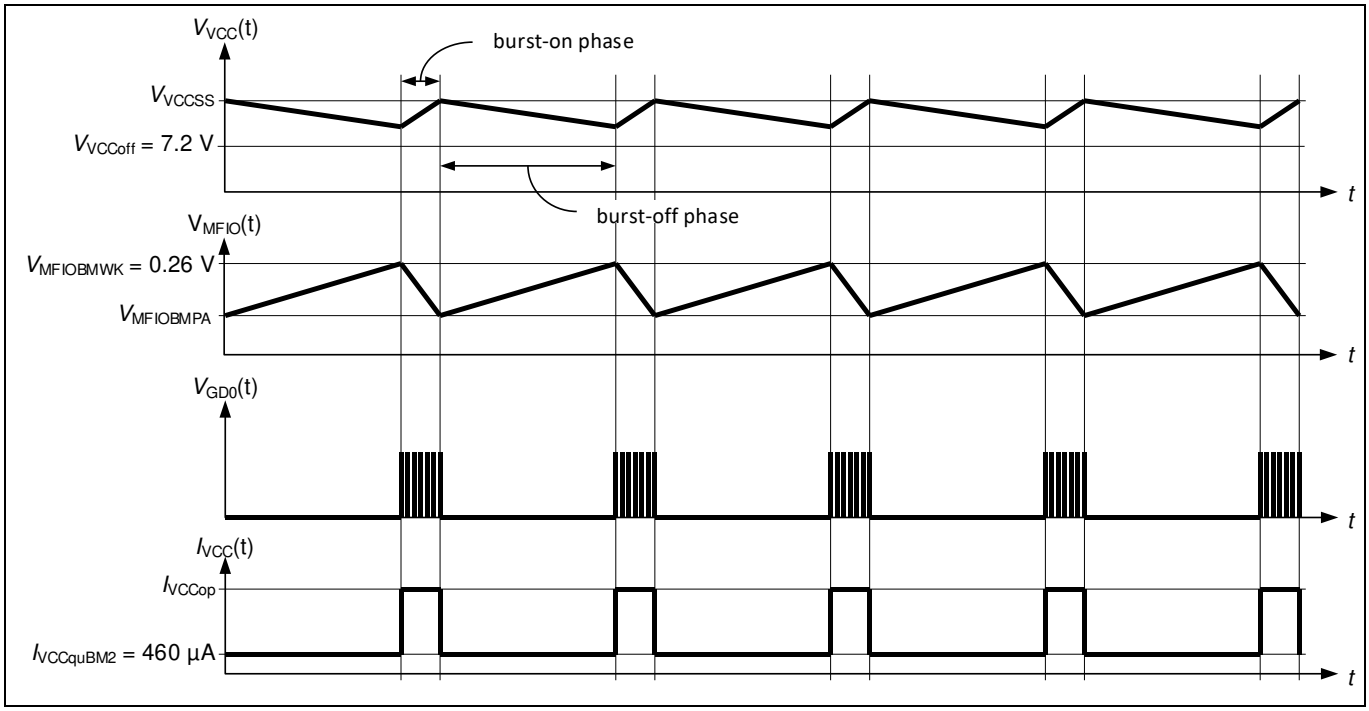

Figure 7 Burst operation

4.1.5 Bang-bang mode during latched and auto-restart operation

The bang-bang mode supports an IC operation without external VCC supply during the latched and auto-restart operation. It directly controls the HV startup cell depending on the set bang-bang mode turn-on threshold $V_{VCCBBon}$ of the corresponding auto-restart and latch mode (see Figure 8). In latch mode, the HV startup cell switch-on threshold is set to $V_{VCCBBon}$ = 9 V (see Chapter 4.1.5.1 and Chapter 4.1.5.2). In auto-restart mode, there is also an additional stand-by timer active that switches on the HV startup cell in a fixed time period of 500ms scheme to keep the VCC all the time at a high level above the brown-in threshold V_{VCCBI} = 9.1 V. Then a restart can take place without going through an additional VCC brown-in cycle. Due to the low current consumption during the auto-restart break time, the startup cell is always turned on by the 500 ms timer.

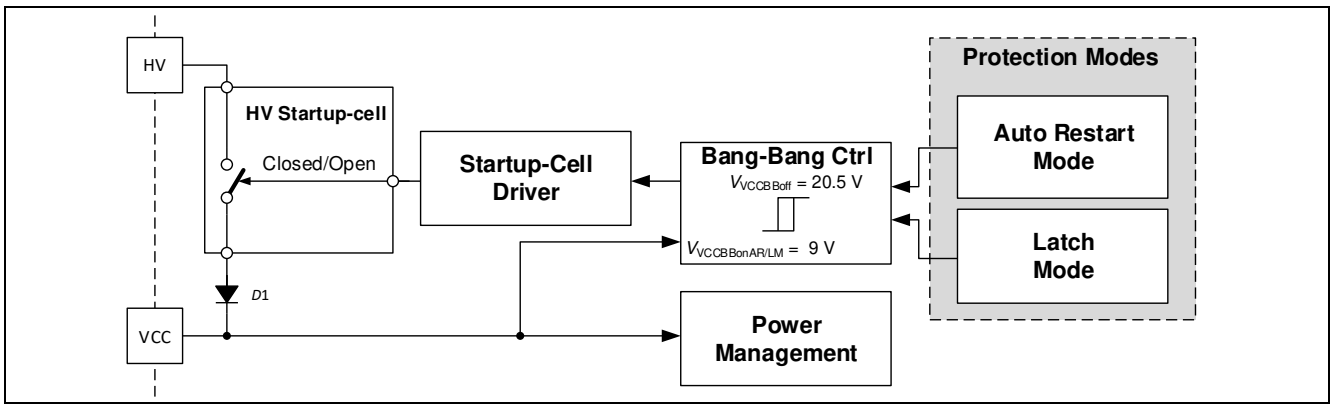

Figure 8 Bang-bang mode control of HV startup-cell

4.1.5.1 During latched operation

If latch mode is entered (see Chapter 4.3.2), the IC stops gate switching and the VCC current consumption is reduced to $I_{VCCquLM}$ = 150 µA. The enabled bang-bang mode ensures that the IC is kept alive by keeping the voltage at VCC pin above the threshold V_{VCCoff} = 7.2 V (see Figure 9). A reset of the latch mode takes place only after the VCC drops below the V_{VCCoff} threshold.

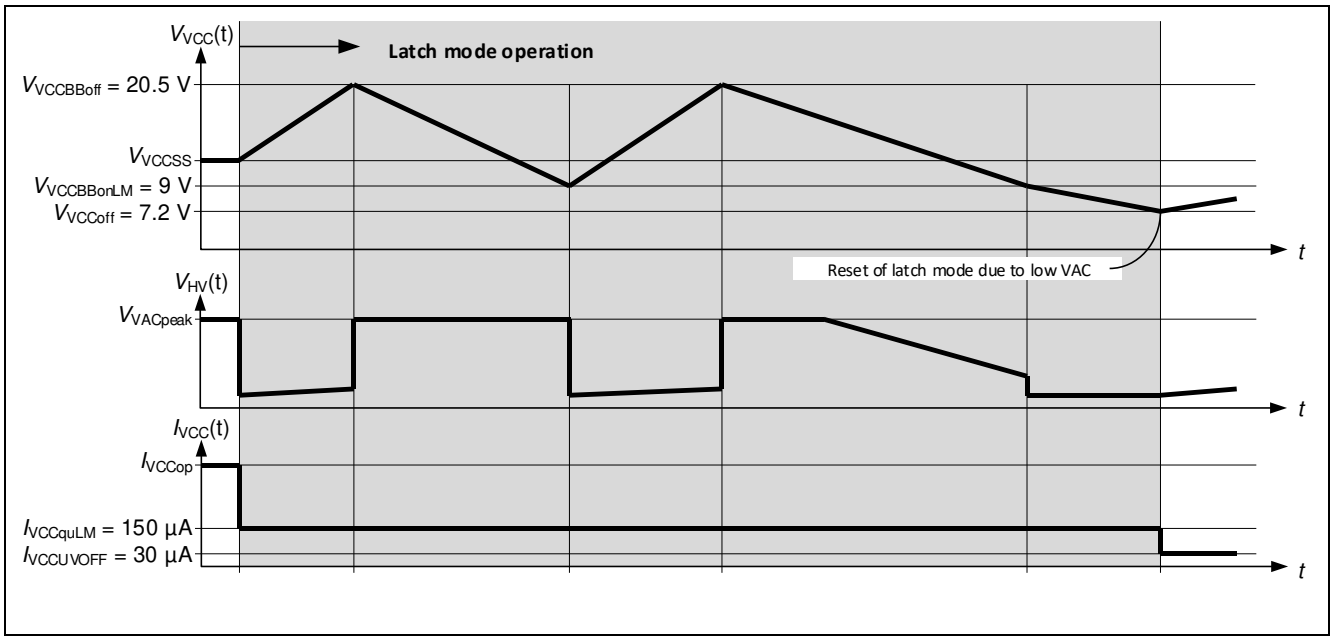

Figure 9 Latch mode operation

4.1.5.2 During auto-restart operation

Once auto-restart mode is entered (see Chapter 4.3.1), the IC stops GD0 switching, the VCC current consumption is reduced to $I_{VCCquAR}$ = 160 µA, and a stand-by timer with 500 ms ($t_{BBoffAR}$) period is activated which turns on the HV startup cell periodically, to charge up the VCC capacitor. Once the voltage at VCC pin exceeds the switch-off threshold $V_{VCCBBoff}$ = 20.5 V, the startup cell is turned off (see Figure 10). This is bang-bang mode operation for the VCC management during the auto-restart break time. In this way, the VCC voltage is kept at a level well above the VCC brown-in threshold to ensure enough energy stored in the VCC capacitor for the coming restart of the system, that is initiated after the auto-restart break time t_{AR} = 3 s. Then after an additional time Δt = ε, the gate driver switching is activated with a soft-start sequence. Here the additional time ε depends on the VCC capacitor charge-up time which is related to the VCC capacitance and the voltage at HV pin.

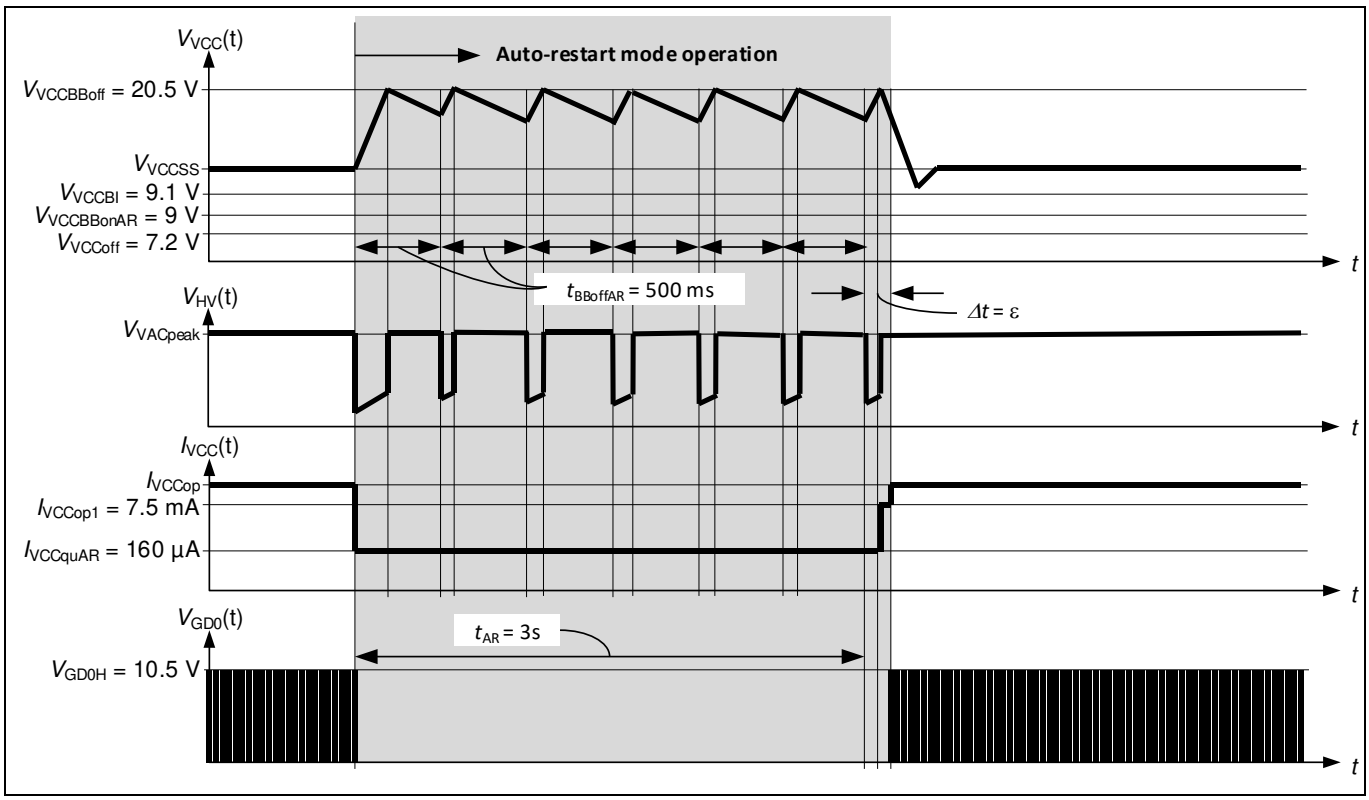

Figure 10 Auto-restart mode operation

4.2 Control features

The XDPS21081 provides peak current control assisted by the features listed in Table 2. A simplified block diagram representing the controller features is shown in Figure 11.

Functional Description

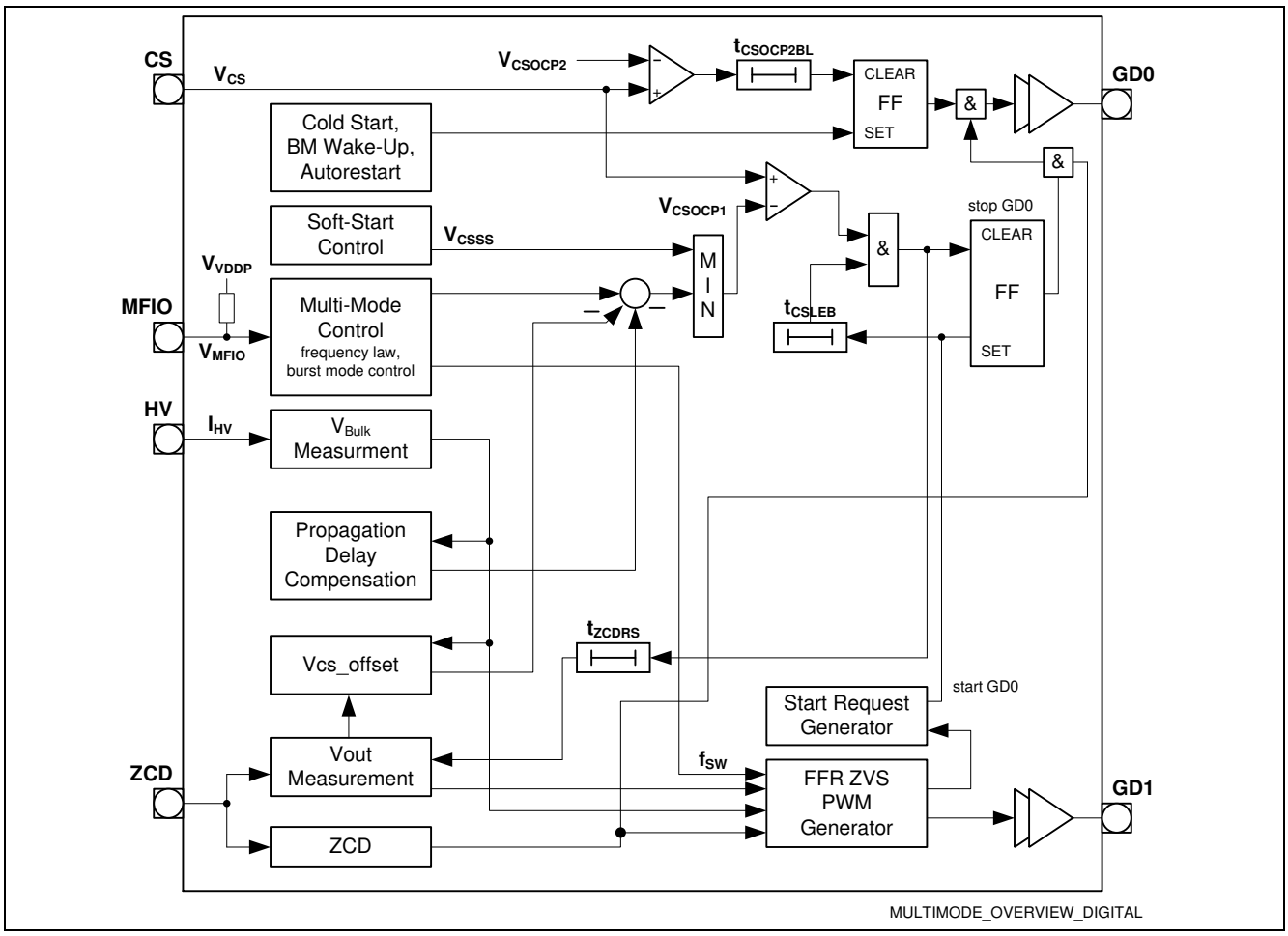

Figure 11 Block Diagram of PWM Control

Table 2 gives an overview about the controller features that are described in the mentioned chapters.

Table 2 Controller Features

Reflected voltage sensing and zero crossing detection at auxiliary winding	Chapter 4.2.1
Vbulk voltage measurement via HV startup cell	Chapter 4.2.2
Propagation delay compensation (PDC)	Chapter 4.2.3
Soft-start	Chapter 4.2.4
Leading edge blanking (LEB) time at CS pin	Chapter 4.2.5
Spike blanking at CS pin for 2nd level over-current detection	Chapter 4.2.6
Gate driver output GD0 and GD1	Chapter 4.2.7
Multi-mode operation	Chapter 4.2.8
Burst mode (QBM) operation	Chapter 4.2.10
Forced quasi resonant mode	Chapter 4.2.11
Forced quasi resonant ZVS mode operation	Chapter 4.2.12
UART function at GPIO pin	Chapter 4.2.13

4.2.1 Reflected voltage sensing and V_{CS} offset calculation based on output voltage

The IC provides output voltage detection by means of measuring the reflected voltage at the auxiliary winding V_{Aux} at the primary side of the transformer via ZCD pin and an external resistive voltage divider. The voltage signal V_{Aux} contains the information of the flyback output voltage, V_{Out}, at the secondary side.

The ZCD pin related circuit is shown in Figure 12. Figure 13 shows a typical voltage waveform of the drain voltage V_{Drain} and the related auxiliary winding voltage V_{Aux}. The sensed output voltage is used for over-voltage protection (see Chapter 4.3.11).

Following topics are described in the sequel:

- Output voltage sensing via ZCD pin (Chapter 4.2.1.1)
- Vcs offset with sensed Vo at ZCD pin (Chapter 4.2.1.3)

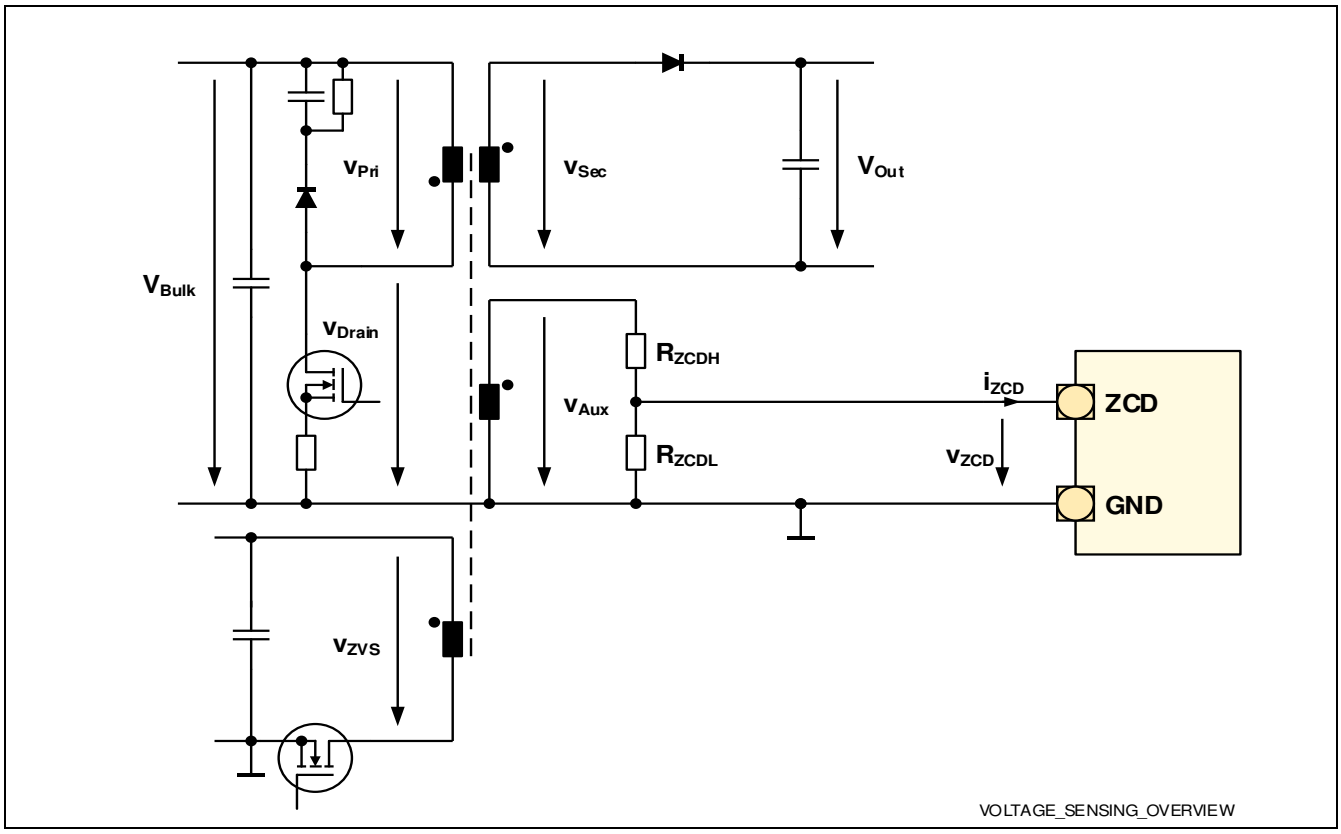

Figure 12 Functionality at ZCD pin

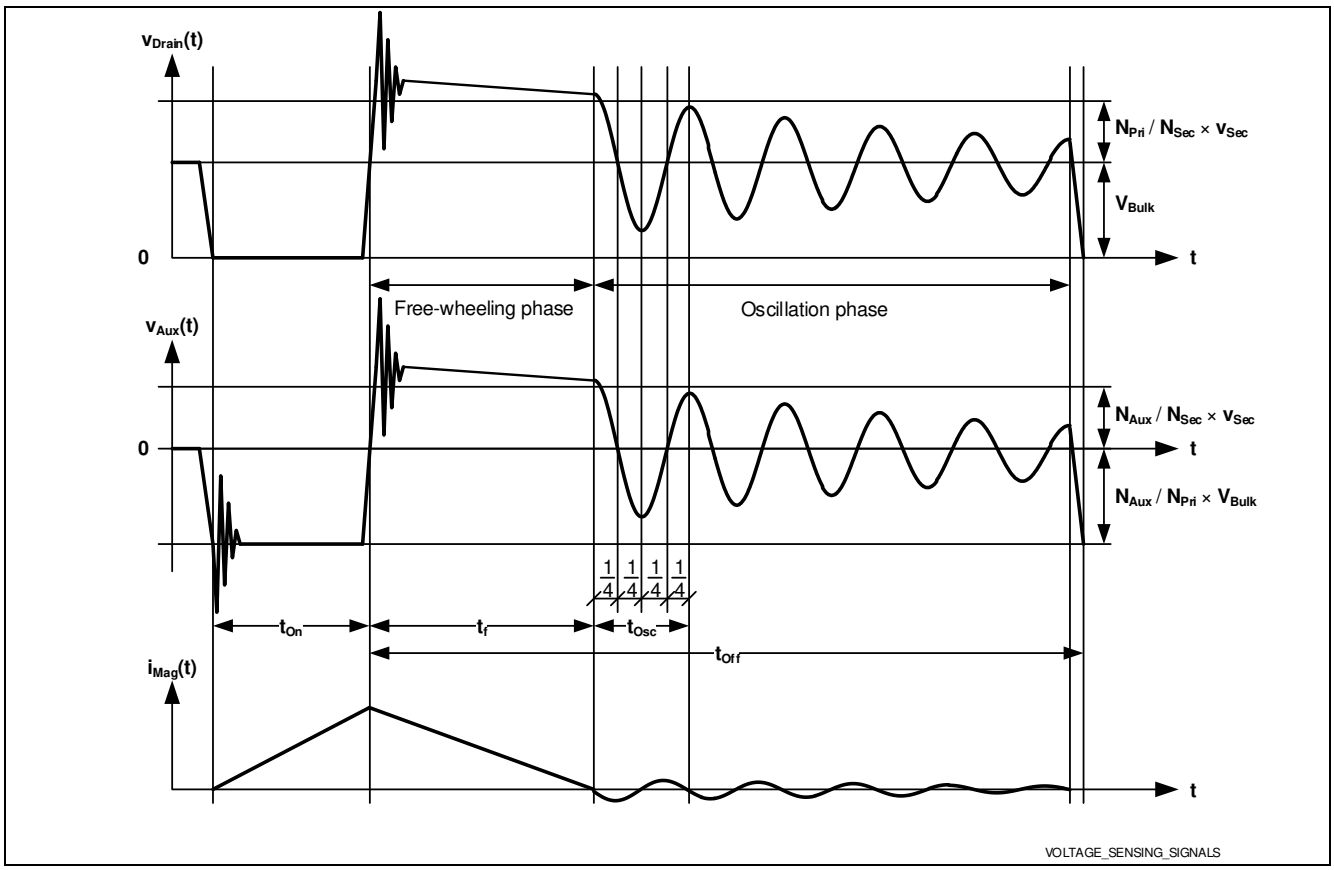

Figure 13 Auxiliary voltage and magnetization current waveforms for standard discontinuous conduction mode operation

4.2.1.1 Output voltage sensing via ZCD pin

Output voltage is sensed at a fixed point of time during the free-wheeling phase. The free-wheeling phase begins when the gate driver is switched off and ends when the secondary side demagnetization current becomes zero. During free-wheeling phase the VCC capacitor of the IC, the output stage and the additional ZVS capacitor at ZVS winding for introducing a forced resonant cycle (see Chapter 4.2.12) are supplied. As soon as VCC capacitor is charged, the auxiliary voltage is a function of secondary side voltage.

$$V_{AUX} = \frac{N_{AUX}}{N_{Sec}} \cdot V_{Sec} \quad (1)$$

Figure 14 shows the schematic related to secondary side voltage sensing and the equivalent network.

Functional Description

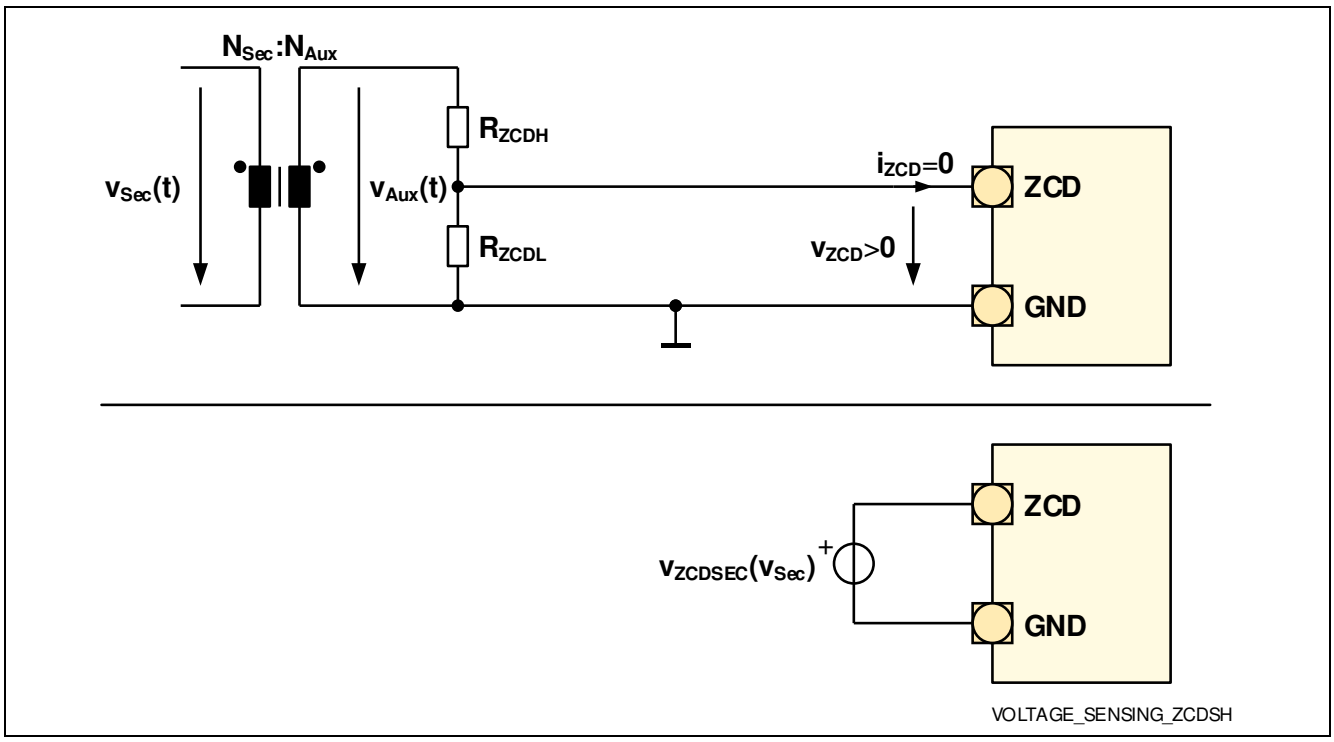

Figure 14 Secondary Side Voltage Sensing

No current clamping applies during the free-wheeling time and the voltage at ZCD pin is given by

$$V_{ZCDSEC}(V_{Sec}) = R_{ZCD} \cdot \left(\frac{V_{AUX}}{R_{ZCDH}}\right) \quad (2)$$

R_{ZCD} is the internal resistance of V_{ZCDSEC} (V_{Sec}) and is the equivalent parallel resistance of R_{ZCDH} and R_{ZCDL}. The related waveforms are presented in Figure 15. After the primary side gate driver is turned off, the auxiliary voltage goes from its negative level to positive. After a ringing phase, the positive level is given by the output voltage plus the secondary side diode voltage drop. During the free-wheeling phase the secondary side diode operates in the linear region until the demagnetization current becomes very small. This linear relationship can be described as a resistor $R_{DSonSec}$, resulting in a falling slope according to $R_{DSonSec} \cdot i_{LSec}(t)$. The secondary side current $i_{LSec}(t)$ decreases with a slope given by the output voltage and the transformer secondary side inductance. Hence the resulting auxiliary winding voltage is more or less constant until the secondary side current becomes zero. The reflected voltage at auxiliary winding is sampled at the end of the ringing suppression time (see Chapter 4.2.1.2). The measured voltage V_{ZCDSEC} includes the output voltage level and a superimposed offset $\Delta V_{ZCDOFFSET}$ that is depending on the secondary side chosen rectification approach and the associated component dimensioning.

To ensure an accurate measurement of the reflected output voltage, the system dimensioning must provide a free-wheeling phase that only finishes after the ringing suppression time t_{ZCDRS}.

Furthermore following effects can influence the output voltage sensing if not properly considered in system dimensioning:

- VCC and ZVS capacitor charging
- Voltage drop on secondary side at the free-wheeling diode or the secondary side switch

The VCC and ZVS capacitors need to be charged up before the ringing suppression time t_{ZCDRS} ends. The superimposed voltage offset $\Delta V_{ZCDOFFSET}$ at sample time point due to secondary side rectification approach needs to be considered either by the dimensioning of the ZCD resistor divider or the internal overvoltage threshold setting V_{ZCDOVP} (see Chapter 4.3.11).

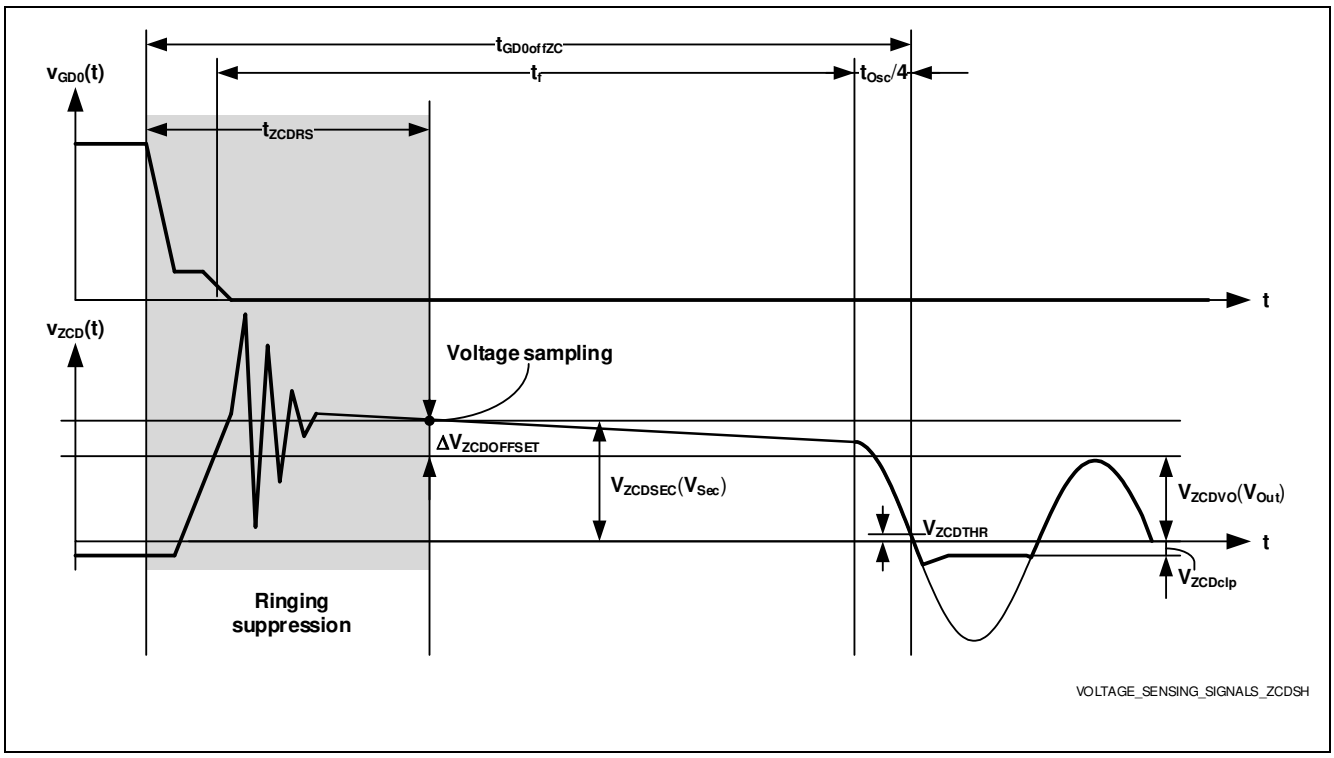

Figure 15 Output Voltage Sensing Signals

4.2.1.2 Ringing suppression time

To prevent erroneous ZCD events due to primary side gate driver turn off ringing, a ringing suppression time t_{ZCDRS} = 0.6µs applies for the zero-crossing events. During this time no zero-crossing is considered.

4.2.1.3 Vcs offset calculation based on output voltage sensed at ZCD pin

To limit the output current at different output voltage, a linear scaled V_{cs} offset is inserted to the peak current command. This offset will be minused from the current command mapping from the frequency law curve.

It is an inverse of the output voltage based on positive ZCD winding voltage. Figure 16 shows when the V_{zcd} is at V_{zcd}_zero_point, the V_{cs} offset is zero. While Vzcd voltage is at minimum level, the V_{cs} offset is maximum. The V_{cs} offset level depends on the slew rate of K_{vcs_offset} and the starting point of V_{zcd}. The equation is as below:

$$Vcs_{offset} = Kvcs_{offset} * (Vzcd - Vzcd\_zero\_point)/65536 \quad (3)$$

All the number in above equation is decimal digital value.

At ZCD pin, the sensed voltage will minus 1.2V offset first, then feed into an ADC channel to get the sense the voltage. Also due to the ADC input voltage range is 1.2-2.8V, so any ZCD voltage out of this range is ignored by the IC and ADC converter value will be saturated at its min(0) and max value(255).

Below is the example on how to set the value,

$V_{zcd\_zero\_point}$ is the voltage level without compensation, here we choose V_{zcd}=1.69V, the digital value of $V_{zcd\_zero\_point\_dig}$=(1.69-1.2)*1.5/2.4*256=79, $K_{vcsoffset}$=20000, for V_{zcd}=1.2V, the digital value of it will be

V_{zcd_dig}=(1.2-1.2)*1.5/2.4*256=0, so $V_{csoffset\_dig}$=20000*(0-79)/65536=24, its analog value will be 24/256*400=38mV.

If system parameters like transformer turns ratio, ZCD pin voltage divider is known, then the corresponding output voltage can be calculated. E.g. N_{aux}=2, N_{sec}=2, R_{zcdH} is 39kohm, R_{zcdL} is 5.6kohm.

$$V_o = V_{zcd} * \frac{N_{sec}}{N_{aux}} * (R_{zcdL} + R_{zcdH})/R_{zcdL} \quad (4)$$

Functional Description

So for V_{zcd}=1.69V, V_o will be 1.69*2/2*(39+5.6)/5.6=13.46V assuming transformer coupling is 1.

For V_{zcd}=1.2V, V_o will be 1.2*2/2*(39+5.6)/5.6=9.56V.

This means that when output voltage is above 13.46V, there is no V_{cs} offset compensation, below 9.56V the compensation is clamped at 38mV as calculated above.

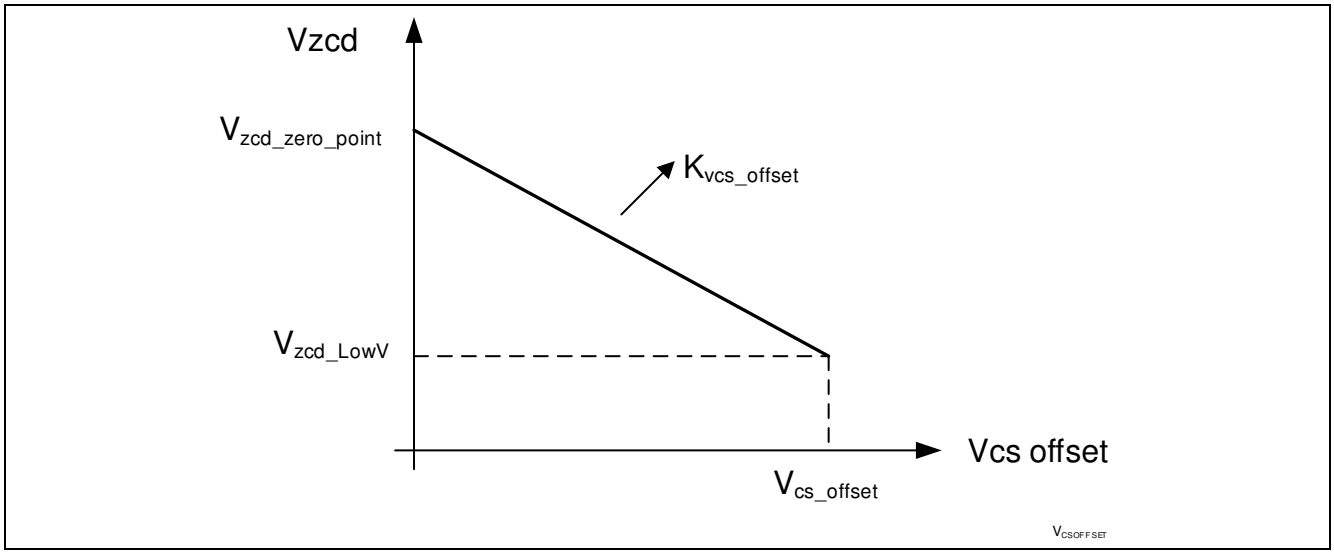

Figure 16 V_{cs_offset} calculation

4.2.2 Vbulk voltage measurement via HV startup cell

The V_{Bulk} voltage is measured via the HV pin that is connected at the bulk capacitor node. The current I_{HV} is sampled in the IC and processed for the following functions:

- Brown-in protection (Chapter 4.3.4)
- Brown-out protection (Chapter 4.3.5),
- Propagation delay compensation (Chapter 4.2.3),

In all these functions, the current I_{HV} represents the bulk voltage.

4.2.3 Propagation delay compensation (PDC)

Due to the gate driver turn-off propagation delay t_{PD}, the level V_{CSOCP1} set by the OCP1 comparator will not directly control the inductor peak current, I_{LPk}.

Without propagation delay, the peak current would be given by $I_{LPk} = R_{CS}^{-1} \cdot V_{CSOCP1}$. However, due to the propagation delay, the OCP1 level is exceeded by

$$R_{CS} \cdot I_{Lpk} = V_{CSOCP1} + V_{CSPD}(V_{Bulk}) \quad (5)$$

Where the propagation delay overshoot $V_{CSPD}(V_{Bulk})$ is

$$V_{CSPD}(V_{Bulk}) = \frac{R_{CS}}{L_{Pri}} \cdot t_{PD} \cdot V_{Bulk} \quad (6)$$

In Figure 17 related example waveforms are presented.

Functional Description

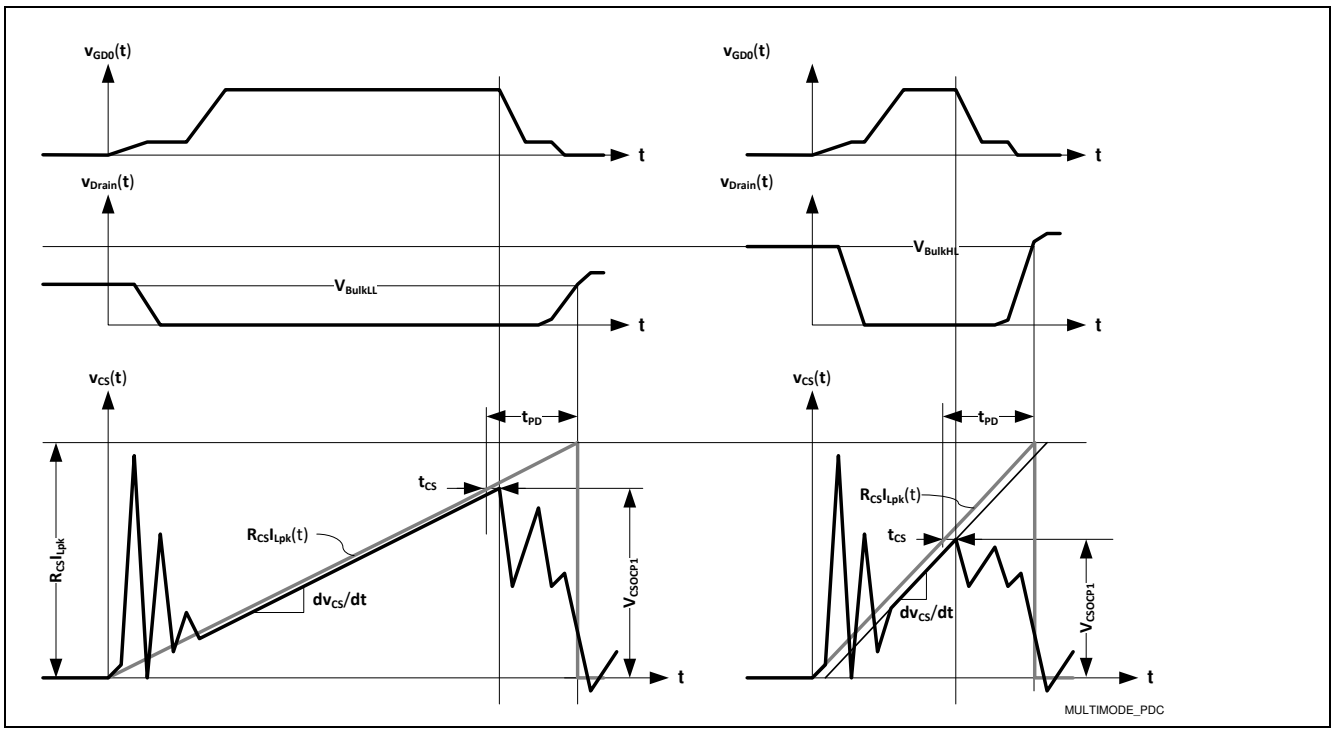

Figure 17 Propagation Delay and Propagation Delay Compensation

On the left side, the bulk voltage is low, the slope of inductor current and of the CS voltage are low, too. When the CS voltage reaches the OCP1 level, the gate driver turns off and the inductor current reaches its peak after the turn off propagation delay t_{PD}. The turn off propagation delay t_{PD} includes the delay t_{CS} of the filter capacitor connected to CS pin and the resistor connected between shunt resistor and CS pin (see Typical Application Figure). The overshoot of the inductor current due to propagation delay is small due to the small slope

$$\frac{dV_{CS}}{dt} = \frac{R_{CS} \cdot V_{Bulk}}{L_p} \quad (7)$$

The right side of Figure 17 shows the same operating waveforms for a higher bulk voltage. In this case, the OCP1 comparator limit needs to be less than on the left side to reach the same inductor peak current. Although the propagation delay remains the same, the slope as well as the overshoot due to propagation delay is larger.

The XDPS21081 controller is defined to measure the HV current I_{HV} representing the bulk voltage V_{Bulk}. The OCP1 comparator limit is adjusted depending on the measured bulk voltage so that the real peak current due to the propagation delay is compensated. For this HV pin needs to be connected to V_{Bulk}.

Consequently, any CS peak parameter V_{CSx} is specified in the electrical characteristics (Chapter 6.5) for a low-line use case (V_{CSxLL}) and for a high-line use case (V_{CSxHL}).

Low-Line Use Case (LL)

- I_{HVLL} = 70 µA as for V_{Bulk} = 72 V, R_{HV} = 100 kΩ
- $(dv_{CS}/dt)_{LL}$ = 49 mV/µs as for V_{Bulk} = 72 V, L_{Pri} = 200 µH, R_{CS} = 0.135 Ω

High-Line Use Case (HL)

- I_{HVHL} = 370 µA as for V_{Bulk} = 372 V, R_{HV} = 100 kΩ
- $(dv_{CS}/dt)_{HL}$ = 251 mV/µs as for V_{Bulk} = 372 V, L_{Pri} = 200 µH, R_{CS} = 0.135 Ω

These use cases set the corners of the propagation delay compensation which operates in a linear manner so that the typical OCP1 threshold for any I_{HV} is given by

$$\frac{V_{CSx}(I_{HV}) - V_{CSxLL}}{I_{HV} - I_{HVLL}} = \frac{V_{CSxHL} - V_{CSxLL}}{I_{HVHL} - I_{HVLL}} \quad (8)$$

4.2.4 Soft-start

The IC control provides a soft-start during initial startup and auto-restart cycles. The soft-start slew rate is defined by the step ΔV_{CSS} = 1.7 mV taking place every time step of t_{Base1} = 52.14 µs. Furthermore, the peak current start level is determined by the parameter V_{CSSS}.

The soft-start phase is latest finished after V_{CS} has ramped up to the maximum level of V_{CSmax} (see Figure 18).

The total soft-start time t_{SSmax} is therefore based on the following equation:

$$t_{SSmax} = t_{Base1} \cdot \frac{V_{CSmax} - V_{CSSS}}{\Delta V_{CSS}} \quad (9)$$

The associated ramped up peak current limitation is determined by internal digital numbers, which are not depending on the propagation delay during peak current limitation process.

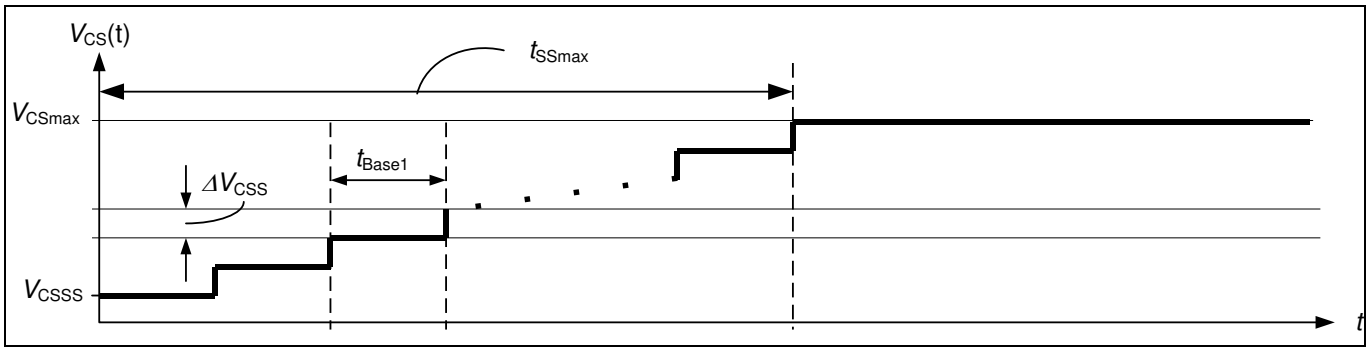

Figure 18 Soft-start timing

The internal soft-start phase is finished once the voltage level at MFIO pin is getting lower than 2.42 V. Then the setting for CS limitation is determined by the feedback signal at MFIO pin via the frequency law (see Chapter 4.2.8.1).

4.2.5 Leading edge blanking (LEB) at CS pin

A digital leading edge blanking filter with t_{CSLEB} = 269 ns (see Chapter 5) is integrated in the OCP1 peak current control path to prevent the current limitation process from distortions, caused by the leading edge spike at the switch-on of the power MOSFET (see Figure 19). The LEB applies only for the OCP1 comparator (see Figure 3) that is used for cycle-by-cycle peak current limitation. The LEB needs also to ensure a monotonous peak current control without being impacted by ringing taking place directly after the leading edge spike.

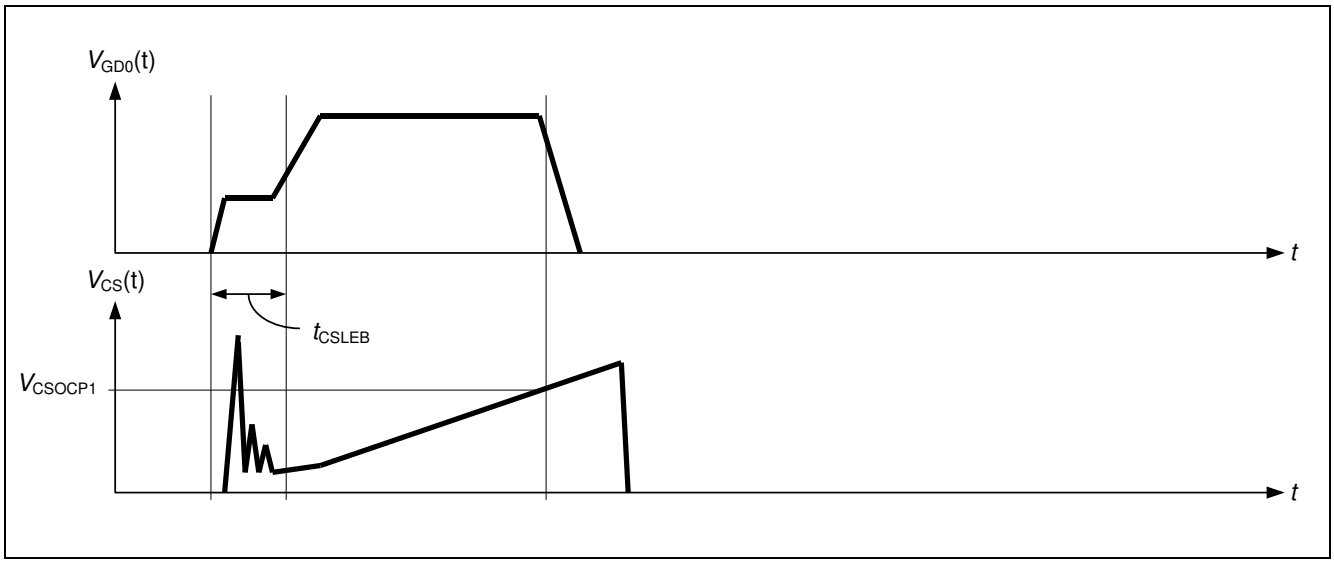

Figure 19 Leading edge blanking

4.2.6 Spike blanking at CS pin for 2nd level over-current detection (OCP2)

A further comparator OCP2 is implemented at CS pin (see Figure 3) to detect dangerous current levels (see Chapter 5), which could occur if one or more transformer windings are shorted or if the secondary side diode is shorted. To avoid an accidental trigger by exceeding this 2nd level over-current protection threshold V_{CSOCP2} = 0.6 V, a spike blanking time $t_{CSOCP2BL}$ = 616.2 ns (see Chapter 5) is implemented in the output path of the OCP2 comparator.

4.2.7 Gate driver output GD0 and GD1

The gate driver GD0 and GD1 are of the same type. The GD0 is used for controlling the main MOSFET connected to the primary main inductance of the flyback transformer. The GD1 is used for controlling the FQR ZVS mode (see Chapter 4.2.8) by driving the dedicated MOSFET that is connected to the ZVS winding at the flyback transformer.

The gate driver output stages consist of a regulated current source connected to VCC pin and a MOSFET switch connected to GND (see Figure 20 and Figure 21). The peak source current at GDx is set to $I_{GDxHPKSRC}$ = -35 mA. The MOSFET switch provides a discharge path for the main power MOSFET with a sink capability of $R_{GDxLSNK} \leqslant 6.5\ \Omega$.

The controlled source current determines together with the gate-source capacitance C_{GS} and the gate-drain capacitance C_{GD} of the external power MOSFET the rising slope during turn-on phase (see Figure 22). The gate driver state control ensures that the charged gate driver output voltage is clamped at the level V_{GDxH} = 10.5 V.

The external gate resistor R_{GDx} is therefore only meant for adjusting the peak sink current and the corresponding gate voltage falling slope during the turn-off phase. Here the turn-on behavior is mainly dominated by the controlled limited current source $I_{GDxHPKSRC}$ as the size of the external gate resistor is mainly limiting the higher peak sink current at GDx pin. When dimensioning the serial gate resistor R_{GDx}, also a minimum load capacitance needs to be considered after R_{GDx} (see Chapter 9.1), which needs to be provided by the corresponding gate-source capacitance C_{GS} of the external power MOSFET. This ensures a smooth and stable settling of the voltage level V_{GDxH} at the end of the turn-on phase.

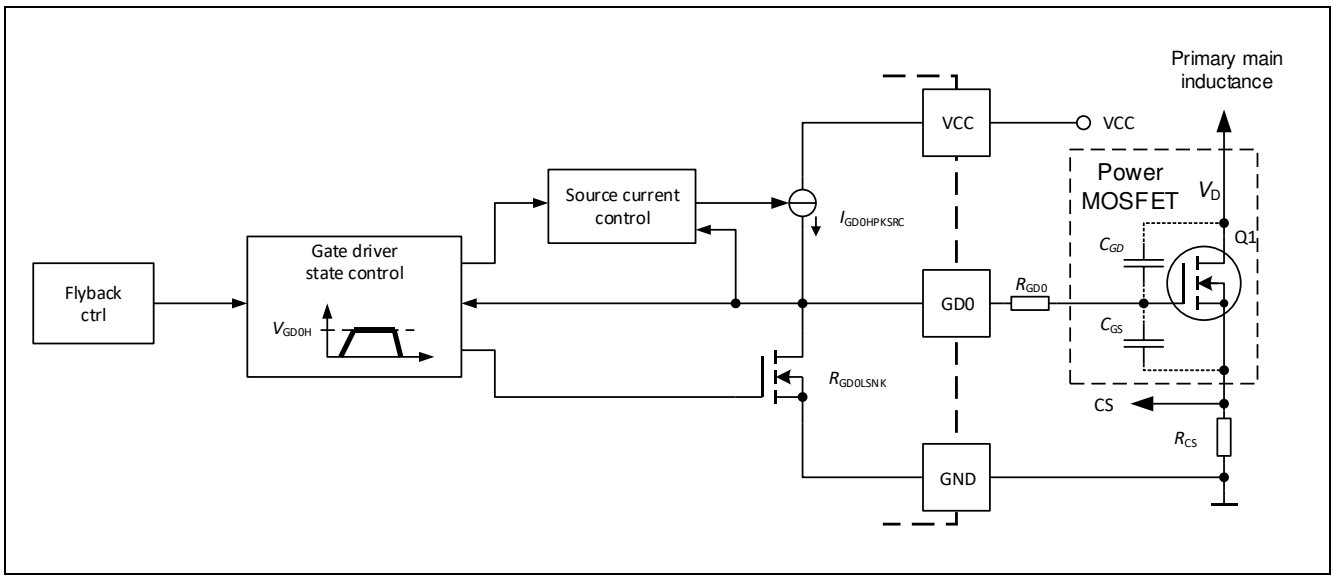

Figure 20 GD0 output stage structure

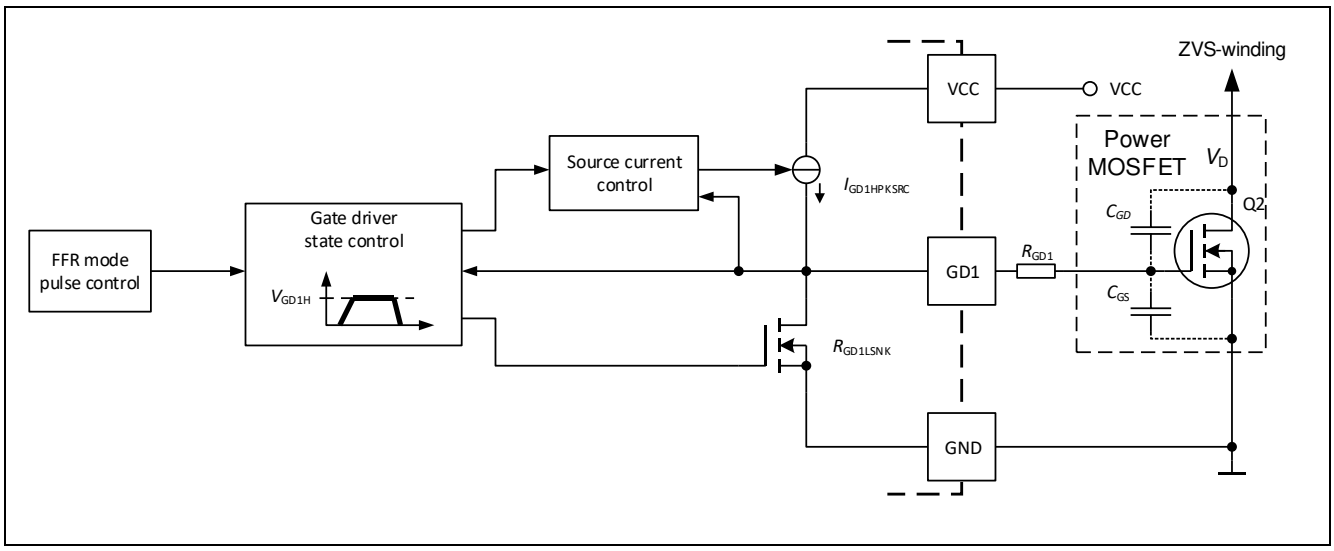

Figure 21 GD1 output stage structure

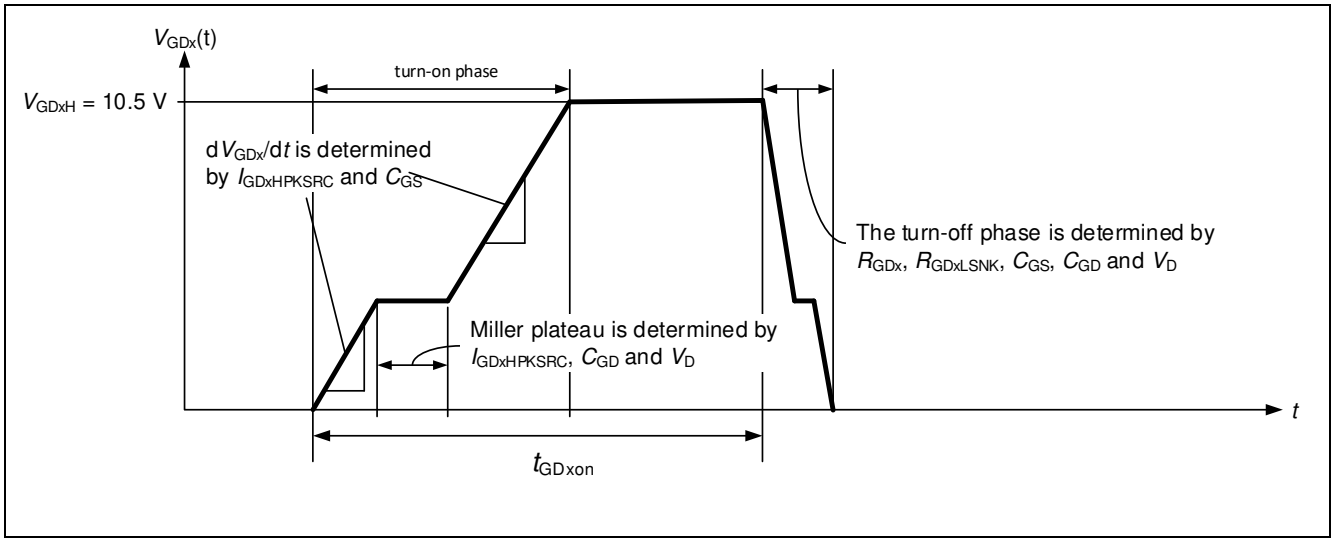

Figure 22 Gate drive output

4.2.8 Multi-mode operation

The multi-mode operation consists of two different operation modes that are controlled by the feedback voltage signal at MFIO pin (see Table 3).

Table 3 Overview multi-modes

Symbol	Operation Mode	Description
BM	Burst mode	Chapter 4.2.10
QRM	Quasi resonant mode at low line	Chapter 4.2.11
FQRZVSM	Forced quasi resonant ZVS mode during BM and DCMx operation at high line	Chapter 4.2.12

The configurable multi-mode operation depends on the inductance design, switching frequency, load condition and the bulk voltage V_{Bulk}. It is characterized by the frequency scheme and peak current correlation shown in Figure 23. The peak current limit V_{CSPK} (y-axis) and the frequency limits are set according to the input signal at MFIO pin. The peak current limits for V_{CSPK} are shown for the low and high-line use case (see Chapter 4.2.3), which consider the propagation delay

Functional Description

compensation (PDC). The border for entering the burst mode (BM) is determined by the setpoint D. The actual peak current and the actual switching frequency areas follow:

- In DCM1 and DCM2 operation, the peak current and the switching frequency are directly given by the curve F-E-D.
- In DCM1 the peak current changes with the voltage V_{MFIO} and the switching frequency is fixed.
- In DCM2 the peak current is fixed, and the switching frequency changes with V_{MFIO}.
- During QRM, the peak current changes with the voltage V_{MFIO} and the switching frequency limited by the curve A-B-C-D.
- the multi-mode controller selects the operating mode (BM, DCM1, DCM2, QRM / FQRZVS)

The following Figure 23 shows an example of using all possible multi-mode operation phases that are determined by the corresponding setpoints A, B, C, D, E and F. The specific frequency law setting for XDPS21081 based on the FW: REV 1.0 is shown in Chapter 4.2.8.1.

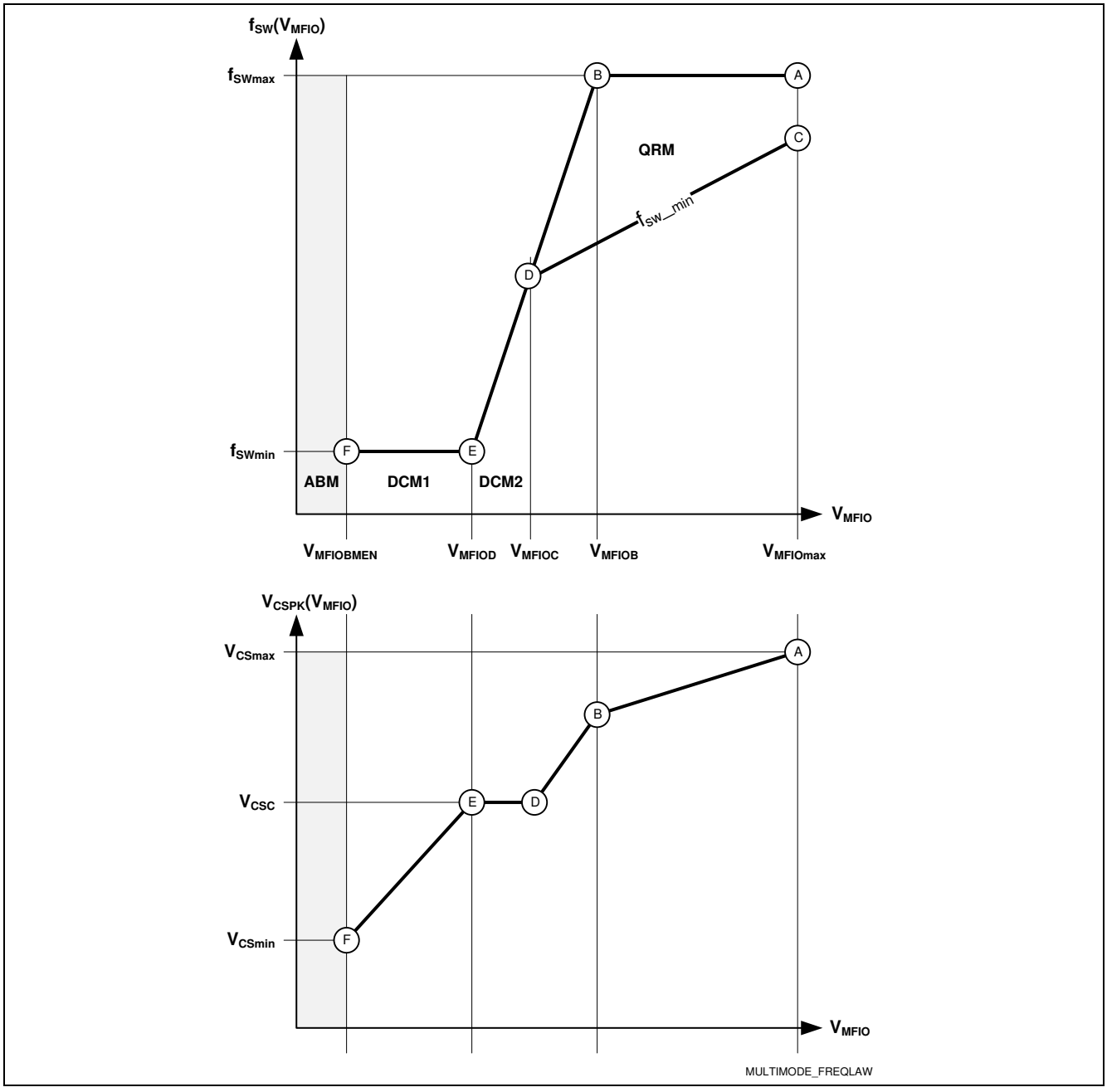

Figure 23 Configurable frequency law and peak current schemes depending on signal at MFIO pin

4.2.8.1 Frequency law setting for XDPS21081

The frequency law setting for XDPS21081 based on the is defined by the set point A, B, C ,D,E and F as shown in Table 4.

Table 4 Corner points for frequency limitation curve and peak current setting for XDPS21081

Assuming LL (low line) =72V, HL (high line) =372V, L_{PRI}=200uH, R_{CS}=0.135 Ω

Setpoint	
A	Corner point for maximum current
	V_{MFIOA} = 2.30V f_{SWmax} = 145 kHz $V_{CSmaxLL}$ = 402mV $V_{CSmaxHL}$ = 368mV
B	Corner point for border between DCM3 and DCM2 for frequency reduction
	V_{MFIOB} = 1.61V f_{SWB} = 145 kHz V_{CSBLL} = 336 mV V_{CSBHL} = 303mV
C	Corner point for border between DCM2 and DCM1 for fixed frequency and peak current reduction
	V_{MFIOC} = 2.30V f_{SWC} = 120 kHz V_{CSCLL} = 402mV V_{CSCHL} = 368mV
D	Corner point at minimum frequency setting
	V_{MFIOD} = 1.23V f_{SWD} = 83.7 kHz V_{CSDLL} = 260mV $V_{CSminHL}$ = 227mV
E	Corner point at minimum frequency setting
	V_{MFIOE} = 0.86 V f_{SWE} = 23 kHz V_{CSELL} = 260mV $V_{CSminHL}$ = 227mV
F	Corner point at minimum frequency setting
	V_{MFIOF} = 0.21V f_{SWmin} = 23 kHz $V_{CSminLL}$ = 67mV $V_{CSminHL}$ = 33mV

4.2.9 Peak current jittering

In order to improve the EMI performance, the XDPS21081 enables peak current jittering at middle to heavy load when Vmfio is larger than 1.0V and Input bulk voltage above 175Vdc (assuming R_{HV}=100K), and disable once

Functional Description

Vmfio is lower than 0.9V or input bulk voltage is lower than 150V (assuming R_{HV}=100K). The jitter of current will cause frequency jittering which improves the EMI spectrum signature.

Both the peak current amplitude and peak current period will jitter over time as shown in Figure24. The default jittering magnitude is ± 15.625mV and the jittering period is 1ms.

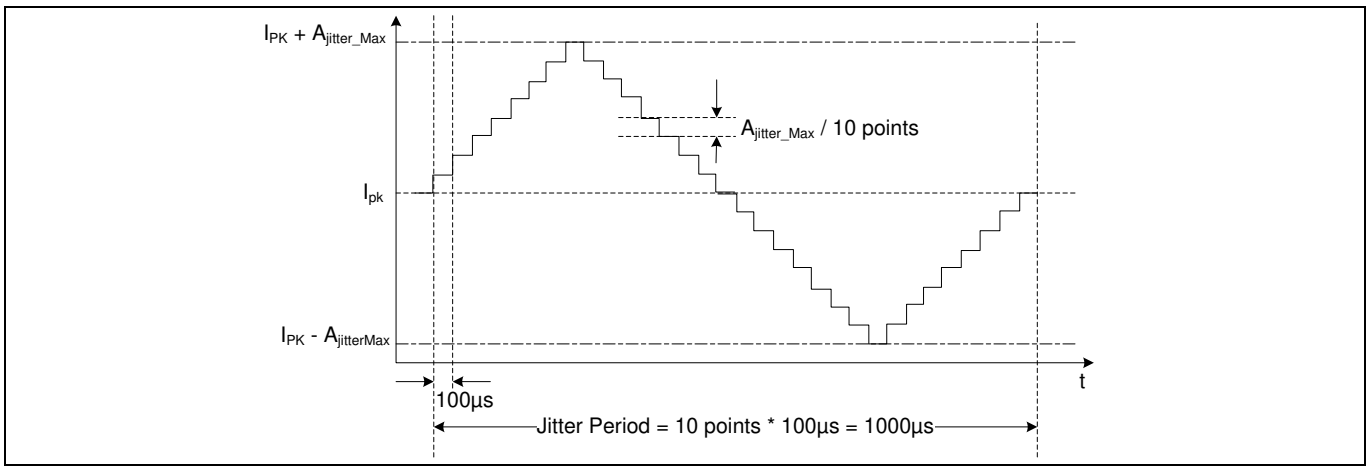

Figure 24 Jittering magnitude and period

Table 5 Peak current jitter parameters

Parameter Name	Physical value	Enable jitter condition	Disable jitter condition
$A_{\_Jitter\_max}$	15.625mV	Vbulk>=175Vdc and Vmfio>=1.0V, Assuming R_{HV}=100K	Vbulk<150Vdc or Vmfio<0.9V, Assuming R_{HV}=100K
$A_{\_Jitter\_period\_val}$	1ms		

4.2.10 Burst mode operation

The burst mode (BM) is entered at light load to optimize efficiency and correlated total power consumption. The BM consists of three main phases:

- Burst mode entry (see 4.2.10.1)
- Burst operation (see 4.2.10.2)
- Burst mode exit (see 4.2.10.3)

The burst mode control is described in the following chapters based on the block diagram in Figure 26 and the signal overview in 4.2.10.1.

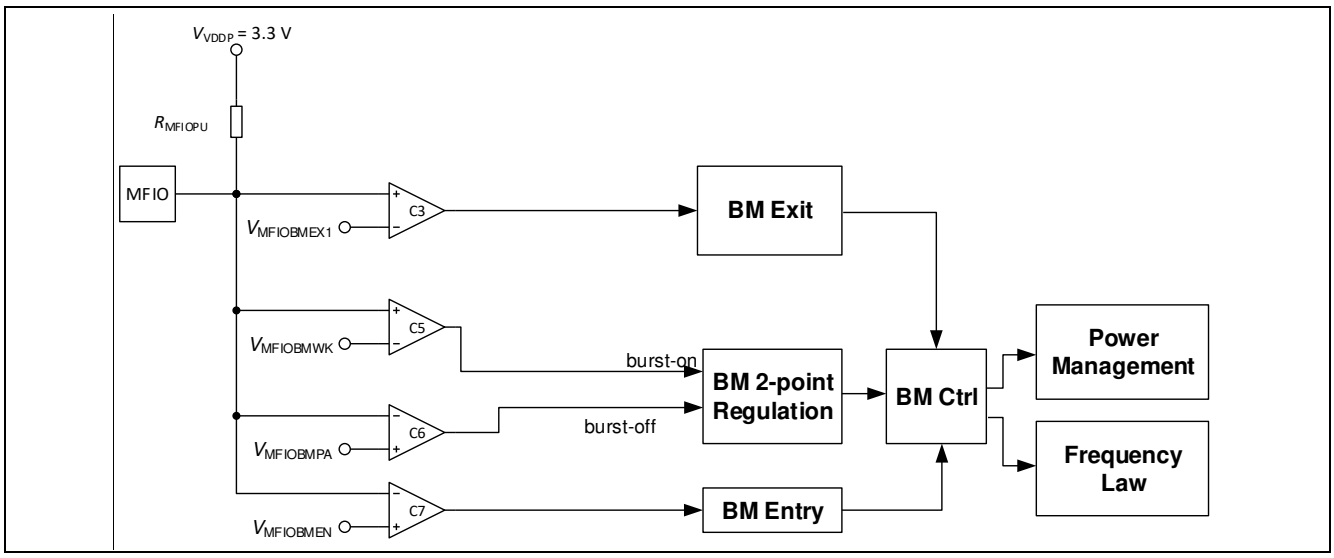

Figure 25 Block diagram burst mode control

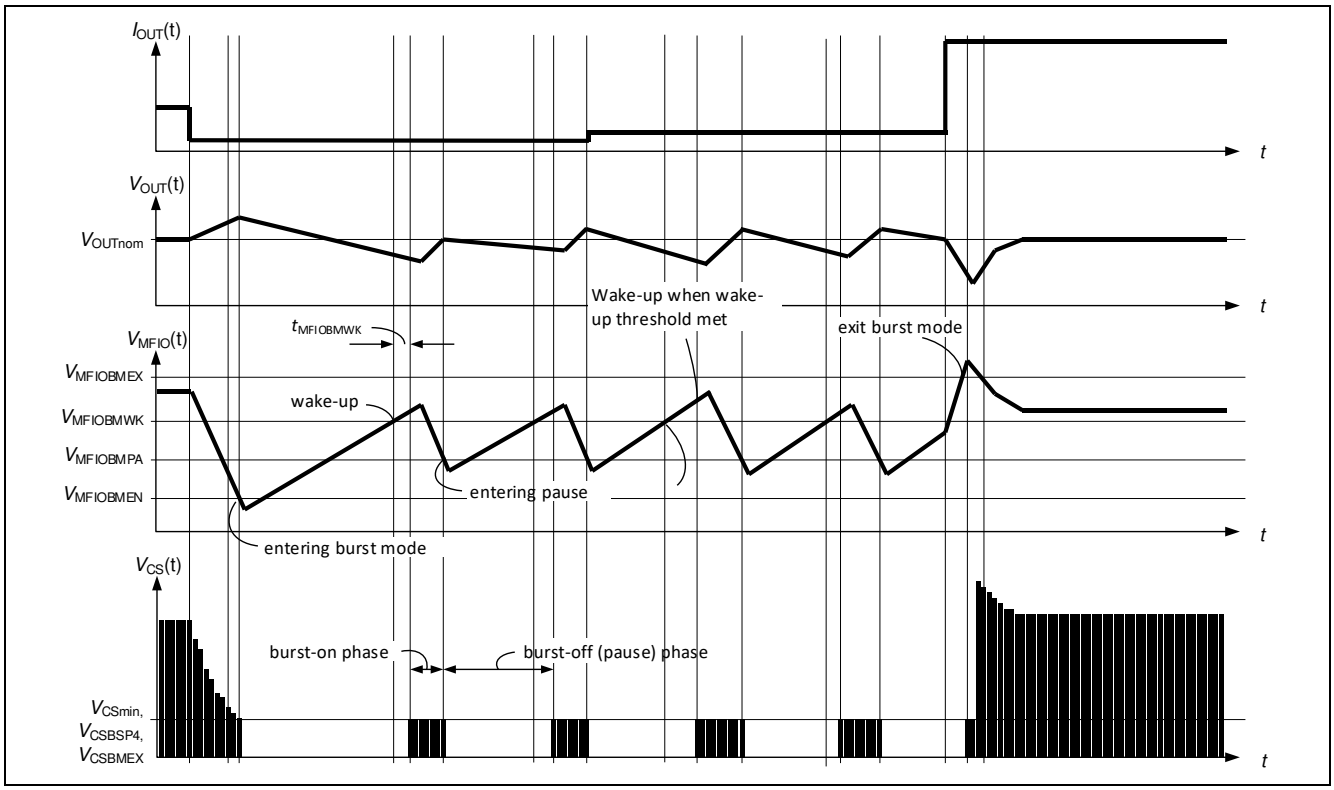

Figure 26 Burst mode signals

4.2.10.1 Burst mode entry

Figure 26 is showing a typical signal scheme for entering quiet burst mode. The frequency law limits the minimum possible power transfer defined at the setpoint F (see Chapter 4.2.8.1). With decreasing load, the voltage at MFIO pin sinks. Once the voltage at MFIO pin falls below the burst mode entry threshold $V_{MFIOBMEN}$, BM is then entered, the IC initiates a burst-off phase, where the IC current consumption is reduced to $I_{VCCquBM2}$. Afterwards, the voltage at MFIO pin controls the output voltage control via the two-point regulator (see Chapter 4.2.10.2).

4.2.10.2 Burst operation

The two-point regulator, that is activated during burst mode operation, is implemented with the comparators C5 and C6 (see Figure 25) with the two thresholds $V_{MFIOBMWK}$ and $V_{MFIOBMPA}$ to determine the burst-on and burst-off phase depending on the feedback signal at the MFIO pin. During this phase, the error signal is now used for the two-point regulator scheme, whereas it correlates with the inverse output voltage AC ripple signal shape (see Figure 26). The wake-up threshold $V_{MFIOBMWK}$ determines the output voltage bottom peak ripple point and the pause threshold $V_{MFIOBMPA}$ determines the output voltage upper peak ripple point. Once the voltage at the MFIO pin exceeds the threshold $V_{MFIOBMWK}$, IC will be waked-up, it takes $t_{MFIOBMWK}$ = 26.6 µs till the first gate pulse of the burst sequence starts. The switching cycles during burst-on phase are predefined and not depending on the voltage at the MFIO pin. All burst sequence pulses have the same switching frequency f_{SWBSPx}, but progressive changed voltage V_{CSBSPx} as shown in Table 17. All following pulses have then the same peak value for V_{CS} as the fourth pulse V_{CSBSP4}. The peak value of the V_{cs} determines, together with the set frequency f_{SWBSP4}, the deliverable limited maximum power during the quiet burst operation. If the output load is exceeding the deliverable limited power for the burst operation, the voltage at MFIO pin will increase. After it exceeds the burst mode exit threshold $V_{MFIOBMEX}$, the control IC may exit burst mode (see Chapter 4.2.10.3).

4.2.10.3 Burst mode exit

At load jumps above the burst mode exit power level, a fast burst mode exit is supported to limit the drop in output voltage. A sudden load demand causes a rising slope at MFIO pin. Once the voltage V_{MFIO} exceeds the threshold $V_{MFIOBMEX}$, the IC exits the burst mode immediately.

Once burst mode is exit, the two-point regulation is terminated and the next pulse is determined by the fixed peak current setting V_{CSBMEX}. The further consecutive pulses are determined by the frequency law (see Chapter 4.2.8) with the voltage V_{MFIO} controlling the switching cycles.

4.2.11 Quasi Resonant Mode

IC has a function to disable ZVS pulse insertion based on configurable bulk cap voltage, if ZVS pulse is disabled, IC enter Quasi resonant mode depend on frequency law settings in Figure 23, i.e the frequency range defined by AB and CD . The Quasi resonant mode at low line is natural ZVS without the need of ZVS pulse and achieves better efficiency since no additional energy injection is needed.

The QR operation is like shown in Figure 27, IC have a frequency band based on Vmfio level, the minimum frequency and max frequency define the Zero crossing number of the operation. E.g If system operates in QR-1 mode, when the load reduce, frequency will go higher and hit max frequency limit, then zero crossing number will increase one , system will run in QR-2. When the load further decreases, IC will go down until the 6th zero crossing in shown example and once min and max frequency limit is same, then IC enter frequency reduction mode.

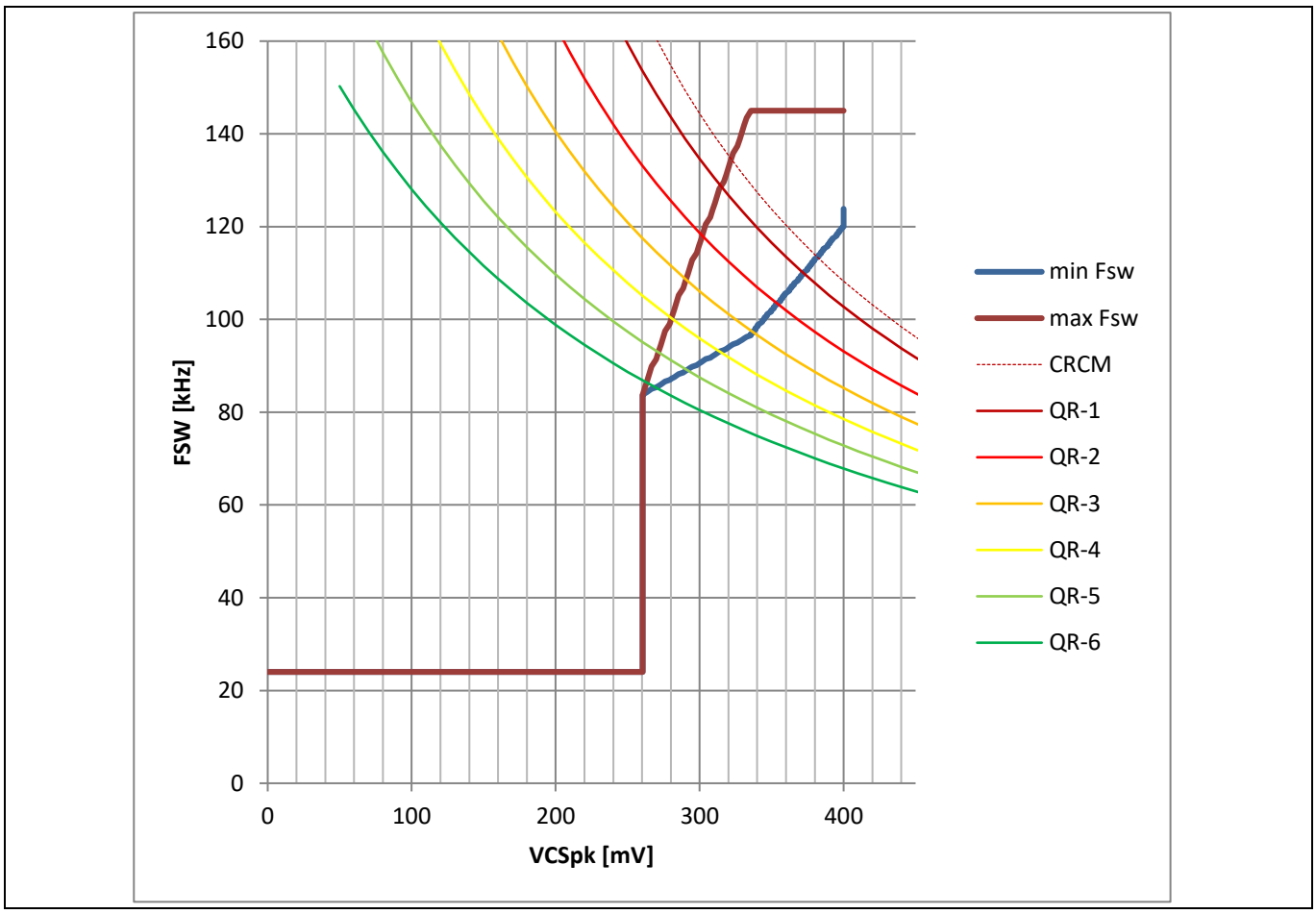

Figure 27 Quasi resonant mode operation range

4.2.12 Forced quasi resonant ZVS mode operation

XDPS21081 provides a special forced quasi resonant ZVS mode to reduce significantly switching losses during operation in discontinuous conduction mode (DCM). Furthermore conducted EMI in the high frequency spectrum > 10MHz and especially radiated EMI can be greatly reduced, which supports the usage of high speed optimized super junction MOSFETs. The idea is to turn on the main power MOSFET only at a controlled lowest drain voltage level in a self-generated oscillation period after demagnetization phase of the flyback transformer has been finished. This self-generated oscillation period is derived from an additional gate driver pulse that introduces to the flyback transformer at a self-determined time a defined negative magnetization. The level of negative magnetization current can be configured (see Chapter 5)

Compared to the so called quasi-resonant (QR) operation, which is focusing on turning on the main power MOSFET only in the valleys after transformer demagnetization, the FQR ZVS provides full control on the switching frequency and the drain voltage swing down level for turning on the MOSFET. Higher frequency design approaches can now be exploited for low line without compromising on efficiency and EMI for the high line operation. When reducing the load, frequency foldback to lowest frequency levels can be supported with avoiding any hard switching cycle (see Chapter 4.2.8.1).

Figure 28 shows the required signals in the application for FQR ZVS mode operation. The second gate driver GD1 drives Q1 for initiating the self-controlled zero voltage switching (ZVS) cycle. The HV pin provides the V_{Bulk} voltage measurement to adapt the timings for the ZVS pulse.

Functional Description

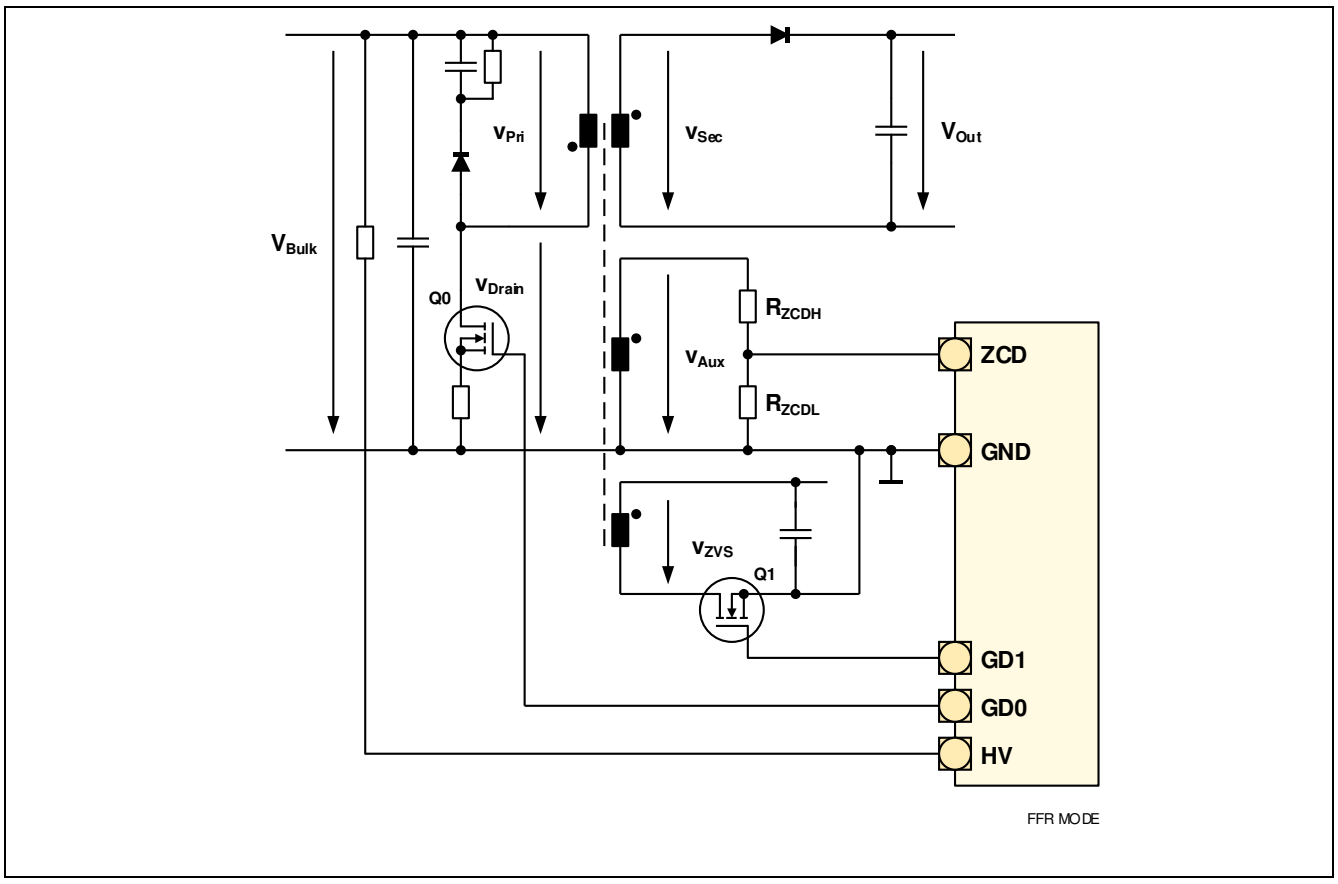

Figure 28 Required signals for forced quasi resonant ZVS mode operation

The ZCD pin provides the zero crossing detection to enable main gate generation. The ZVS gate can be enabled based on configurable line voltage with 20Vdc hysteresis.

Figure 29 shows the FQR ZVS mode signal wave forms and associated timings. The FQR ZVS mode is implemented by introducing a ZVS pulse via the gate driver GD1 during the time frame t1-t2 and subsequent dead-time $t_{ZVSdead}$ from t2-t3 until gate driver GD0 turns on the main power MOSFET. The dead-time $t_{ZVSdead}$ should be dimensioned in such a manner that the turn-on of GD0 takes place at the minimum drain voltage oscillation magnitude, which correlates to a transformer magnetization close to zero. The forced frequency operation of GD0 is achieved by directly controlling the switching period $t_{SWperiod}$ of GD0. GD1 is prematurely turned on after the delay time $t_{ZVSdelay}$, when a zero crossing has been detected.

Functional Description

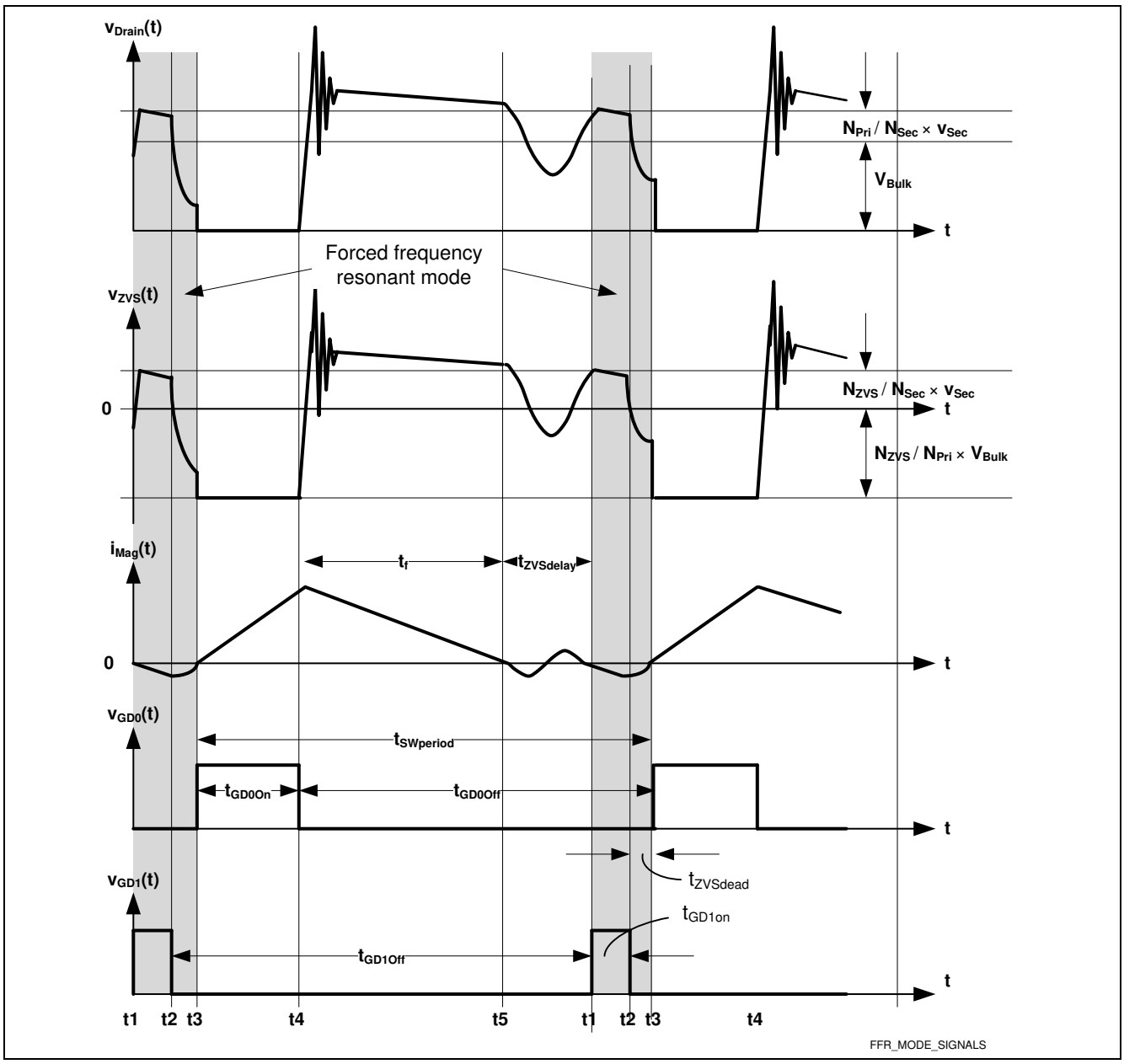

Figure 29 Signal overview for forced frequency resonant mode operation

The length of the ZVS pulse and the charged voltage of the ZVS capacitor determine the amount of introduced negative transformer magnetization. A higher level of introduced negative magnetization leads to a lower drain voltage swing down, which could further optimize the switching losses and high frequency EMI behavior of the main power MOSFET. However, as this comes along with the expense of increased power losses associated with the additional ZVS pulse generation, a trade off needs to be found to maximize the potential increase in efficiency and reduction in EMI. Depending on the chosen main power MOSFET different drain voltage levels might be adapted for turning on the main power MOSFET. This is mainly depending on the output capacitor characteristic of the power MOSFET, which is highly nonlinear increasing, when going for low drain voltages. The amount of necessary negative magnetization current increases with the size of the output capacitor of the power MOSFET and parasitic coupling capacitor of transformer. Therefore the dimensioning for the ZVS pulse generation is significantly depending on the system dimensioning. The default parameter set is optimized for a 65 W USB PD adapter.

The required ZVS pulse length t_{GD1on} is depending on V_{Bulk}. The GD1 on-time t_{GD1on} needs to increase with increasing V_{Bulk} to ensure the same low drain voltage level for turning on the main power MOSFET for the whole VAC input range. Whereas the ZVS dead-time is fixed at $t_{ZVSdead}$ = 236ns (see Chapter 5.2).

The default configured relationship between t_{GD1on} and V_{Bulk} and determined by following implemented equation:

Functional Description

$$t_{GD1on} = \left(V_{bulk} * \frac{K_{zvson}}{65535} \frac{1}{V} + 2\right) * 15.8ns + (2.34V - V_{zcd}) * \frac{K_{zvson_{vout}}}{65535} * \frac{1}{V} * 15.8ns \quad (10)$$

The parameter V_{bulk} (V) is calculated based on the measured current at HV pin I_{HV} via the external resistor R_{HV} = 102kΩ. V_{zcd} is the voltage seen in zcd pin which reflect output voltage, it shows that the zvs ontime is increased if output voltage is reduced.

4.2.13 UART function at GPIO pin

GPIO pin provides a digital IO interface for UART communication. Configuration of defined parameters and HW setups are supported (see Chapter 5.2). The UART function at GPIO pin is normally enabled till the VCC brown-in is reached (see Chapter 4.1.2). After VCC brown-in, the UART function is disabled.

On the other hand, the UART function can be kept enabled during normal operation by sending a corresponding soft command before VCC brown-in. Then configuration “on the fly” is supported and change of parameters during normal operation is possible.

4.3 Protection features

Table 6 shows the protection features and their corresponding reaction on malfunction. Two protection modes (auto-restart mode and latch mode) as well as a HW reset (IC reset by VCC under-voltage lockout) are implemented.

Note: All protection features w/o UVOFF only apply during normal operation. During sleep phase (in burst or protection mode), neither pin measurement of pin voltage nor temperature sensor is active.

Table 6 Protection Features

Protection Feature	Symbol	Reaction	Description
VCC Under-Voltage lockout	UVOFF	Deactivate IC	Chapter 4.3.3
Brown-In Protection (when Brown-in conditions not met)	BIP	Block switching	Chapter 4.3.4
Brown-Out Protection	BOP	Stop switching	Chapter 4.3.5
Over-Current Protection level 1	OCP1	CbC limit	Chapter 4.3.6
Over-current protection level 2	OCP2	Auto-restart	Chapter 4.3.7
Vcc Over-Voltage Protection	VccOVP	Auto-restart	Chapter 4.3.8
MFIO pin High	MFIOH	Auto-restart	Chapter 4.3.9
Internal Over-Temperature Protection	IntOTP	Auto-restart	Chapter 4.3.10
Primary side output Over-Voltage Protection	VoutOVP	Auto-restart / Latch mode	Chapter 4.3.11
Over load protection	OLP	Auto-restart	Chapter 4.3.12
CS pin short protection	CSP	Auto-restart	Chapter 4.3.13

4.3.1 Auto-Restart Mode (ARM)

Once the auto-restart mode is entered, the IC stops the gate driver switching at GD0 pin and enters stand-by mode with reduced current consumption of $I_{VCCquAR}$ = 160 µA. After the auto-restart off-time t_{AR} = 3 s, the control IC resumes its operation with soft-start after the VCC capacitor is charged up and the VCC voltage reaches its turn-on threshold. During the auto-restart off-phase, the HV startup-cell is operating in the bang-bang mode (see Chapter 4.1.5.2) to keep the VCC voltage at a high level to have enough energy stored in the VCC capacitor for the system startup.

4.3.2 Latch Mode (LM)

When latch mode is entered, the gate driver switching at GD0 pin is stopped and the control IC enters stand-by mode where the current consumption is reduced to $I_{VCCquLM}$ = 150 µA. During the latch mode the HV startup-cell is operating in the bang-bang mode to keep the IC alive and staying in latch mode. Here the voltage V_{VCC} is varying in a wider range compared to the bang-bang mode operation in auto-restart mode (see Chapter 4.1.5.1).

4.3.3 VCC Under-Voltage lockout (UVOFF)

The implemented VCC under-voltage lockout (UVLO) ensures a defined activation and deactivation of the IC operation depending on the supply voltage V_{VCC}. The UVLO contains a hysteresis with the voltage thresholds V_{VCCon} = 20.5 V for activating the IC. For deactivating the IC, two thresholds are defined. They are:

- V_{VCCoff} = 7.2 V during normal operation / during auto-restart break time
- $V_{VCCoffBO}$ = 9.6 V after brown-out detected

The higher $V_{VCCoffBO}$ threshold leads to earlier deactivation of the IC and earlier charge-up of the VCC capacitor and supports a new system startup earlier.

Both VCC on- and off-thresholds contain a spike blanking t_{VCCon} and t_{VCCoff}.

4.3.4 Brown-In Protection (BIP)

At initial power-up or auto-restart, the brown-in condition at the HV pin and at the VCC pin must be fulfilled for starting the soft-start procedure. The controller measures the current at HV pin through the internal shunt resistor R_M (see Figure 3). The input brown-in is fulfilled if the current I_{HV} exceeds the threshold I_{HVBI} = 1.15 mA. The VCC brown-in is fulfilled if the voltage V_{VCC} is above the threshold V_{VCCBI} = 15 V. No blanking time applies for brown-in detection. If one of the brown-in conditions is not fulfilled, the IC stays active, but without gate switching. The voltage at VCC pin drops then. Once it falls below the threshold V_{VCCoff} = 7.2 V, the control IC is deactivated, and the startup cell is turned on automatically to charge up the VCC capacitor.

4.3.5 Brown-Out Protection (BOP)

The brown-out protection for bulk voltage prevents the IC from operating with a too low line voltage, which could lead to high RMS current stress in the application. Brown-out detection is also performed via the HV pin as for brown-in detection. Here an under-voltage detection of the bulk voltage V_{Bulk} is provided to support brown-out protection. The measured current I_{HV} is compared with the bulk under-voltage detection threshold I_{HVBO} = 0.443 mA. The brown-out protection applies if bulk under-voltage is detected for certain blanking time. This blanking time is set to t_{HVBO} = 1.09 ms during normal operation and to t_{HVBOSS} = 5.27 ms during soft-start phase. Once brown-out protection is entered, the IC stops switching.

4.3.6 Over-Current Protection level 1 (OCP1)

The over-current protection level 1 (OCP1) is performed by means of the cycle-by-cycle peak current control via the comparator OCP1 (see Figure 3). A leading edge blanking (see Chapter 4.2.5) prevents the IC from false switching-off the power MOSFET due to the leading edge spike. The maximum peak setting for V_{CS} is compensated by the propagation delay compensation (see Chapter 4.2.3), to provide an input voltage level independent current limitation. The highest peak setting for V_{CS} of $V_{CSmaxLL}$(max) = 402mV occurs at low-line and defines the maximal saturation current of the flyback transformer.

4.3.7 Over-Current Protection level 2 (OCP2)

The over-current protection level 2 (OCP2) protects the flyback converter under critical fault conditions such as shorted transformer windings or shorted secondary side rectifier diode. In this case, the repeating cycle-by-cycle over-current protection level OCP1 cannot properly limit the inductor current due to the very steep slope of the current ramp and the propagation delay in the peak current control. With the over-current protection OCP2, once the threshold V_{CSOCP2} = 0.6V is

exceeded for longer than $t_{CSOCP2BL}$ = 616.2 ns during normal operation or $t_{CSOCP2BL}$ = 1.001 µs during startup operation, auto-restart mode (see Chapter 4.3.1) is entered. In this way, over-heating of the flyback converter is avoided.

4.3.8 Vcc Over-Voltage Protection (VccOVP)

The implemented VCC Over-Voltage protection prevent IC from damage caused by unregulated Vcc which may exceed max allowed Vcc level. Once Vcc exceed 21.8V (typ.) and last for longer than blanking time 100µs , IC stop switching immediately and trigger auto restart mode.

The normal operation will be resumed as soon as VccOVP is removed.

4.3.9 MFIO pin high (MFIOH)

There are several phenomena that causes MFIO pin high; feedback loop open, overload, etc. The feedback open-loop protection is implemented by means of a digital comparator C2 (see Figure 3). When the voltage at MFIO pin exceeds the threshold V_{MFIOH} = 2.41 V, a timer is triggered. Auto-restart mode (see Chapter 4.3.1) is entered if the timer exceeds the period of t_{MFIOH} = 31.3 ms. This is mainly for open loop and startup protection, during startup, since the output voltage hasn't reach the setpoint, MFIO pin voltage is always high.

4.3.10 Internal over-temperature detection (IntOTP)

An internal over-temperature protection is implemented in this control IC. Once the internal temperature exceeds the threshold of T_{JOTP} = 130 °C for longer than the blanking time t_{JOTP} = 10.5 ms, internal over-temperature is detected and the control IC enters auto-restart mode (see Chapter 4.3.1). The normal operation will be resumed if the internal temperature is dropped by 20 °C from T_{JOTP}.

4.3.11 Primary side output Over-Voltage Protection (VoutOVP)

The IC provides primary side output over-voltage detection via the ZCD pin. Here the reflected output voltage from the flyback transformer is sampled at ZCD pin during the demagnetization phase (see Chapter 4.2.1.1). In each switching cycle, the XDPS21081 compares the measured output voltage V_{ZCDVO} with the output over-voltage threshold V_{ZCDOVP} = 2.75V.

That comparison can refer to

- The demagnetization phase of the same switching cycle or
- The demagnetization phase of an earlier switching cycle.

A blanking filter is implemented to avoid erroneous output over-voltage detection. This filter consists of a symmetrical counter. Each comparison where $V_{ZCDVO} < V_{ZCDOVP,}$ will decrement the counter (but not below zero) while each comparison where $V_{ZCDVO} \geq V_{ZCDOVP}$ will increment the counter. If the counter is increased to N_{ZCDOVP}+1, auto-restart mode (see Chapter 4.3.1) is entered. This protection mode is a configurable parameter. It can be changed to latch mode (see Chapter 4.3.2) by .dp Vision.

4.3.12 Over load power protection

The IC provides protection against over load by means of the integrated maximum peak current limitation combined with an over-load timer (OLPT). Once OLP is detected, the control IC enters auto-restart mode (see Chapter 4.3.1).

XDPS21081 uses current mode control, so the OCP1 Look-Up-Table (LUT) values are designed by considering the propagation delay at different line voltages and operation modes. Once the OCP1 LUT value is hit, the OLP timer will start to count up. The counter will reduce the count if OCP1 LUT value is not hit in the cause of OCP1 protection. Finally the IC will enter AR if protection timer reaches the pre-definite time.

This protection can distinguish with open loop protection by setting different OLP timer. E.g during power up, Vmfio is always high before voltage rise up, so with different timer, it can separately control the open loop protection and over load protection.

Table 7 Power protection parameters

Protection	Parameter Name	Protection level	Digital value	Blanking time
OLP	L_{OLP}	0.402V @ 72V_{DC} 0.368V @ 372V_{DC}	213.5 @ 72 V_{DC} 213.5 @ 372 V_{DC}	31.3ms

4.3.13 CS pin short protection

During first power up, IC will check three pulses continuously, if the pulses length are longer than 1.5 µs , IC will go to auto restart mode.

5 Configuration

This chapter contains an overview about the parameters and functions that can be configured via the UART interface at GPIO pin. Furthermore the configuration procedure is described. Mapping overviews show the correlation between the data sheet parameters and the correlated firmware symbols. Furthermore the equations are listed to provide the specific correlation between the configured FW parameter and the system parameter.

The chapter “configuration” is grouped in following sections:

- Overview of configuration parameters using .dp Vision (Chapter 5.1)
- Overview of configurable parameters and functions (Chapter 5.2)

The following shown default parameter settings correlate to the firmware version REV 1.0 .

5.1 Overview of configurable parameters using .dp Vision

The Infineon graphic user interface (GUI) .dp Vision connects to XDPS21081 via the isolated USB interface board called .dp Interface Gen2. The .dp interface Gen2 provides power via VCC to XDPS21081 and connects via UART interface at pin GPIO/UART. The common UART interface enables communication with the IC even without the interactive GUI tool. This allows easy configuration during mass production.

For project development, a graphic user interface called .dp Vision guides the designer through the configuration of parameters. More detailed information on .dp Vision can be found in the .dp Vision User Manual prepared by Infineon.

5.2 Overview of configurable parameters and functions

There are 2 types of parameters; configurable and fixed. The configurable parameters are allowed to change. On the other hands, the fixed parameters are not recommended to change. The list of parameters shown is default value and has been verified in the 65W HD adapter demonstrator. The parameters are typical values. Please refer to the corresponding electrical characteristics in Chapter 6.5 for the min/max tolerances.

5.2.1 Configurable parameters and functions

The following table shows the default value of the configurable parameters. If necessary, the parameters can be changed.

Table 8 List of configurable Parameters

Feature	Parameter	Default	Description	Chapter/Table
Propagation delay compensation for peak current control	k_PDC	9000d	Propagation Delay Compensation factor	Chapter 4.2.3,
	k_PDC_OFFSET	0d	Propagation Delay Compensation offset	
Leading edge blanking (LEB)	t_{CSLEB}	283ns	Blanking filter at CS pin to avoid erroneous turn-off of GD0 due to leading edge spike at GD0 turn-on	Chapter 4.2.5
ZVS dead-time	$t_{ZVSdead}$	236ns	Dead-time between end of ZVS pulse at GD1 and start of GD0	Chapter 4.2.11
ZVS pulse length factor	k_{ZVSon}	3600	ZVS pulse length factor per bulk voltage	
	k_{ZVSon_vout}	9000	ZVS pulse length factor per output voltage	
ZVS gate turn on point	T_{zvs_turnon}	750ns 204ns	Turn on of the ZVS gate after Zero crossing detected	

Configuration

Gate driver capability	$I_{\_GD0\_drive}$	35mA	Sourcing current of Gate driver 0	Chapter 4.2.7
ZVS enable voltage	$V_{BULK\_ZVS\_ON}$	250Vdc	Above this voltage ,ZVS gate is allowed to turn on	
	t_{MAX_OnTime}	140000ns		
Protections	T_{JOTP}	130 °C	Internal Over-temperature detection level	Chapter 4.3.10
	t_{ocp2}	600ns	Blanking time for OCP2 of Vcs signal	
	$t_{peakpower}$	30ms	Blanking time for overload protection	
	En_OLP	Enabled	To enable or disable over load protection	
	Response_OVP	Auto restart	Protection mode for OVP, configurable for AR or Latch	Chapter 4.1.5
Burst mode parameters	*Vcs_bst*	0.078V	Burst mode current limit	Chapter 4.2.10
	Freq_bst	50.4kHz	Burst mode frequency	
	V_bst_pause	0.2V	Pause threshold at MFIO pin during on-phase in burst mode operation	
	V_bst_exit	0.26V	Burst mode exit voltage at MFIO pin	
	V_bst_wakeup	0.26V	Burst mode wakeup voltage at MFIO pin	
	T_reentry_bst	0ms	minimum time to re-entry the burst mode	
Adaptive Vcs offset	$K\_V_{cs\_offset}$	20000	Gradient for compensation curve	Chapter 4.2.1.3
	$V_{cs\_offset}\_V_{zcdzeropoint}$	79	ZCD voltage level(digital value) without Vcs offset	
	$En\_V_{cs\_offset}$	Enabled	To enable or disable $V_{cs\_offset\ compensation}$	

6 Electrical Characteristics

All signals are measured with respect to ground GND pin. The voltage levels are valid if other ratings are not violated.

Attention: Limits are subject to change according to test engineering results

6.1 Definitions

Figure 30 illustrates the definition for the voltage and current parameters used in this data sheet.

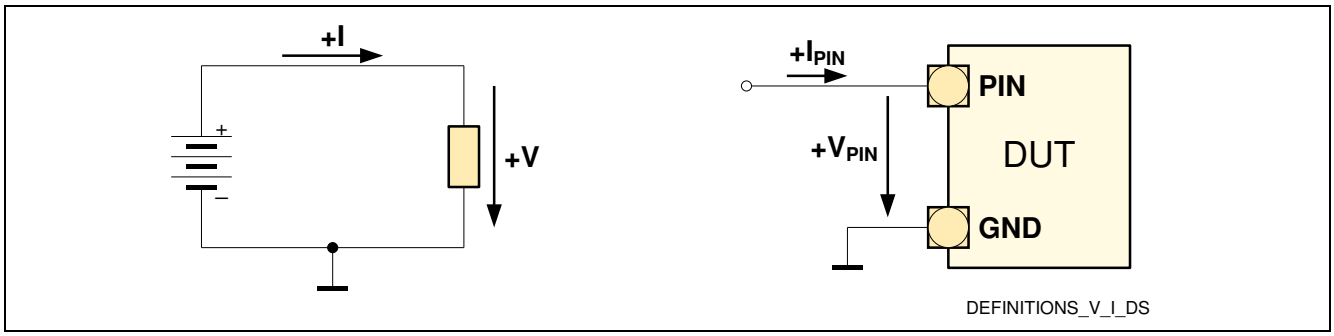

Figure 30 Voltage and Current Definitions

Values indicated under “absolute maximum ratings” must not be exceeded.

Values indicated under “operating conditions” can be exceeded if a corresponding explicit “absolute maximum rating” is given for this parameter, but the related function of the device is not ensured.

6.2 Absolute Maximum Ratings

Stresses above the values listed below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for given periods may affect device reliability. Maximum ratings are absolute ratings; exceeding anyone of these values may cause irreversible damage to the device.

Table 9 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Voltage at VCC pin	V_{VCC}	-0.5	26	V	[3]
Voltage at GD0 pin	V_{GD0}	-0.5	V_{VCC}+0.3	V	Internally clamped to V_{GD0H}
Average current at GD0 pin	$\lvert I_{GD0}\rvert_{AVG}$	—	20	mA	[1], absolute average over 1 ms
RMS Current at GD0 pin	I_{GD0RMS}	—	100	mA	[2], RMS over 20 µs
Voltage at GD1 pin	V_{GD1}	-0.5	V_{VCC}+0.3	V	Internally clamped to V_{GD1H}
Voltage at HV pin	V_{HV}	-0.5	600	V	[3]
Current at HV pin	I_{HV}	—	10	mA	
Voltage at ZCD pin	V_{ZCD}	-0.5	3.6	V	[3]
Maximum negative transient input voltage for ZCD	$-V_{ZCD\_TR}$	—	2.0	V	[4] <500ns
Voltage at CS pin	V_{CS}	-0.5	3.6	V	[3]

Electrical Characteristics

Maximum negative transient input voltage for CS	$-V_{CS\_TR}$	—	3	V	4)<500ns
Maximum transient input clamping current for ZCD and CS	$-I_{CLN\_TR}$	—	6	mA	4)<500ns
Maximum permanent input clamping current for ZCD	$-I_{CLN\_DC\_ZCD}$	—	3.5	mA	
Maximum permanent input clamping current for CS	$-I_{cln\_DC\_CS}$	—	2.5	mA	
Voltage at MFIO pin	V_{MFIO}	-0.5	3.6	V	3)
Voltage at GPIO pin	V_{GPIO}	-0.5	3.6	V	3)
Junction temperature	T_J	-40	125	°C	
Storage temperature	T_S	-55	150	°C	
Maximum power dissipation	P_{TOT}	—	0.46	W	T_A = 60 °C T_J = 125 °C R_{thJA} = 141 K/W
Soldering temperature	T_{Sold}	—	260	°C	5), wave soldering
ESD capability	V_{HBM}	—	2	kV	6), human body model
	V_{CDM}	—	500	V	7), charged device model
Latch-up capability	I_{LU}	—	150	mA	8)

1) Relevant w.r.t. electro migration.
2) Relevant w.r.t. thermal heating at small duty cycles.
3) Permanently applied as DC value.
4) Negative range must fulfill clamping current limits
5) According to JESD22-A111A
6) According to ANSI/ESDA/JEDEC JS-001-2012
7) According to JESD22-C101F
8) According to JESD78D, 85 °C (Class II) temperature

6.3 Package Characteristics

Table 10 Thermal Characteristics

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Thermal resistance from junction to ambient	R_{thJA1}	—	141	K/W	1), JEDEC 1s0p
	R_{thJA2}	—	81	K/W	1), JEDEC 2s2p
Creepage distance between HV vs. GND-related pins	D_{CR}	3.3	—	mm	

1) IC footprint and PCB trace with 35 µm Cu, T_A = 85 °C, 180 mW power dissipation

6.4 Operating Range

Table 11 shows the operating range, in which the electrical characteristics shown in Chapter 6.5 are valid.

Table 11 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Junction Temperature	T_J	-25	*125*	°C	
Voltage at VCC pin	V_{VCC}	V_{VCCoff}	V_{VCCon}	V	[4]
Voltage at HV pin	V_{HV}	-0.3	600	V	
Current into HV pin	I_{HV}	—	5	mA	Limited by external R_{HV}
Voltage at ZCD pin	V_{ZCD}	-0.3	3.3	V	An applied voltage lower than 0V needs to respect the negative maximum clamping current I_{ZCD}
Current into ZCD pin	I_{ZCD}	-1.5	—	mA	
Voltage at CS pin	V_{CS}	-0.3	3.3	V	
Current into CS pin	I_{CS}	-10	0.1	mA	
Voltage at MFIO pin	V_{MFIO}	-0.3	3.3	V	
Voltage at GPIO pin	V_{GPIO}	-0.3	3.3	V	
Voltage at GD0 pin	V_{GD0}	-0.3	V_{VCC}+0.3	V	Internally clamped at V_{GD0H}
Voltage at GD1 pin	V_{GD1}	-0.3	V_{VCC}+0.3	V	Internally clamped at V_{GD1H}
Minimum required capacitive load at GDx pin	$C_{GDxload}$	1.5	—	nF	[1), 2)], $R_{GDxload}$ = 10 Ω in series to $C_{GDxload}$
Low state output reverse current at GDx pin	$-I_{GDxLREV}$	—	100	mA	[3)], applies if V_{GDx} < 0 V and driver at low state

[1)] Not tested in production test.

[2)] See figure in Chapter 8.1

[3)] Assured by design.

[4)] In practical application design, the applied Vcc voltage need to be less than 19V (min. value of V_{VCCon})

6.5 Characteristics

The electrical characteristics involve the spread of values given within the specified supply voltage and junction temperature range T_J from -25 °C to 125 °C. Typical values represent the median values related to T_J = 25°C. All voltages refer to GND and the assumed supply voltage is V_{VCC} = 14 V, if not otherwise mentioned.

The following characteristics are specified

- Power Supply at VCC pin (Table 12)
- HV pin (Table 13)
- ZCD pin(Table 14)
- MFIO pin (Table 15)
- GPIO pin (Table 16)
- CS pin (Table 17)
- GDx pin (Table 18)
- IC Control Features (Table 19)
- IC Protection Features (Table 20)

Table 12 Electrical Characteristics of the Power Supply at VCC pin

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
VCC UVOFF current	$I_{VCCUVOFF}$	—	30	50	µA	$V_{VCC} < V_{VCCon}$(min) - 0.3 V
VCC operating current	I_{VCCop1}	—	7.5	8.7	mA	[1], normal operation with gate driver GDx output low, GPIO pin open, I_{MFIO}-=280 µA
	I_{VCCop2}	—	—	8.4	mA	[1], as for I_{VCCop1}, but T_J = 110 °C
	I_{VCCop3}	—	—	8.2	mA	[1], as for I_{VCCop1}, but T_J = 100 °C
	I_{VCCop4}	—	—	8.0	mA	[1], as for I_{VCCop1}, but T_J = 85 °C
	I_{VCCop5}	—	11	—	mA	[1], C_{load} = 2 nF, f_{SWGDx} = 83 kHz, I_{MFIO}=-280µA,T_J=25 ˚C
VCC average quiescent current in latched mode	$I_{VCCquLM}$	0.080	0.150	0.300	mA	V_{VCC}=8 V, latch mode, MFIO, GPIO open
VCC average quiescent current during sleep phase in auto-restart mode	$I_{VCCquAR}$	—	0.160	0.310	mA	V_{VCC}=7 V, sleep phase in auto-restart mode, MFIO, GPIO open
VCC quiescent current during sleep phase in quiet burst mode	$I_{VCCquBM1}$	—	0.18	1.2	mA	Burst mode entered, MFIO, GPIO pin open
	$I_{VCCquBM2}$	—	0.46	1.5	mA	[1], [2], burst mode entered, I_{MFIO}=-280 µA, GPIO pin open

Electrical Characteristics

	$I_{VCCquBM3}$	—	—	1.2	mA	[1], as for $I_{VCCquBM2}$, T_J=110 °C
	$I_{VCCquBM4}$	—	—	1.0	mA	[1], as for $I_{VCCquBM2}$, T_J=100 °C
	$I_{VCCquBM5}$	—	—	0.8	mA	[1], as for $I_{VCCquBM2}$, T_J=85 °C
VCC turn-on threshold	V_{VCCon}	19	20.5	21.5	V	dV_{VCC}/dt =0.2 V/ms
VCC turn-off threshold	V_{VCCoff}	6.84	7.2	7.56	V	During normal operation, IC latched and auto-restart break time
VCC turn-on/off hysteresis during normal operation	$V_{VCChysOP}$	—	13.3	—	V	[1]
VCC turn-off blanking time	t_{VCCoff}	550	—	—	ns	[1], 1 V overdrive
VCC turn-on delay	t_{VCCon}	—	—	2	µs	[1]
VCC threshold for turning on HV startup cell in protection mode	$V_{VCCBBon}$	8.5	9	9.5	V	[1], bang-bang mode during auto-restart and latch mode
Blanking time for turning on HV startup cell in auto-restart and latch mode	$t_{VCCBBon}$	0.6	—	2.2	µs	[1], 1 V overdrive, bang-bang mode
VCC threshold for turning off HV startup cell in auto-restart and latch mode	$V_{VCCBBoff}$	19	20.5	21.5	V	
Blanking time for turning off HV startup cell in auto-restart and latch mode	$t_{VCCBBoff}$	0.7	—	2.4	µs	[1], 1 V overdrive, bang-bang mode
VCC brown-in threshold	V_{VCCBI}	8.4	9.1	9.7	V	[1], [3]
VCC Over-Voltage Protection threshold	V_{VCCOVP}	20.9	21.8	22.7	V	[1], [3]
VCC Over-Voltage Protection Blanking time	$t_{VCCOVPBLK}$	—	100	—	µs	[1], [3]

[1] Not tested in production test.

[2] Current value is based on the sum of external sink current I_{MFIO} and IC quiescent current $I_{VCCquBM1}$.

[3] See configuration Chapter5

Table 13 Electrical Characteristics of HV pin

Electrical Characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Brown-in threshold	I_{HVBI}	1.10	1.156	1.21	mA	[1],[2], no blanking
Brown-out threshold	I_{HVBO}	0.420	0.443	0.465	mA	with blanking t_{HVBO}
Brown-out blanking time during normal load	t_{HVBO}	0.99	1.09	1.21	ms	[1], [2], [3]
Brown-out blanking time during soft-start	t_{HVBOSS}	4.95	5.27	5.59	ms	[1], [2]
HV peak VCC charge current capability	$I_{HVchargeVCC}$	2.4	5	10	mA	[4], V_{VCC}=1 V, V_{HV}=30 V
Leakage current at HV pin	I_{HVLK}	—	—	10	µA	V_{HV}=600 V, HV startup cell disabled
Bulk voltage threshold for special frequency clamp	V_{bulk_high}		200		V	[1]

[1] Not tested in production test.

[2] See configuration Chapter 5.

[3] Min. and max. values are based on master clock period t_{MCLK} limits (see Table 20).

[4] Max. peak charge current will be limited in the application by an external resistor connected to HV pin.

Table 14 Electrical Characteristics of ZCD pin

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input leakage current, no pull device	I_{ZCDLK}	-10	—	10	µA	V_{ZCD}=0 V/3 V
		-1	—	1	µA	[1], T_J=85 °C V_{ZCD}=0 V/3 V
ZCD voltage threshold	V_{ZCDTHR}	20	35	55	mV	
ZCD voltage threshold debouncing time	t_{ZCDPW}	150	—	—	ns	[1], shorter pulses are ignored
ZCD zero crossing comparator propagation delay	t_{ZCDP}	20	40	60	ns	[1]
ZCD ringing suppression time	t_{ZCDRS}	570	608	647	ns	[1], [2]
ZCD clamping of neg. voltages	$-V_{ZCDclp}$	150	180	220	mV	
Minimum time from GD0 turn off to first zero-crossing to ensure settling of ZCD sampling	$t_{GD0offZCMin}$	—	—	3.33	µs	[1]

Electrical Characteristics

ZCD output over-voltage threshold in HV mode	V_{ZCDOVP}	2.72	2.75	2.79	V	[1], [2] $t_{GD0offZC} \geqslant t_{GD0offZCMin}$
ZCD debouncing counter threshold for output over-voltage detection	N_{ZCDOVP}	—	2	—		[1], [2] $t_{GD0offZC} \geqslant t_{GD0offZCMin}$
ZCD threshold voltage for compensation of ZVS ontime based on output voltage	V_{zcd_vout}		2.34		V	[1]
ZCD threshold voltage hysteresis		-	0.177	-	V	[1]

[1] Not tested in production test.

[2] See configuration Chapter 5.

Table 15 Electrical Characteristics of MFIO pin

Assuming LL (low line) =72V, HL (high line) =372V, L_{PRI}=200uH, R_{CS}=0.135 Ω

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input leakage current without pull device activated	I_{MFIOLK}	-10	—	10	µA	V_{MFIO}=0 V/3 V
		-1	—	1	µA	[1], T_J=85 °C V_{MFIO}=0 V/3 V
Open circuit output voltage	V_{MFIOOC}	3.0	3.3	3.6	V	Normal mode
		3.0	3.2	3.4	V	[1], [2], sleep mode
Open-loop detection threshold	V_{MFIOH}	2.25	2.30	2.36	V	[1], [3]
Maximum control range	$V_{MFIOmax}$	—	2.30	—	V	[1], [3]
Setpoint B of the frequency law	V_{MFIOB}	1.56	1.61	1.66	V	[1], [3]
Setpoint C of the frequency law	V_{MFIOC}	2.25	2.30	2.36	V	[1], [3]
Setpoint D of the frequency law	V_{MFIOD}	1.19	1.23	1.28	V	[1], [3]
Setpoint E of the frequency law	V_{MFIOD}	0.82	0.86	0.91	V	[1], [3]
Setpoint F of the frequency law	V_{MFIOD}	0.17	0.21	0.25	V	[1], [3]

Electrical Characteristics

Burst mode entry threshold	$V_{MFIOBMEN}$	0.175	0.209	0.242	V	[1], [3]
Internal pull-up resistor	R_{MFIOPU}	8.8	11	13.2	kΩ	[3]
Burst wake-up threshold during burst-off phase	$V_{MFIOBMWK}$	0.231	0.266	0.300	V	[1], [3]
Minimum input pulse width for burst wake-up	$t_{MFIOBMWKPW}$	300	—	—	ns	[1], shorter pulses will be suppressed
Time between burst wake-up and the first burst sequence pulse	$t_{MFIOBMWK}$	—	26.6	32	µs	[1], dV_{MFIO}/dt = 100 mV/µs
Burst-off entering threshold during burst-on phase	$V_{MFIOBMPA}$	0.175	0.209	0.242	V	[1], [3]
BM exit threshold	$V_{MFIOBMEX}$	0.231	0.266	0.300	V	[1], [3]

Not tested in production test.

During burst mode, auto restart and latch mode operation.

See configuration Chapter 5.

Table 16 Electrical Characteristics of GPIO pin

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input leakage current without pull device activated	I_{GPIOLK}	-10	—	10	µA	V_{GPIO}=0 V/3 V
		-1	—	1	µA	[1], T_J=85 °C V_{GPIO}=0 V/3 V
Open circuit output voltage	V_{GPIOOC}	3.0	3.3	3.6	V	
Input capacitance	C_{GPIOIN}	—	—	10	pF	[1]
Threshold for logic “0”	V_{GPIOIL}	—	—	1.0	V	
Threshold for logic “1”	V_{GPIOIH}	2.0	—	—	V	
Low input pull-up current	$-I_{GPIOLPU}$	30	—	90	µA	[2] at V_{GPIOIL}(max)
Output sink current	$I_{GPIOSNKOL}$	—	—	2	mA	
Output source current	$-I_{GPIOSRCOH}$	—	—	2	mA	
Output rise time (0 → 1)	$t_{GPIORISE}$	—	—	50	ns	20 pF load, push/pull output
Output fall time (1 → 0)	$t_{GPIOFALL}$	—	—	50	ns	20 pF load, push/pull output

[1] Not tested in production test.

[2] Currents flowing out of the device (DUT) are marked with a negative sign in the ‘Symbol’ column

Electrical Characteristics

Table 17 Electrical Characteristics of CS pin

Assuming LL (low line) =72V, HL (high line) =372V, L_{PRI}=200uH, R_{CS}=0.135 Ω

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input leakage current without pull device activated	I_{CSLK}	-10	—	10	µA	V_{CS}=0 V/3 V
		-1	—	1	µA	1), T_J=85 °C V_{CS}=0 V/3 V
CS OCP2 threshold	V_{CSOCP2}	—	0.60	—	V	
CS OCP2 propagation delay until GD0 turn-off at I_{GD0}>2mA	$t_{CSGD0OCP2}$	125	155	190	ns	1) dV_{CS}/dt=100 V/µs
CS OCP2 blanking time for auto-restart	$t_{CSOCP2BL}$	498.8 810	616.2 1001	733.6 1192	ns ns	Normal operation During startup 1), 2), 3)
CS OCP1 comparator minimum pulse width	$t_{CSOCP1PW}$	—	35	—	ns	1), shorter pulses will be suppressed
CS OCP1 propagation delay until GD0 turn-off at I_{GD0} > 2 mA	$t_{CSOCP1PDLL}$	180	260	345	ns	1), low line use case
	$t_{CSOCP1PDHL}$	120	185	250	ns	1), high line use case
	$t_{CSOCP1PD}$	100	130	165	ns	1), dV_{CS}/dt=100 V/µs
CS OCP1 threshold steps	ΔV_{CSOCP1}	—	2.371	—	mV	
CS OCP1 threshold accuracy	$\Delta V_{CSOCP1THR}$	-25	—	25	mV	1)
Leading edge blanking time	t_{CSLEB}	255	269	284	ns	1), 2), 3)
CS OCP1 maximum CS limit	$V_{CSmaxLL}$	370	402	431	mV	1), 2), low line use case
	$V_{CSmaxHL}$	323	368	417	mV	1), 2), high line use case
Tolerance for CS OCP1 maximum CS FASTOPP limit	$\Delta V_{CSFASTOPPLL}$	-50	—	50	mV	1),low line use case
	$\Delta V_{CSFASTOPPHL}$	-60	—	60	mV	1), high line use case
CS limit at setpoint B	V_{CSBLL}	305	336	365	mV	1), 2),low line use case
	V_{CSBHL}	257	303	351	mV	1), 2),high line use case
CS limit at setpoint C	V_{CSCLL}	370	402	431	mV	1), 2),low line use case
	V_{CSCHL}	323	368	417	mV	1), 2),high line use case
CS limit at setpoint D	V_{CSCLL}	229	260	289	mV	1), 2),low line use case
	V_{CSCHL}	189	227	275	mV	1), 2),high line use case

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CS limit at setpoint E	V_{CSCLL}	229	260	289	mV	[1], [2],low line use case
	V_{CSCHL}	189	227	275	mV	[1], [2],high line use case
CS limit at setpoint F	V_{CSCLL}	35	67	96	mV	[1], [2],low line use case
	V_{CSCHL}	-	33	82	mV	[1], [2],high line use case
Minimum CS limit at burst mode entry	$V_{CSminLL}$	35	67	96	mV	[1], [2],low line use case
	$V_{CSminHL}$	0	33	82	mV	[1], [2],high line use case
Burst sequence: 1st pulse CS limit	$V_{CSBSP1LL}$	—	78	—	mV	[1], [2],low line use case
	$V_{CSBSP1HL}$	—	44	—	mV	[1], [2],high line use case
Burst sequence: 2nd pulse CS limit	$V_{CSBSP2LL}$	—	78	—	mV	[1], [2],low line use case
	$V_{CSBSP2HL}$	—	44	—	mV	[1], [2],high line use case
Burst sequence: 3rd pulse CS limit	$V_{CSBSP3LL}$	—	78	—	mV	[1], [2],low line use case
	$V_{CSBSP3HL}$	—	44	—	mV	[1], [2],high line use case
Maximum CS limit during burst mode operation	$V_{CSBSP4LL}$		78		mV	[1], [2], low line use case 4th and consecutive pulses after start of burst sequence
	$V_{CSBSP4HL}$		44		mV	[1], [2], high line use case 4th and consecutive pulses after start of burst sequence
CS limit for 1st pulse directly after BM exit	$V_{CSBMEXLL}$		86		mV	[1], [2],low line use case
	$V_{CSBMEXHL}$		52		mV	[1], [2],high line use case
Initial soft-start CS limit limitation without PDC	V_{CSSSLL}	24	—	83	mV	[1], [2],low line use case
	V_{CSSSHL}	46	—	129	mV	[1], [2],high line use case
Soft-start step for cycle by cycle limitation	ΔV_{CSS}	—	1.71	—	mV	[1], [2],step every $t_{\Delta VCSS}$

[1] Not tested in production test.

[2] See configuration Chapter 5.

[3] Min. and max. values are based on master clock period t_{MCLK} limits (see Table 19).

Table 18 Electrical Characteristics of GDx pin

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Low state sink peak current	$I_{GDxLPKSNK}$	500	—	—	mA	[1], V_{GDx}=4 V, C_{Load}=2 nF
Low state resistance	$R_{GDxLSNK}$	—	—	6.5	Ω	
High state peak source current of GD_1	$-I_{GD1HPKSRC}$	100	118	136	mA	[2], [3], C_{Load}=2 nF

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High state peak source current of GD_0	$-I_{GD0HPKSRC}$	30	35	41	mA	[2], [3], C_{Load}=2 nF
High state output voltage	V_{GDxH}	9.97	10.5	11.03	V	[3], I_{GDx}=-1 mA
High state rail-to-rail output voltage	V_{GDxHRR}	V_{VCC}-0.5	—	V_{VCC}	V	V_{VCC}<V_{GDxH}
APD low voltage (active pull down while device is not powered or gate driver is not enabled)	V_{GDxAPD}	—	—	1.6	V	I_{GDx}=5 mA
Permanent pull-down resistor inside gate driver	R_{GDxPPD}	450	600	750	kΩ	

[1] Not tested in production test.

[2] Currents flowing out of the device (DUT) are marked with a negative sign in the 'Symbol' column.

[3] See configuration Chapter 5.

Table 19 Electrical Characteristics of IC Control

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
VREF internal voltage reference	V_{REF}	2.397	2.428	2.459	V	
Time base 1	t_{Base1}	49.50	52.1	54.78	µs	[1]
Time base 2	t_{Base2}	99.0	104.28	109.56	µs	[1]
Master clock period	t_{MCLK}	15.0	15.8	16.6	ns	[2]
Stand-by clock period	t_{STBCLK}	9.09	10.0	11.11	µs	[3]
Maximum soft-start time	t_{SSmax}	6.64	7.0	7.36	ms	[1]
Boot sequence time when activating IC	t_{BootIC}	—	1.2	—	ms	[1],[4], V_{VCC}>V_{VCCon}
Maximum frequency operation	f_{SWmax}	132.3	139.1	146.6	kHz	[1]
Switching frequency setting at minimum power operation point	f_{SWmin}	21.9	23.0	24.3	kHz	[1]
Burst sequence: 1st pulse switching frequency	f_{SWBSP1}	—	50.2	—	kHz	[1]
Burst sequence: 2nd pulse switching frequency	f_{SWBSP2}	—	50.2	—	kHz	[1]
Burst sequence: 3rd pulse switching frequency	f_{SWBSP3}	—	50.2	—	kHz	[1]

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Burst sequence: 4th and consecutive pulse switching frequency	f_{SWBSP4}	—	50.2	—	kHz	[1]
Switching frequency 1st pulse directly after BM exit	$f_{SWBMEXHV}$	132.3	139.1	146.6	kHz	[1]

[1] Not tested in production test.

[2] The master clock period is the base for all time measurements without stand-by. Relative tolerances of all performed time measurements are same as with t_{MCLK}.

[3] The stand-by clock is the base for all time related characteristics during stand-by operation.

[4] Phase for loading the OTP content to the internal RAM

Table 20 Electrical Characteristics of IC Protection Features

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Auto-restart bang-bang mode off-time	$t_{BBoffAR}$	455	500	556	ms	[1],[2]
Auto-restart time	t_{AR}	2.73	3	—	s	[1],[2]
Blanking time of open-loop timer	t_{MFIOH}	29.7	31.3	33	ms	[1],[3] $V_{MFIO}>V_{MFIOOLP}$
Over-temperature detection	T_{JOTP}	122	130	-	°C	[1],[4]
Over-temperature blanking time	t_{JOTP}	9.90	10.50	11.10	ms	[1],[3]
Over-temperature Hysteresis	T_{JHYS_OTP}	-	20	-	°C	[1]

[1] Not tested in production test.

[2] Min. and max. values are based on stand-by clock period t_{STBCLK} limits (see Table 20).

[3] Min. and max. values are based on master clock period t_{MCLK} (see Table 20).

[4] The recommended temp is below 125 °C, above this temperature, IC function cannot be guaranteed, Customer should guarantee the design will never exceed the 125 °C of IC die temperature.

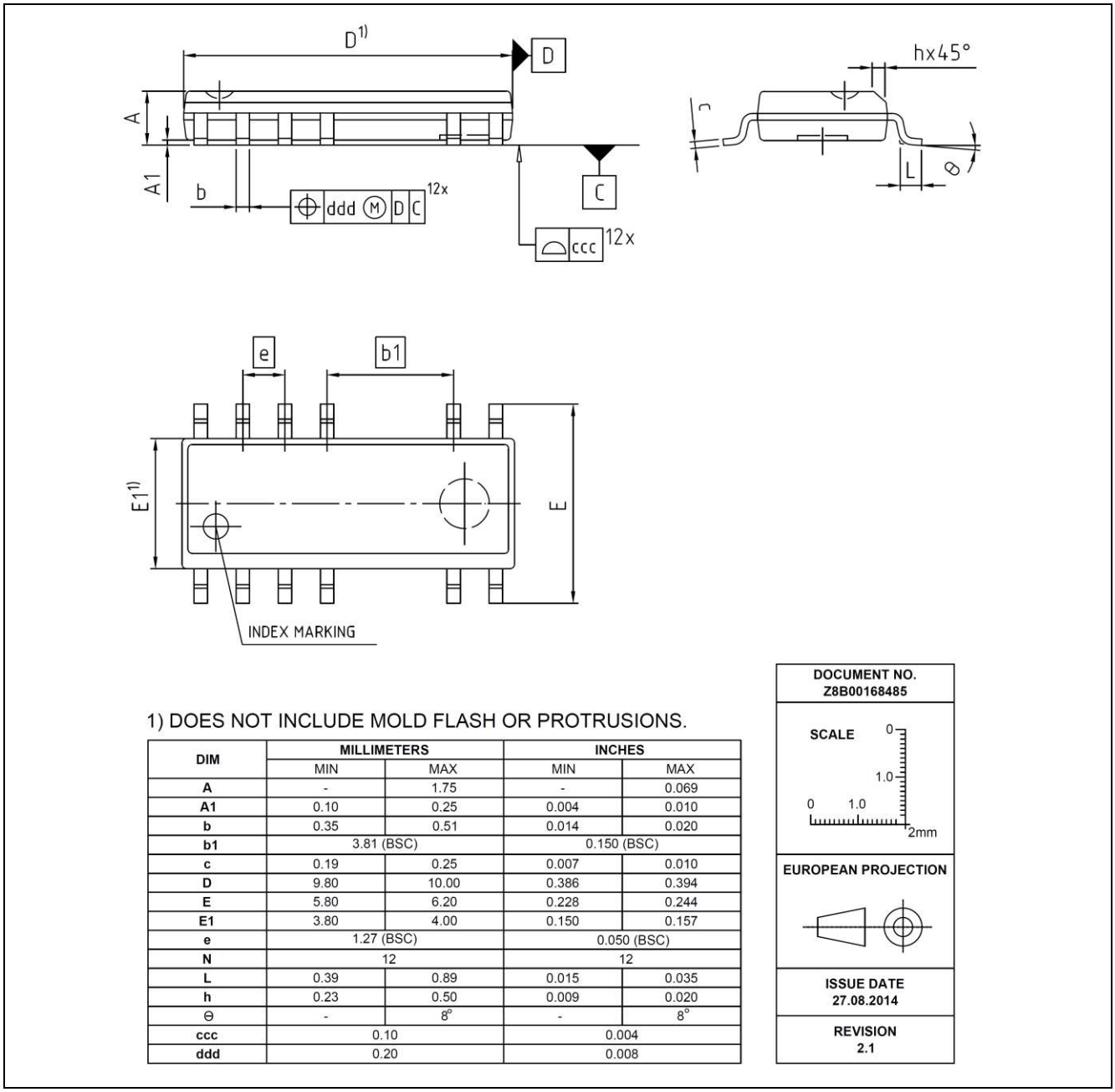
7 Package Information

The package information contains the outline dimensions (see Chapter 7.1); footprint and packing overviews (see Chapter 7.2).

Notes

1. *You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": **http://www.infineon.com/products**.*
2. *Dimensions in mm.*

7.1 Outline dimensions



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
b	0.35	0.51	0.014	0.020
b1	3.81 (BSC)		0.150 (BSC)	
c	0.19	0.25	0.007	0.010
D	9.80	10.00	0.386	0.394
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 (BSC)		0.050 (BSC)	
N	12		12	
L	0.39	0.89	0.015	0.035
h	0.23	0.50	0.009	0.020
Θ	-	8°	-	8°
ccc	0.10		0.004	
ddd	0.20		0.008	

Figure 31 PG-DSO-12 Package Outline

7.2 Footprint and packing

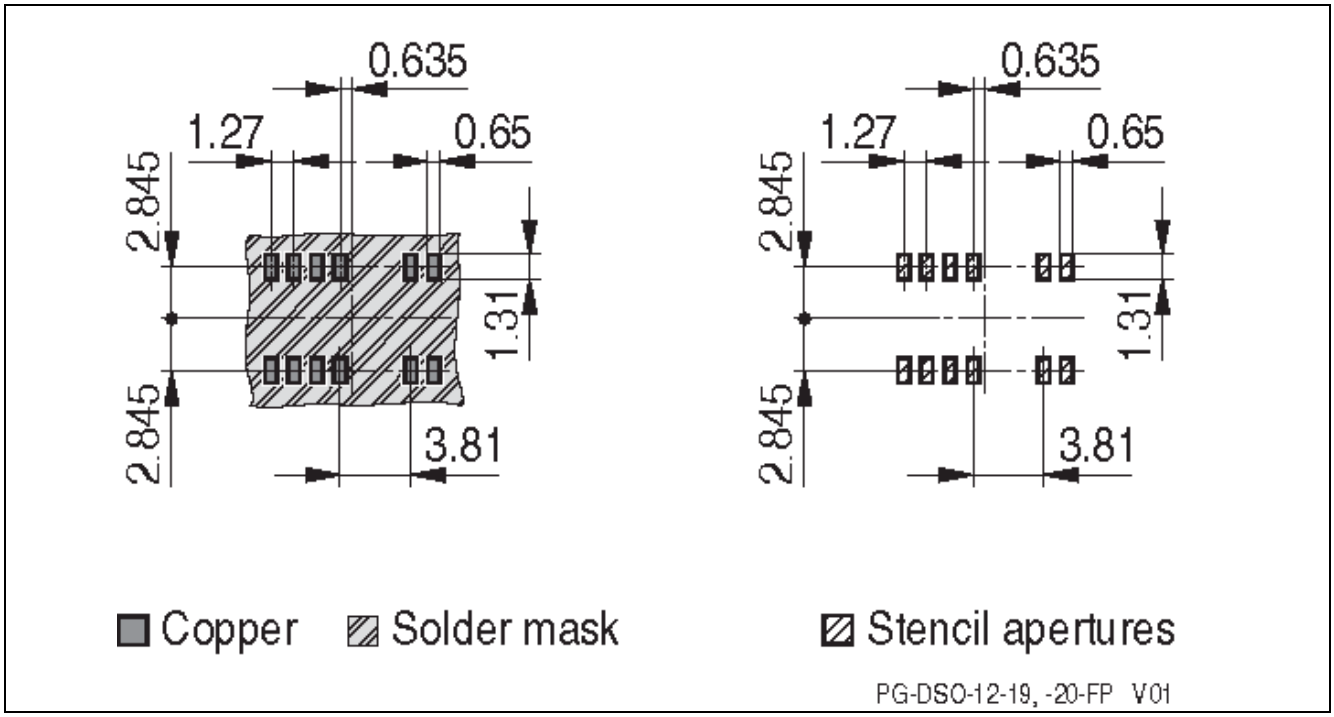


Figure 32 Overview footprint

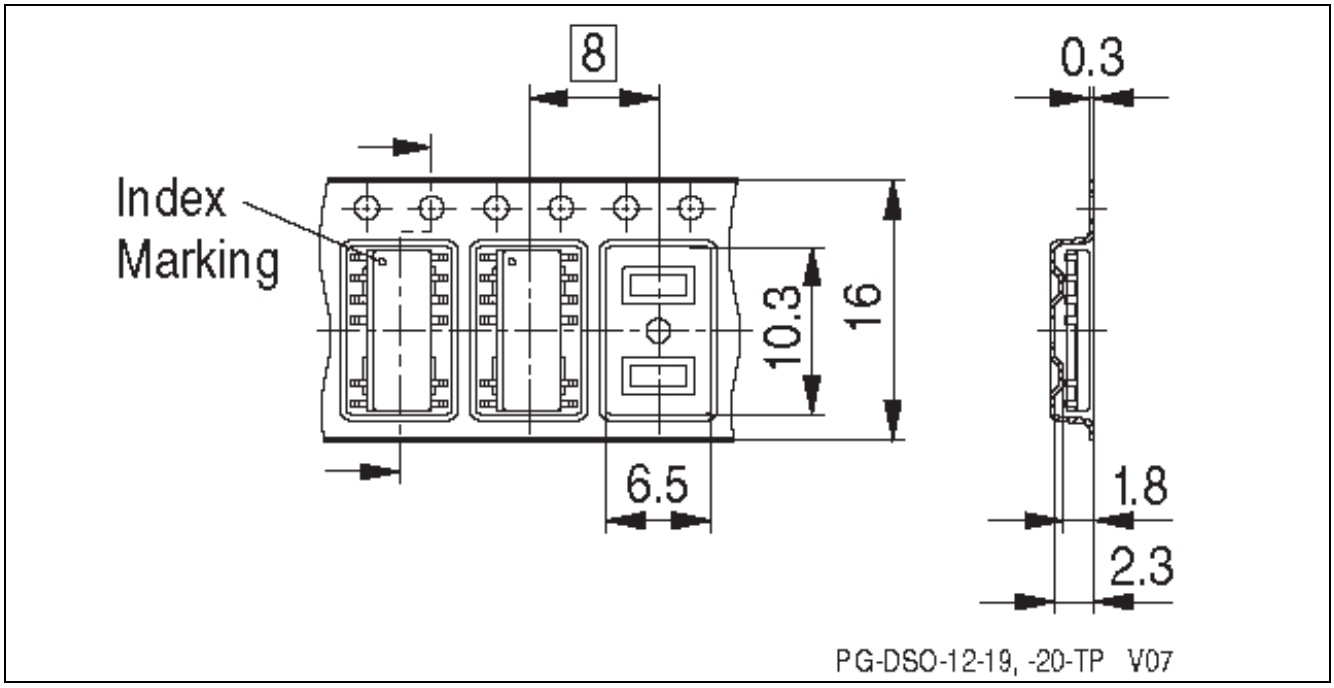


Figure 33 Overview packing

8 Marking

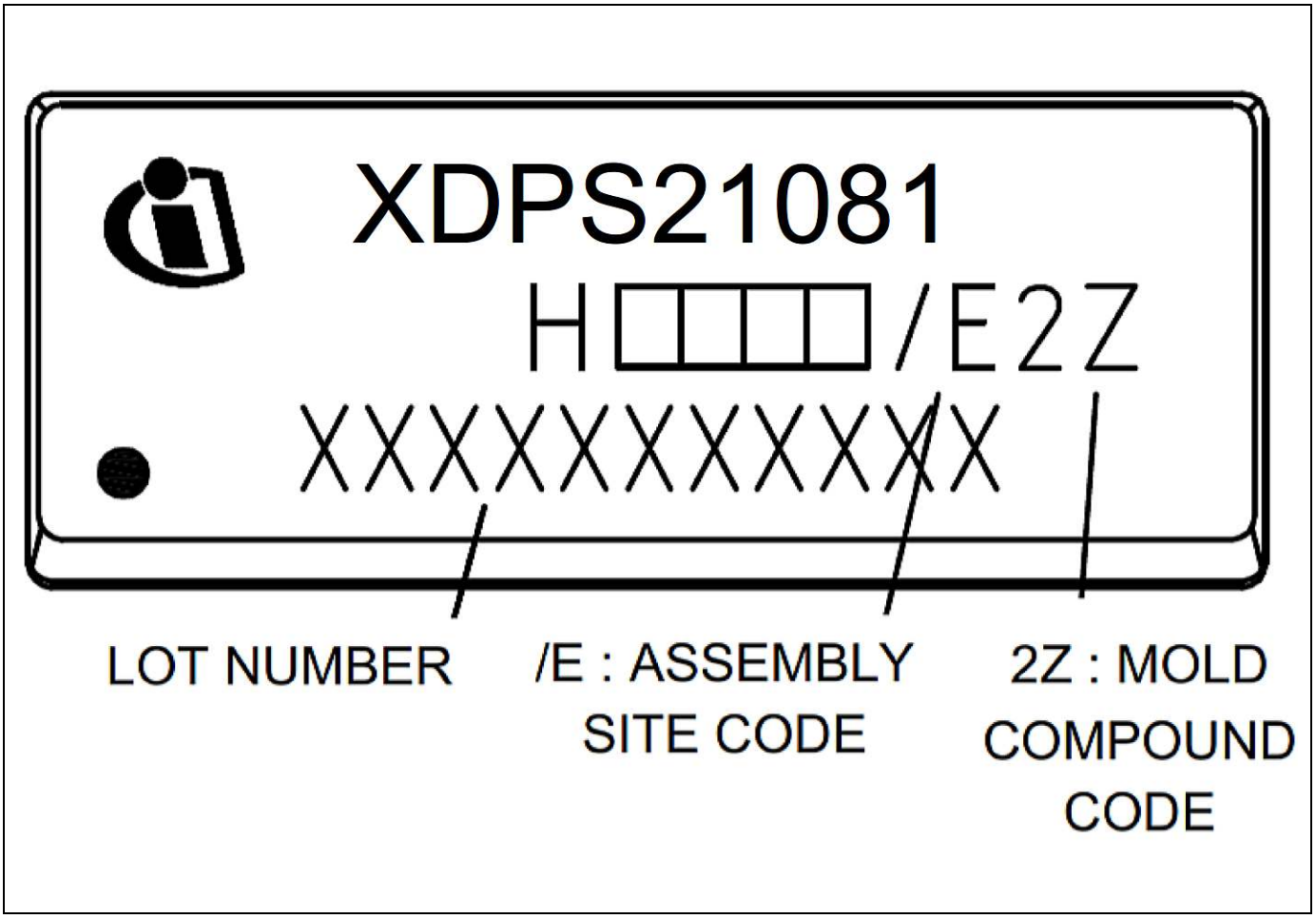


Figure 34 Marking of XDPS21081

9 Appendix

This appendix contains additional information on electrical characteristics and specific test conditions.

9.1 Minimum required capacitive load at GD0 and GD1 pin

The output stage of GD0 and GD1 consist of a controlled current source (see 4.2.7). This current source charges up an external capacitive load until the voltage level V_{GDxH} = 10.5 V is reached. The internal control loop for this source current requires a minimum load capacitance at GDx pin to avoid a turn-on ringing on the signal V_{GDx}.

The minimum required capacitive load is depending on the dimensioned serial gate resistor at GDx pin, which is meant for limiting the low state sink current.

Furthermore, the required load is depending on the configured source current. The shown dependency in Figure 35 is based on the typical source current of $-I_{GDxHPKSRC}$=118mA. Lower configured values for the source current requires also smaller capacitive loads.

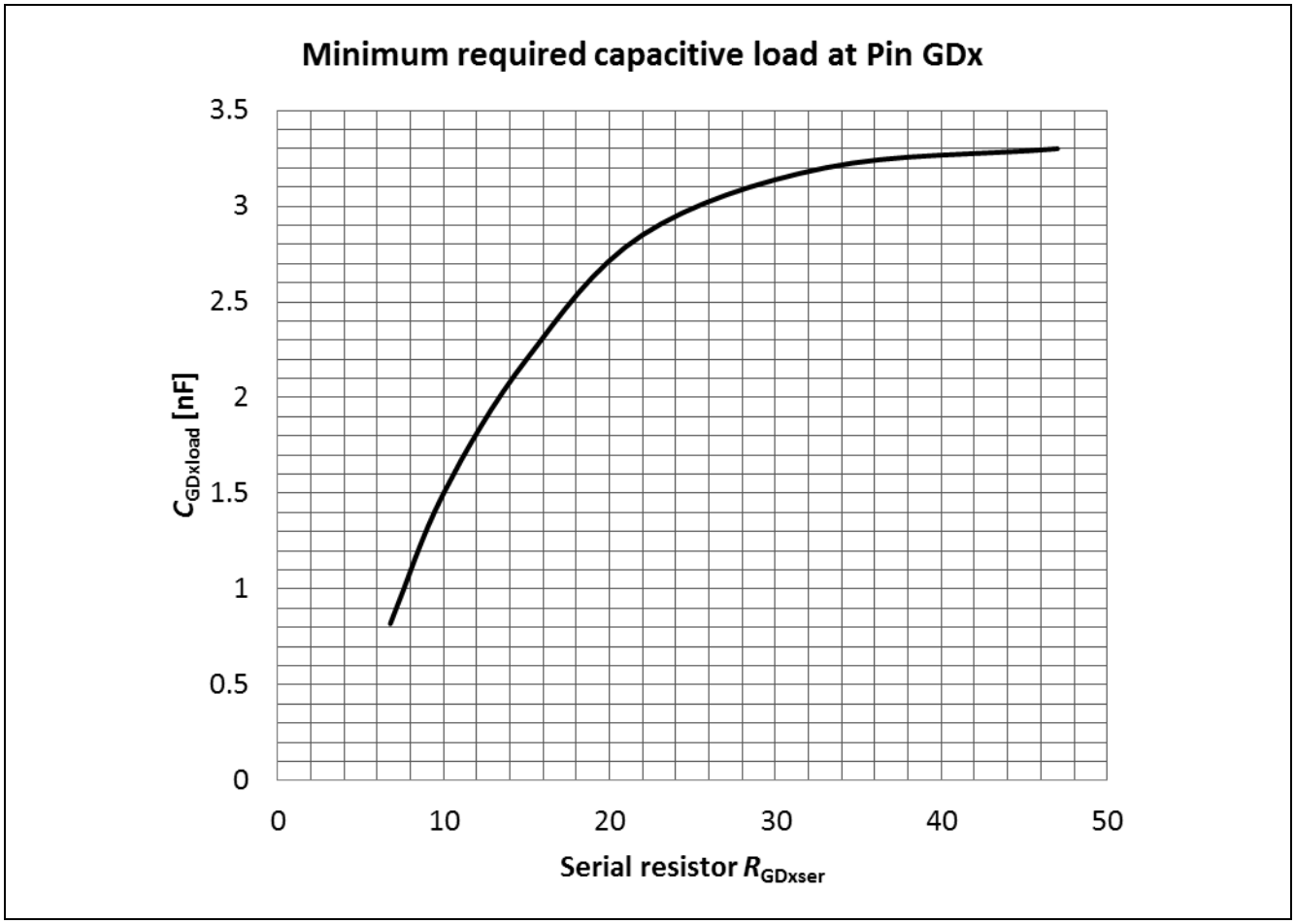


Figure 35 Minimum required capacitive load at GDx pin in correlation with serial gate resistor

10 References

The following list shows the reference documents that are used as base for this data sheet.

[1] Development firmware version: REV 1.0

Revision history

Major changes since the last revision

Document version	Date of release	Description of changes
V 2.0	20 Aug 2020	First release

Edition 2020-01-13

Published by

Infineon Technologies AG

81726 München, Germany

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Document reference

Infineon-XDPS21081-DS-v2.0-EN

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