TUSB6020 Evaluation Model (EVM) Compatible With TMS320C6437 DaVinci LC EVM

User's Guide

Literature Number: SLAU242
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TUSB6020 EVM

The TUSB6020 is a USB 2.0 high-speed, On-the-Go (OTG) high-performance dual-role USB controller with intergrated PHY designed for a seamless connection to the VLYNQ serial interface, and is ideal for a wide range of applications. The USB OTG dual-role controller can operate either as a function controller for a USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other functions. The integrated USB 2.0 PHY provides one-port operation at low speed (1.5 Mb/s), full speed (12 Mb/s), and high speed (480 Mb/s).

The device is fully compliant with *Universal Serial Bus Specification* Revision 2.0 and *On-The-Go Supplement to the USB 2.0 Specification* Revision 1.3.

The TUSB6020 EVM is compatible with several TI DSP platforms that are equipped with a mini-PCI interface with an active VLYNQ connection. This includes the DM6437 Digital Video Development Platform as well as the C6424 DSP Evaluation Module. The TUSB6020 EVM can provide a variety of USB functions to a DSP platform. Specifically, the TUSB6020 EVM has proven OTG host and OTG device capability. Alternatively, the TUSB6020 EVM can be configured to respond as a USB mass storage device.

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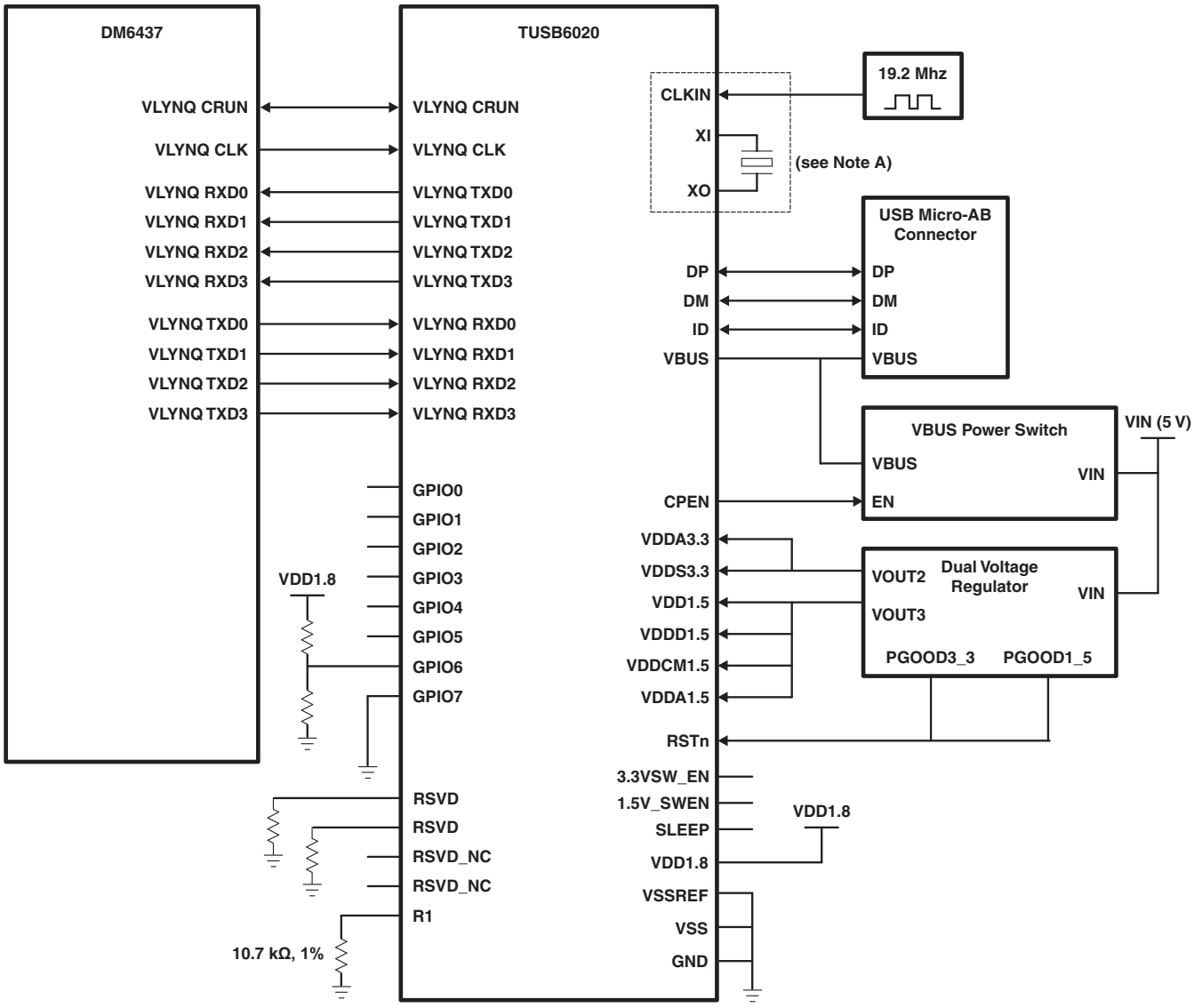
1.1 TUSB6020 Connection Overview

Figure 1-1 shows a high-level diagram of the connections between the TUSB6020 and the various components on the TUSB6020 EVM, as well as the DSP platform.



A Only CLKIN or XI/XO is required. This is selected by GPIO6 at power up.

Figure 1-1. TUSB6020 Connection Block Diagram

1.2 TUSB6020 EVM

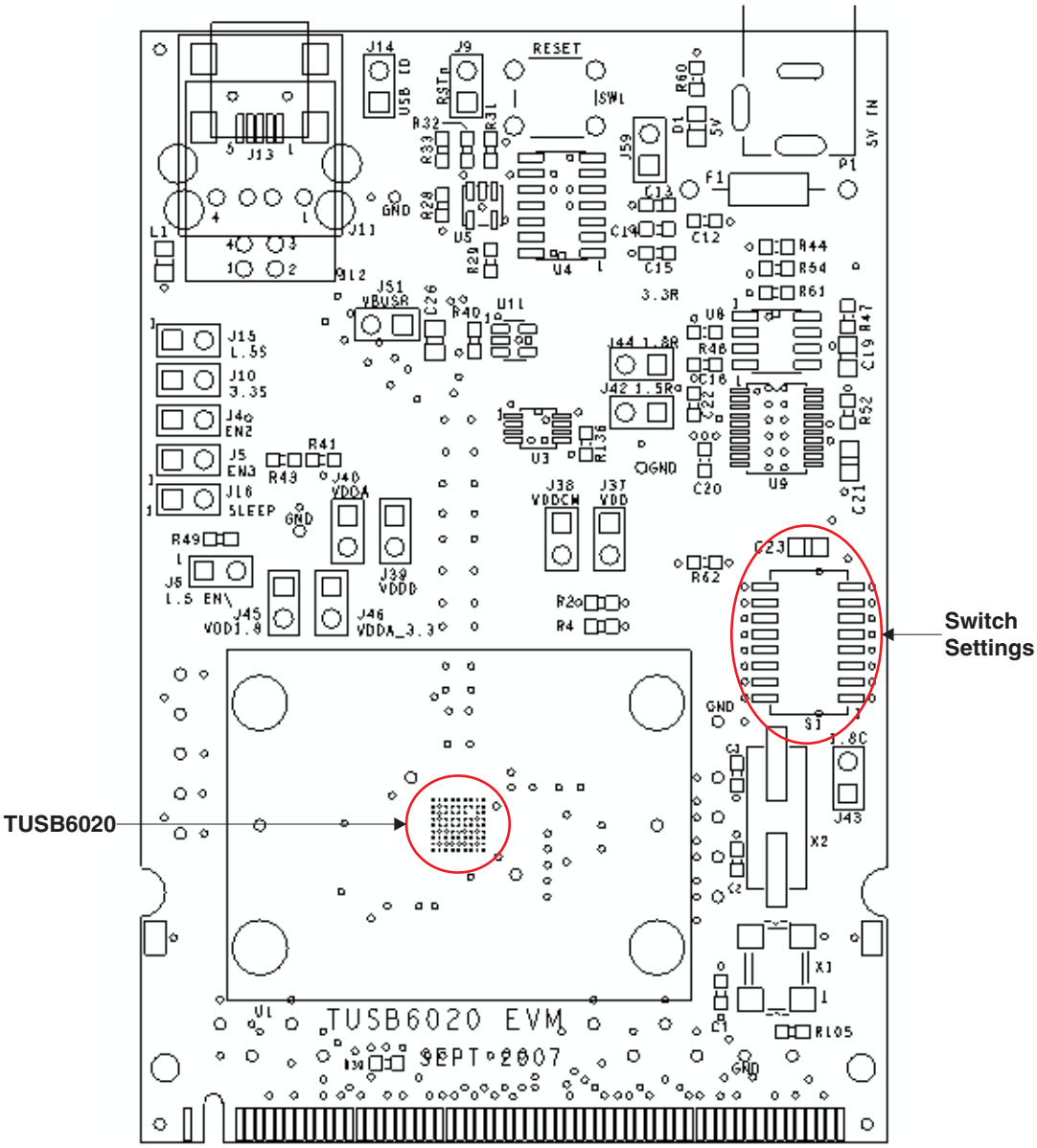


Figure 1-2. TUSB6020 EVM – Top Side

1.3 TUSB6020 EVM Features

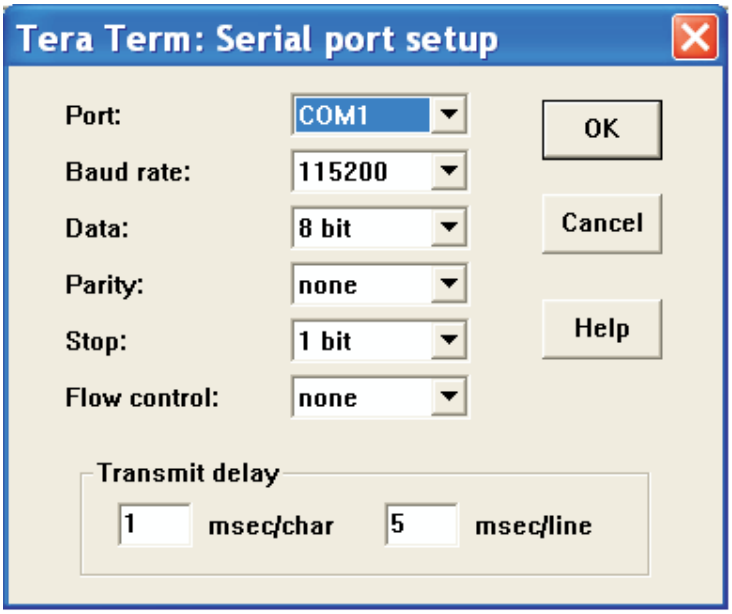
- The TUSB6020 EVM is shipped with a USB mini-AB connector, J13, installed. There are also overlapping footprints on the EVM for a USB Standard A connector and a USB Standard B connector. If one of these options is needed, the mini-AB connector can be de-soldered from J13, and a B connector added to J12 or an A connector added to J11. There is also a jumper, J14, that allows for the ID pin of the mini-AB connector to be grounded for test purposes if installed.
- There are two clock source options available on the TUSB6020 EVM. There is a 24-MHz crystal clock source, X2, and a 19.2-MHz oscillator clock source, X1. The clock source used by the TUSB6020 is detemined by the setting of Switch 7 of the toggle switch set, S1.
- The toggle switches at S1 connect to the GPIO7:0 pins of the TUSB6020. Switch 8 must be turned on at power-up (GPIO7 = low) for the TUSB6020 to operate properly. The setting of switch 7 at power up is used to determine the clock source. After power up, any of the switches can be used as inputs for the associated GPIOs.
- A reset to the TUSB6020 device can be generated in a variety of ways on the TUSB6020 EVM. A reset can be manually generated using the pushbutton installed at SW1. A reset is generated automatically based on the power-good outputs of the voltage regulator at power up. In addition, by installing jumper, J9, a reset can be generated and held by installing the jumper to ground.
- There are a number of test jumpers and test points on the TUSB6020 EVM that are not necessary to TUSB6020 EVM operation but could be used to test functionalities for use in production designs. Some of these are: the SLEEP jumper at J16, the 1.5V_SWEN jumper at J15, the 3.3V_SWEN jumper at J10, and the jumper on the level shifted version of CP_EN at J4.
- The power circuitry of the TUSB6020 EVM is set up to allow for easy power measurements. The 5-V power jack at P1 is not installed because the TUSB6020 can be powered by the DSP platform via the mini-PCI interface. To take a power measurement, the trace connecting the associated jumper pins should be cut and the jumper installed so that an ammeter can be inserted between the pins. See the schematic for particulars on voltage rails, but traces connect the jumper pins on the following: J37, J38, J39, J40, J42, J43, J45, J46, J51, and J59.

1.4 Quick Hardware Setup

1. Check that switches 7 and 8 in S1 are set to select the TUSB6020 normal device mode and the clock source. For normal operation, switch 8 must be turned on to pull GPIO7 low. Switch 7 must be turned on to select the XI clock input (24 MHz) with GPIO6 pulled low or left off to select the CLKIN clock input (19.2 MHz) with GPIO6 pulled high.
2. Insert the TUSB6020 EVM into the mini-PCI slot of the unpowered TMS320C6437 or TMS320C6424 EVM.
3. Connect a UART cable from the TMS320C6437 EVM to a PC.
4. Connect a mini-USB cable from EMU-USB, J501, of the TMS320C6437 EVM to a PC loaded with the Code Composer, CCStudio v3.3, C6424 software.
5. Add wallpower to 5V IN, J14, of the TMS320C6437 EVM.
6. Check that LEDs, DS5 and DS502, are lit on the TMS320C6437 EVM.
7. Check that LED D1 is lit on the TUSB6020 EVM.

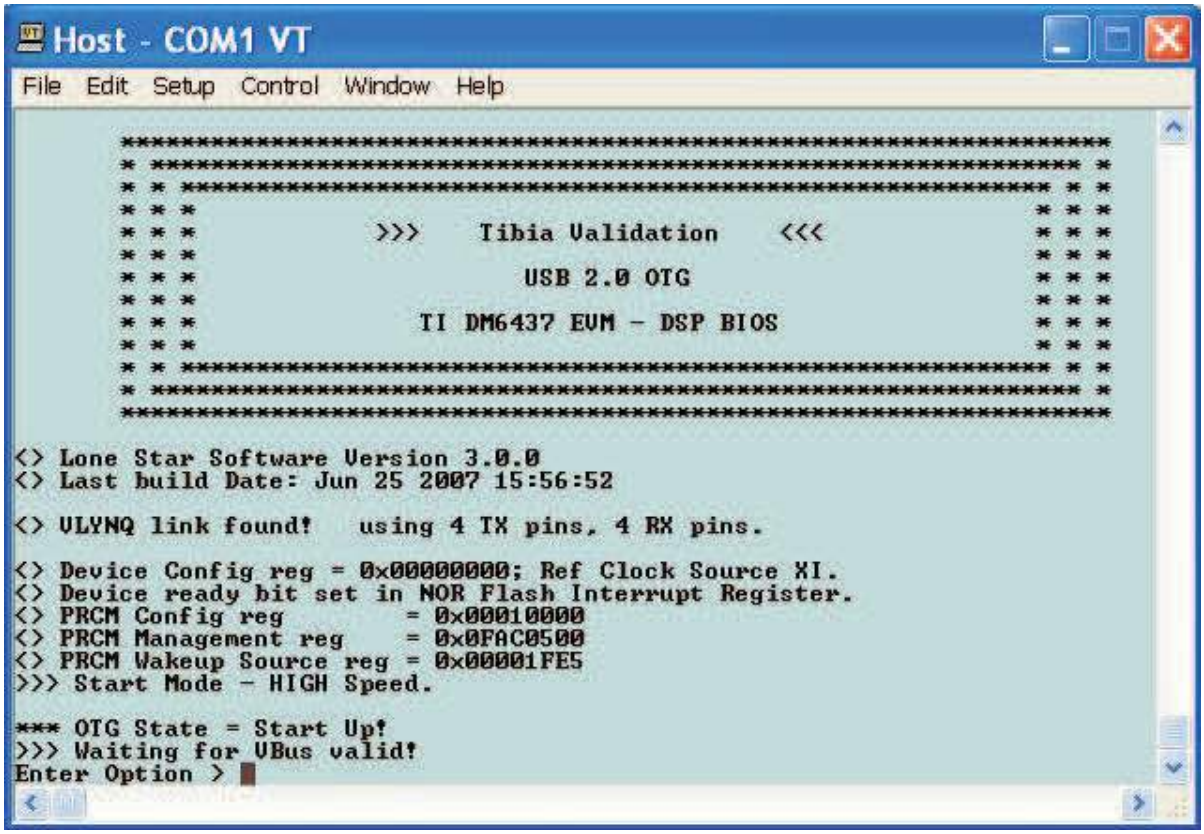
1.5 Quick Software Setup

1. Set up the COM port.

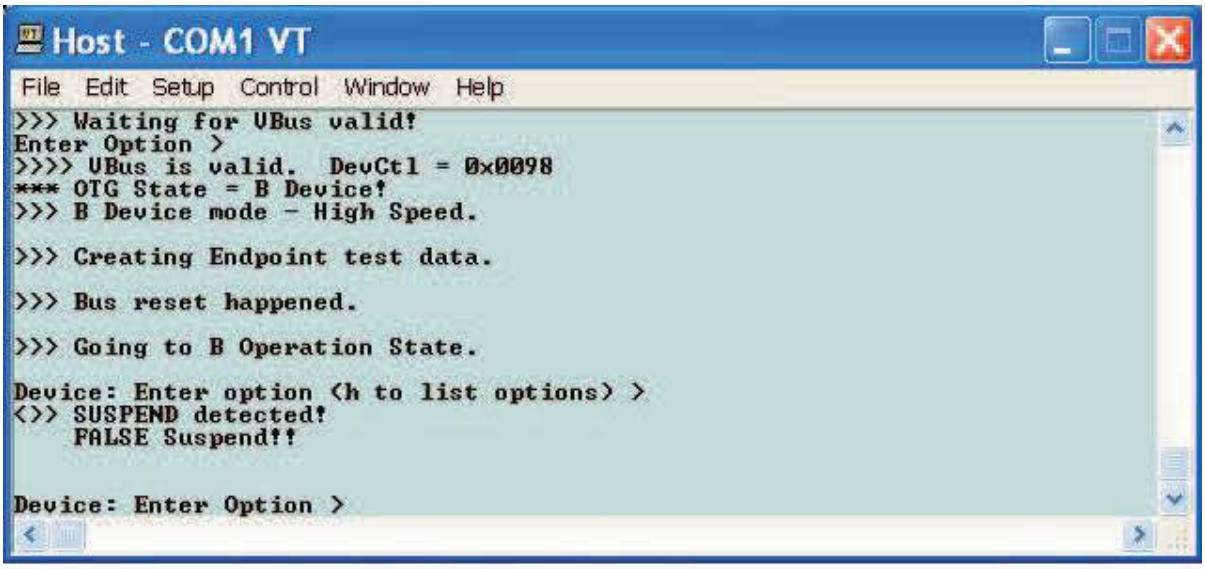


2. Start the Code Composer software select Debug → Connect.

3. Select File → Load program and select the program and then run it. On the COM port you should see:



4. Connect a USB cable from a PC to the TUSB6020 EVM. You should see the following on the COM port:



5. At the prompt, enter h to display a list of test options.

1.6 TUSB6020 EVM Features

Table 1-1. Bill of Materials and Schematics

ITEM	QUANTITY	REFERENCE	PART	PKG	MANUFACTURER	PART NO.	NOTES
1	10	C1, C28, C30, C38, C39,C42, C44, C53, C56, C59	.01 µF	603			
2	2	C2, C3	33 pF	603			
3a	7	C12, C58, C6, C62, C63,C64, C65	10 µF	603			
3b	3	C19, C21, C23, C13, C18,C20, C22, C27, C29, C37,C40, C41, C43, C54,C57	10 µF, Tantalum	805			
4	15	C60, C66, C67	.1 µF	603			
5	2	C14, C45	1 µF	603			
6	1	C15	4.7 µF	603			
7	1	C26	1 µF	805			
8	1	D1	GREEN	805	Panasonic	LNJ306G5PRX	
9	1	F1	3A FUSE	N/A	LittelFuse	R251003	
10	19	J4, J5, J6, J9, J10, J14, J15, J16, J37, J38, J39, J40, J42, J43, J44, J45, J46, J51, J59	HDR2X1 M .1				DNI
11	1	J11	USB Series A	N/A			DNI
12	1	J12	USB Series B	N/A			DNI
13	1	J13	USB Mini/Micro AB		Mill-Max	MNE20-5G5P10	

Table 1-1. Bill of Materials and Schematics (continued)

ITEM	QUANTITY	REFERENCE	PART	PKG	MANUFACTURER	PART NO.	NOTES
14	23	J20, J21, J22, J23, J24, J25, J26, J27, J28, J29, J30, J31, J32, J33, J34, J35, J36, J54, J55, J56, J57, J58, J61	PAD				DNI
15	1	L1	INDUCTOR	mpz.pdf	TDK	MPZ2012S331AT	
16	1	P1	5 V at 3 A		CUI Inc	CP-202AH	
17	1	P2	128 pin Mini PCI Edge	N/A	N/A	N/A	DNI
18	1	R2	10.7K 1%	603			
19	15	R4, R30, R4, R106, R107, R108, R109, R110, R111, R112, R113, R114, R115, R123, R124	1K	603			
20	16	R28, R40, R43, R49, R61, R62, R105, R116, R117, R118, R119, R120, R121, R122, R135, R136	10K	603			
21	4	R29, R31, R32, R48	0	603			
22	1	R33	0	603			DNI
23	4	R44, R47, R52, R54	250K	603			
24	1	R60	330	603			
25	1	SW1	SW TACT		Alps	SKHHALA010	
26	1	S1	SW DIP-8		ITT	TDA08H0SK1R	
27	1	U1	TUSB6020	ZQE80	TI	TUSB6020ZQE	
28	1	U3	SN74LVC2T45, Dual Bit/Supply Transceiver	SM8	TI	SN74LVC2T45DCTR	
29	1	U4	SN74ALVC08, Multiple AND Gate	SOIC14	TI	SN74ALVC08D	
30	1	U5	TPS3836E18, Reset Supervisor	5SOT-23	TI	TPS3836E18	
31	1	U8	TPS77618, 1.8 V Regulator	SOIC8	TI	TPS77618D	
32	1	U9	TPS70848, Dual Voltage Rregulator	SM20	TI	TPS70848PWP	
33	1	U11	TPS2051B, V_{BUS} Power Switch	DBV5	TI	TPS2051BDBV	
34	1	X1	19.2 MHz, CSX-1	SMT	Crystek	601512	
35	1	X2	24 MHz, C_L = 20 pF	SMT	Crystek	16808	

1.7 TUSB6020 Schematics

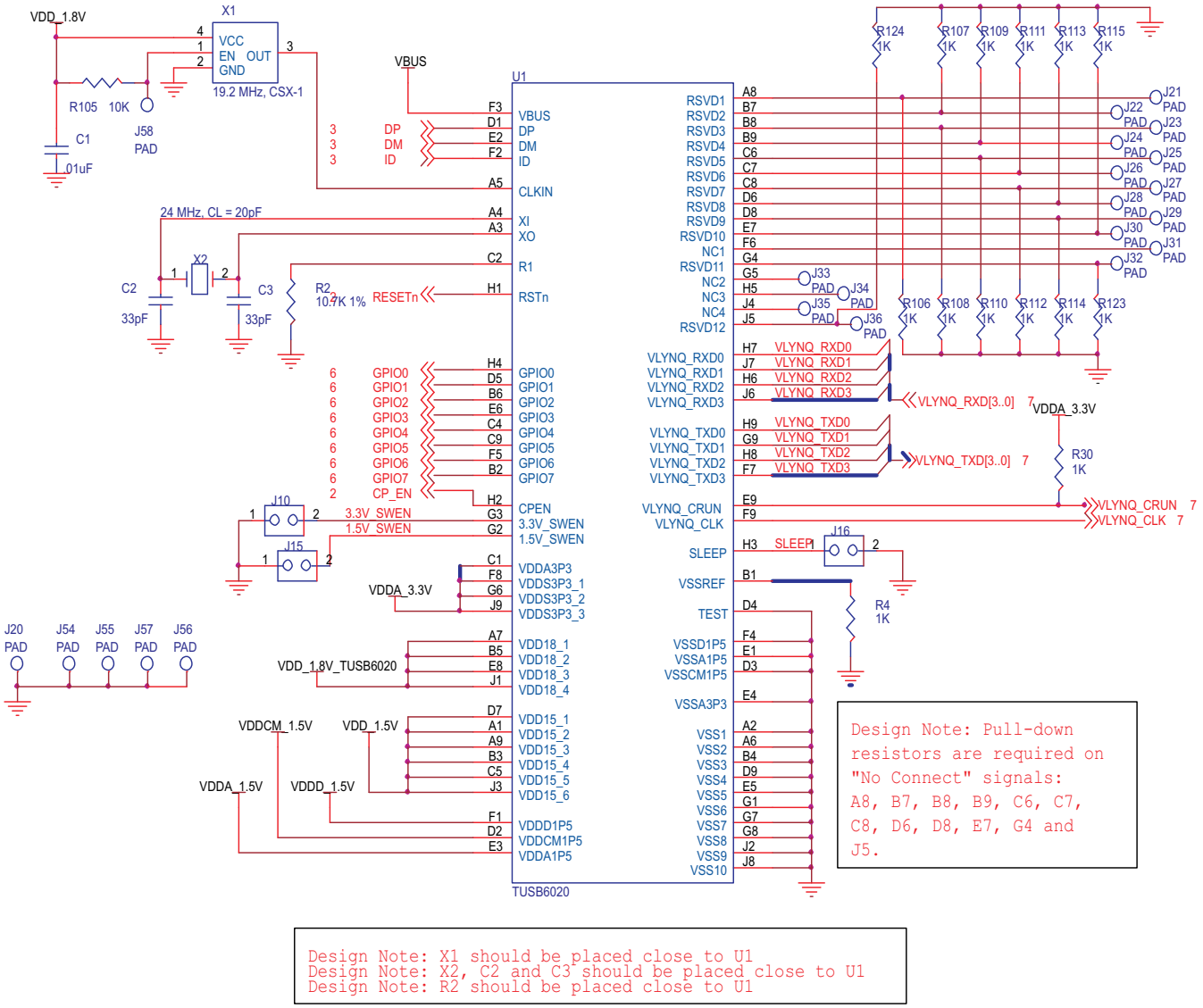


Figure 1-3. TUSB6020

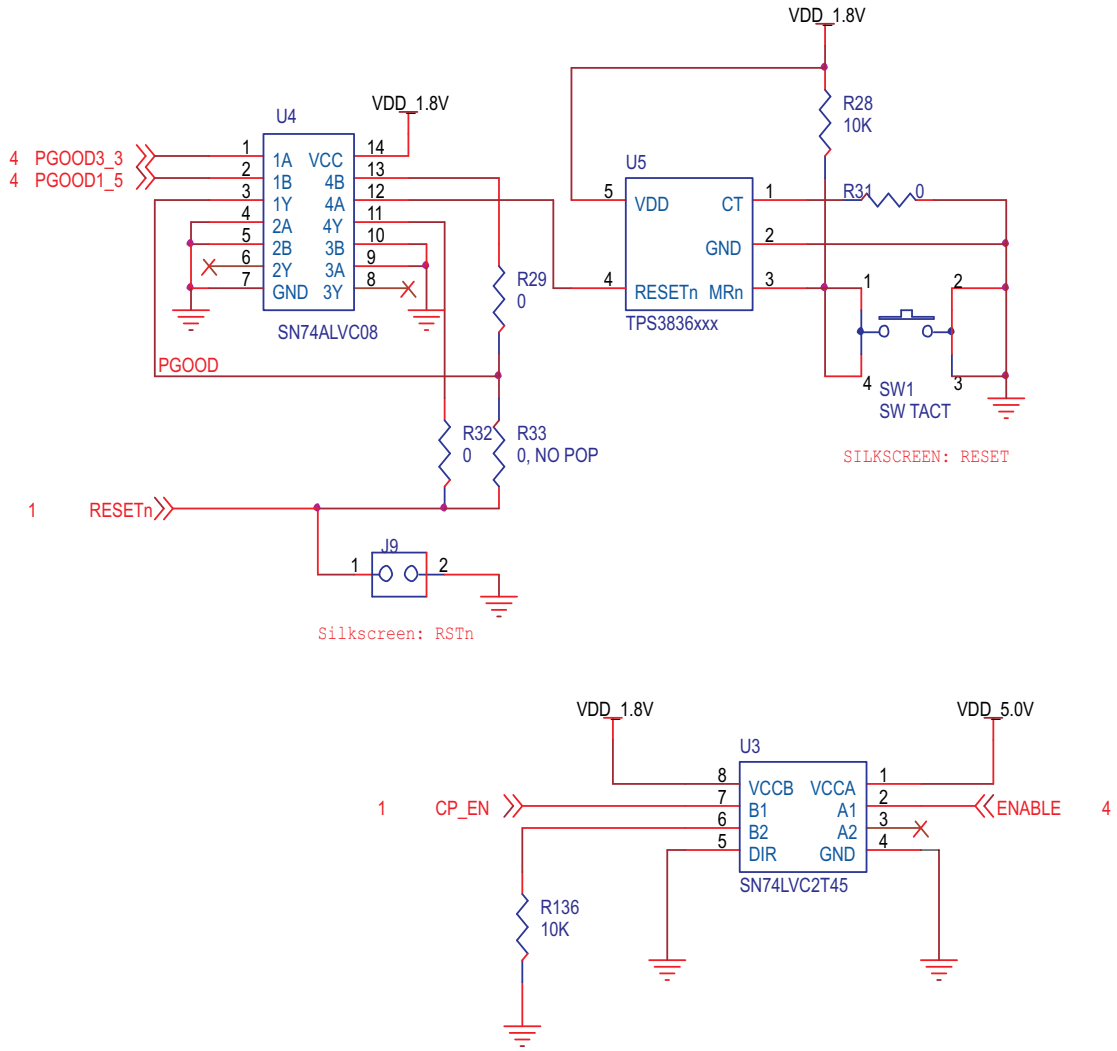
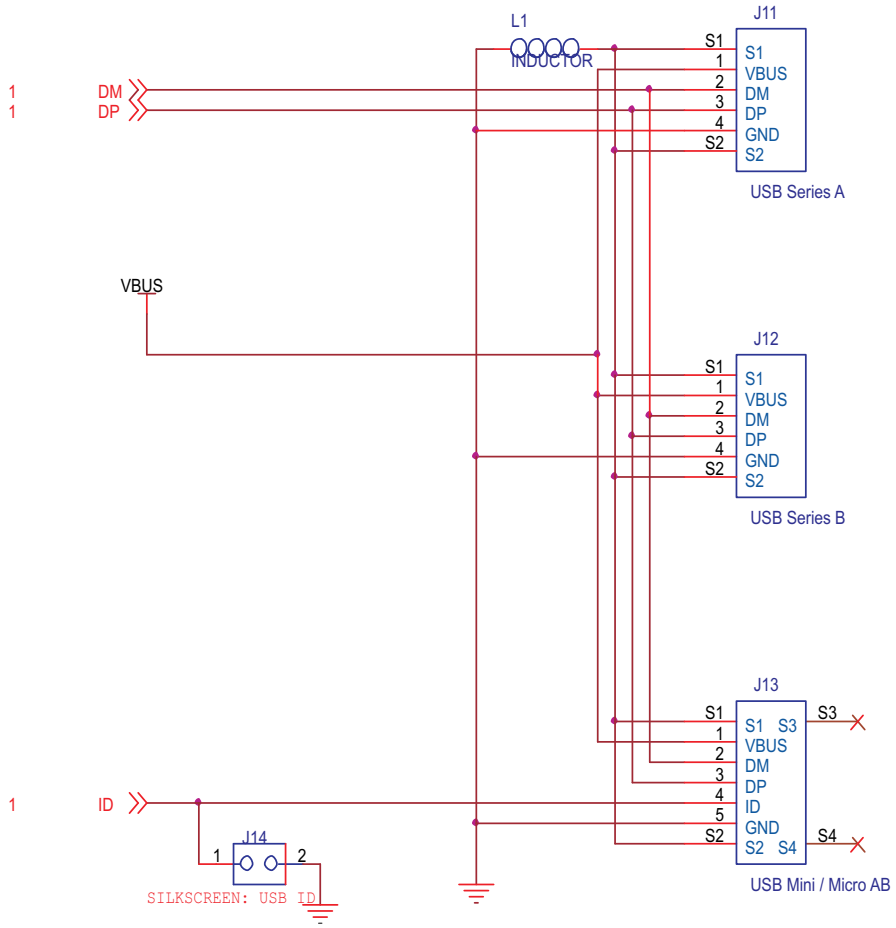
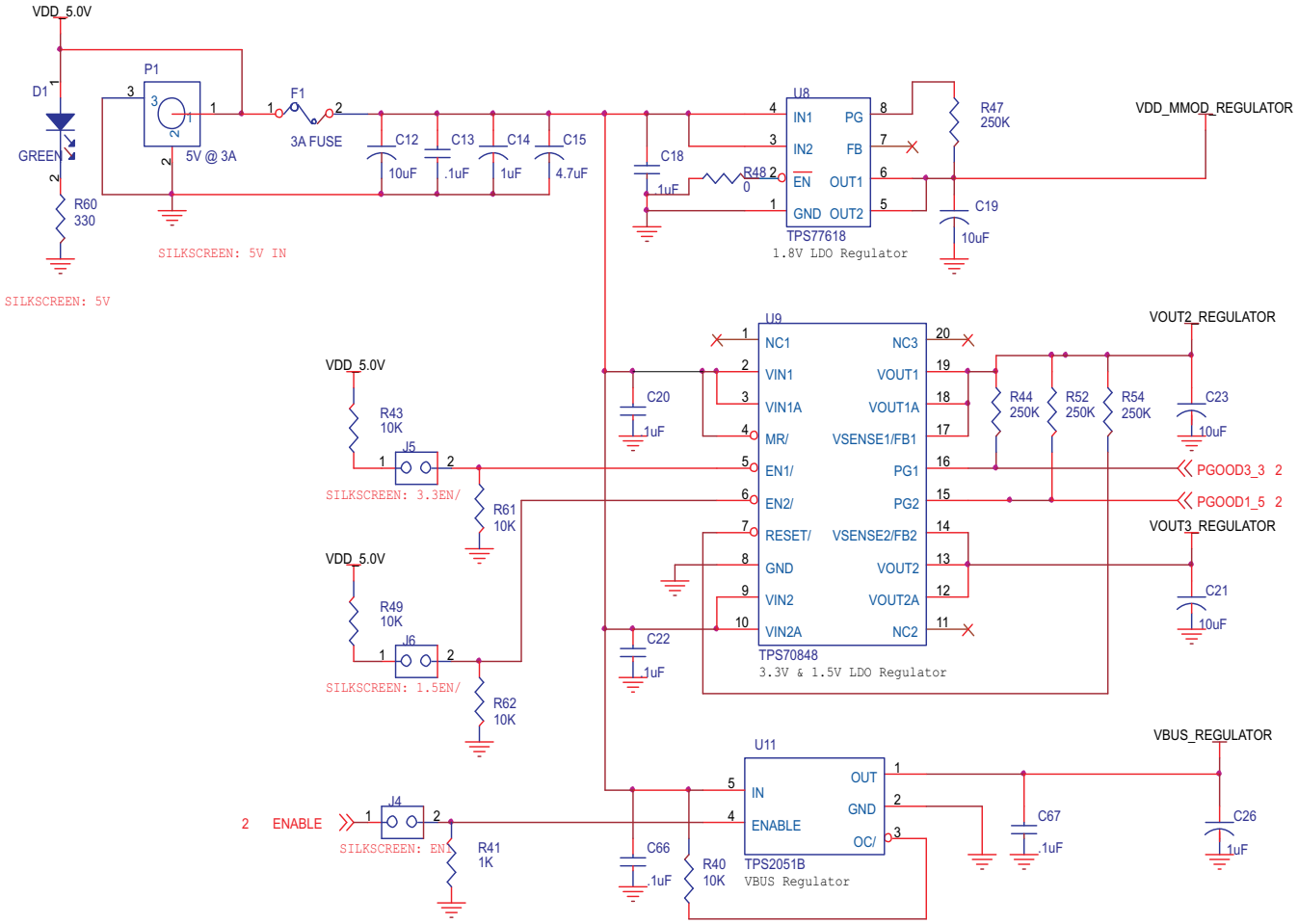


Figure 1-4. Reset



PLACEMENT NOTES: OVERLAP SHORTED USB SERIES A, SERIES B, AND MINI / MICRO AB FOOTPRINTS. ROUTE DP/DM LINES ON TOP LAYER OF BOARD AS 90 OHM DIFFERENTIAL PAIRS. SURROUND DP/DM LINES WITH GROUND PLANE AND GROUND VIAS.

Figure 1-5. USB Connectors



Design Note: J4 should have a default trace run between pins 1 and 2 on the top layer.

Figure 1-6. Voltage Regulators

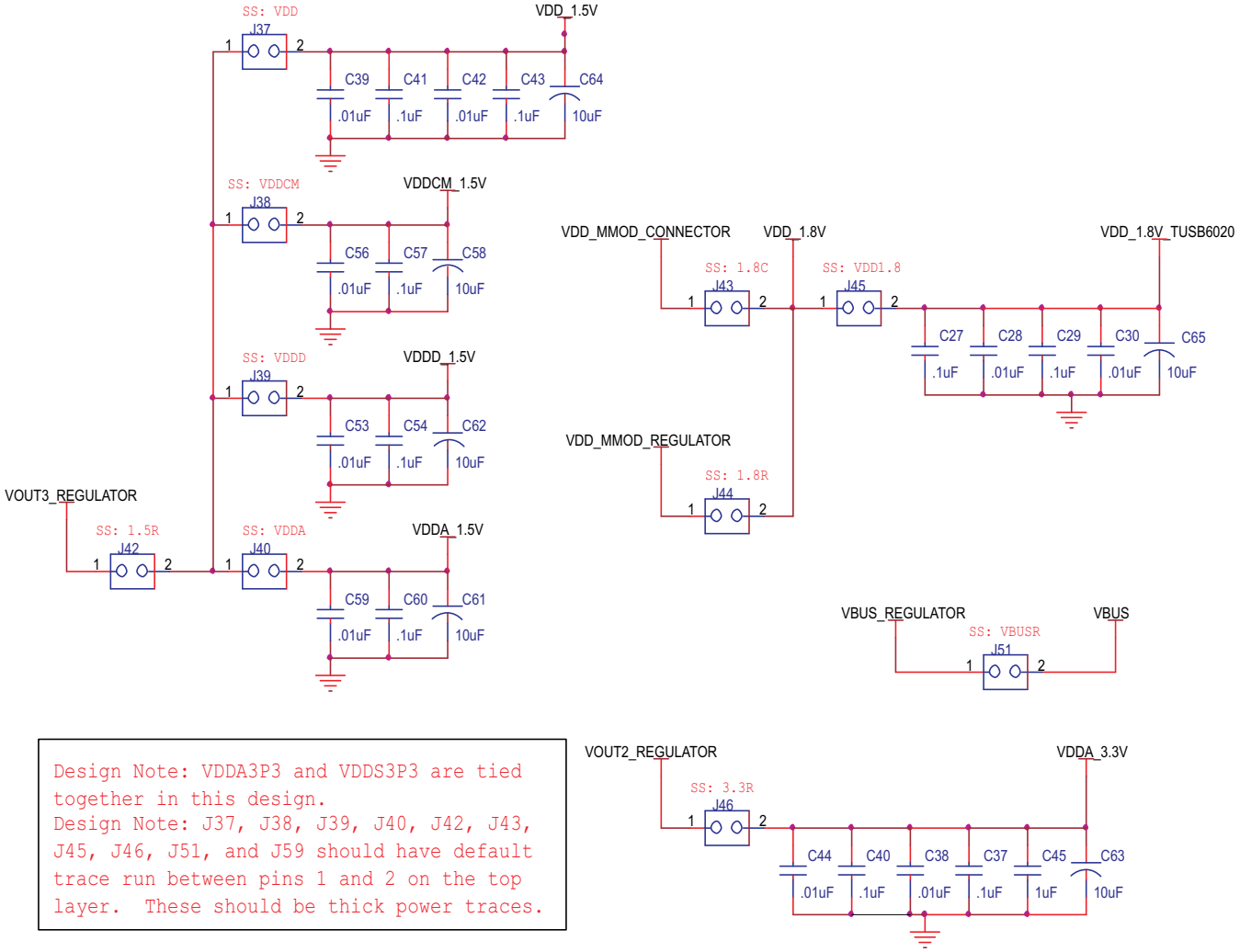


Figure 1-7. Power Jumpers

Design Note: GPIO7 must always be pulled low, directly to ground, for the TUSB6020 to operate properly. GPIO6 can be pulled low to select the XI input, otherwise the TUSB6020 will select the CLKIN as the clock source.

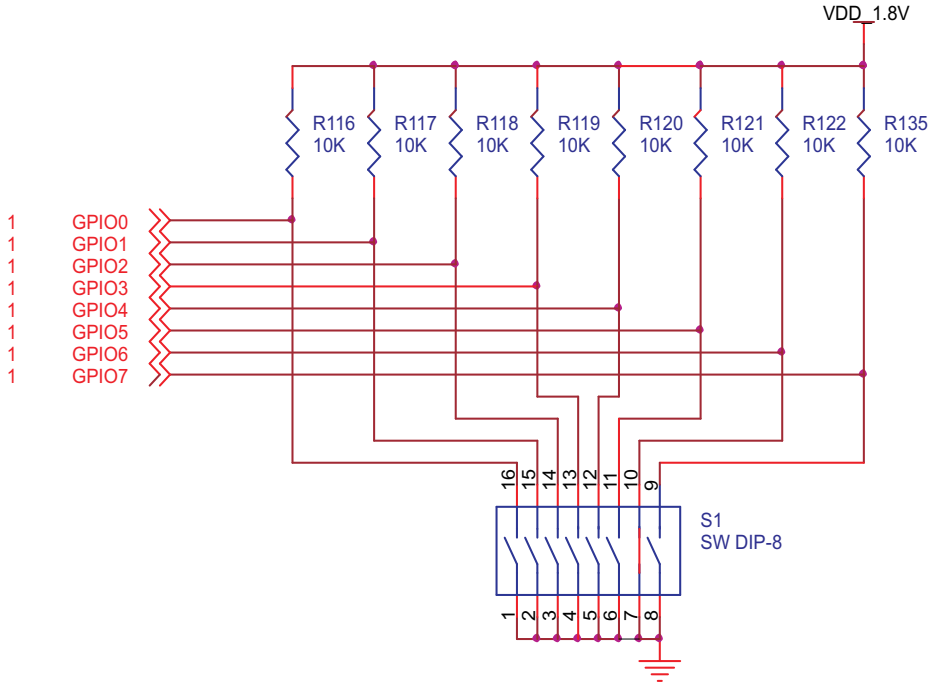


Figure 1-8. GPIO Switches

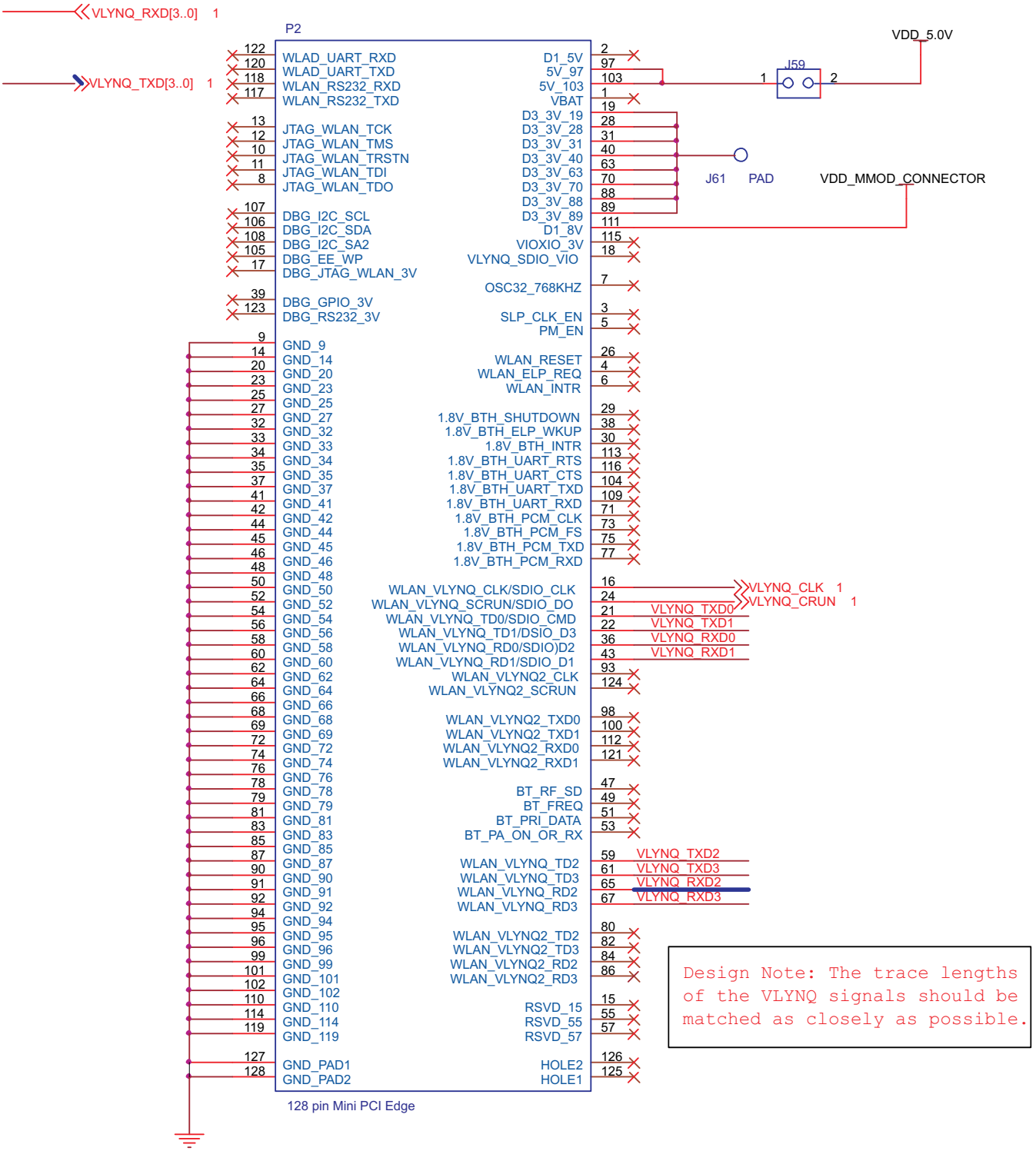


Figure 1-9. Mini PCI Connector

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 5 VDC and the output voltage range of 5 VDC.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than . The EVM is designed to operate properly with certain components above as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
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