

GaAs pHEMT MMIC 0.5 WATT POWER AMPLIFIER, DC - 30 GHz

Typical Applications

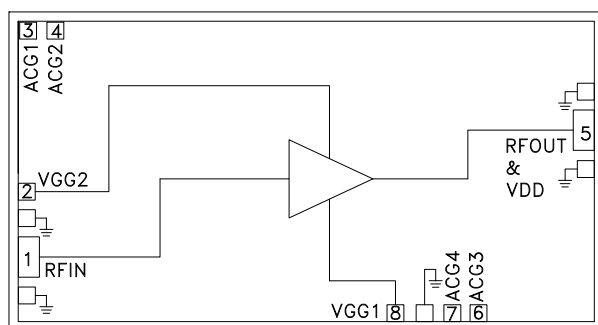
The HMC994A is ideal for:

- Test Instrumentation
- Military & Space
- Fiber Optics

Features

- High P1dB Output Power: 28 dBm
- High Psat Output Power: 30 dBm
- High Gain: 14 dB
- High Output IP3: 39 dBm
- Supply Voltage: +10 V @ 250 mA
- 50 Ohm Matched Input/Output
- Die Size: 2.75 x 1.45 x 0.1 mm

Functional Diagram



General Description

The HMC994A is a GaAs MMIC pHEMT Distributed Power Amplifier which operates between DC and 30 GHz. The amplifier provides 14 dB of gain, +39 dBm output IP3 and +28 dBm of output power at 1 dB gain compression while requiring 250 mA from a +10 V supply. The HMC994A exhibits a slightly positive gain slope from 2 to 20 GHz, making it ideal for EW, ECM, Radar and test equipment applications. With up to 39 dBm Output IP3 the HMC994A is ideal for high linearity applications in military and space as well as test equipment where high order modulations are used. The HMC994A amplifier I/Os are internally matched to 50 Ohms facilitating integration into Multi-Chip-Modules (MCMs). All data is taken with the chip connected via two 0.025 mm (1 mil) wire bonds of minimal length 0.31 mm (12 mils).

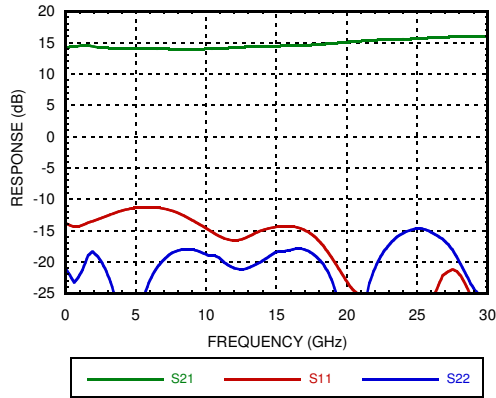
Electrical Specifications, $T_A = +25^\circ\text{C}$, $V_{dd} = +10\text{V}$, $V_{gg2} = +3.5\text{V}$, $I_{dd} = 250\text{mA}^*$

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range	DC - 18			18 - 26			26 - 30			GHz
Gain	11.5	14.5		12	15		12.5	15.5		dB
Gain Flatness		±0.25			±0.5			±0.15		dB
Gain Variation Over Temperature		0.004			0.005			0.01		dB/°C
Input Return Loss		13			22			22		dB
Output Return Loss		20			18			20		dB
Output Power for 1 dB Compression (P1dB)	26	28		26	28		24.5	27.5		dBm
Saturated Output Power (Psat)		30			30			29		dBm
Output Third Order Intercept (IP3) Pout / tone = +16dBm		39			36			36		dBm
Noise Figure		3.5			3			3.5		dB
Supply Current (Idd) (Vdd= 10V, Vgg1= -0.6V Typ.)		250			250			250		mA
Supply Voltage	8	10	11	8	10	11	8	10	11	V

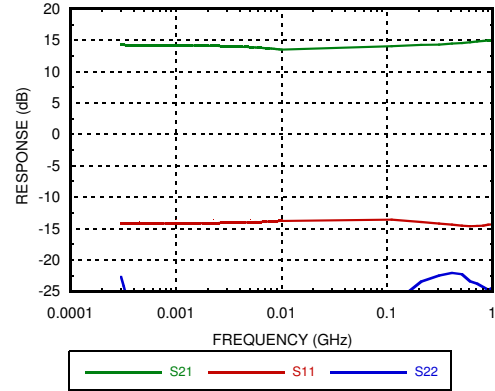
* Adjust Vgg1 between -2 to 0 V to achieve 250 mA typical, Vgg1 typical = -0.6 V

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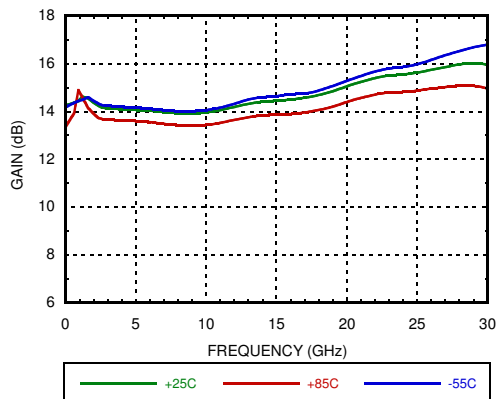
Gain & Return Loss



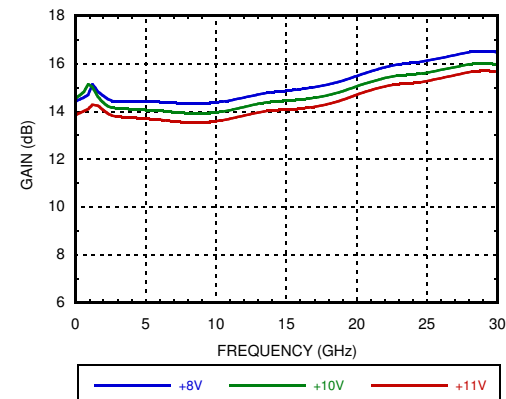
Low Frequency Gain & Return Loss



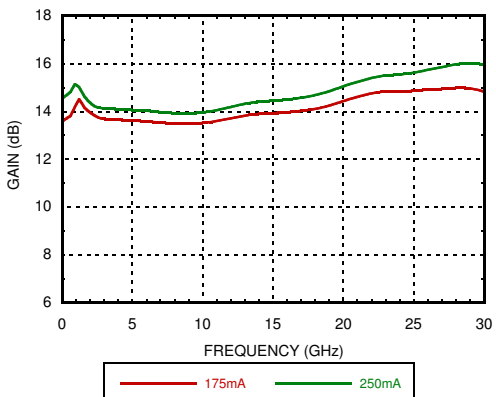
Gain vs. Temperature



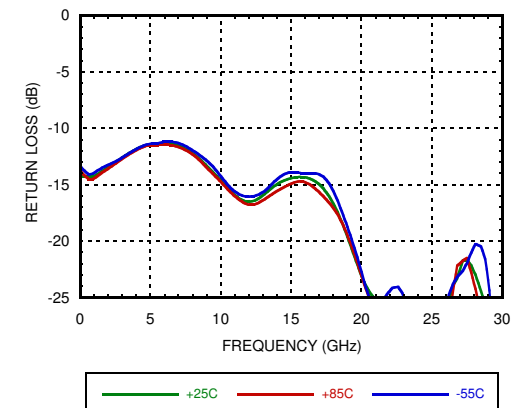
Gain vs. Vdd



Gain vs. Idd



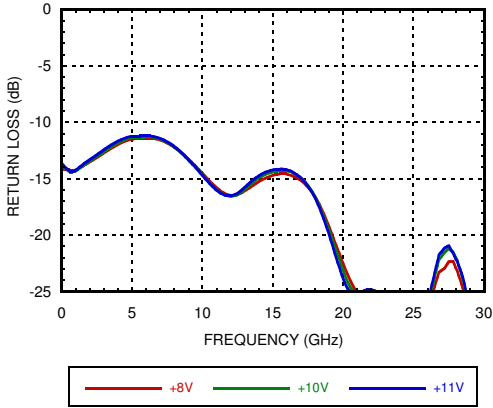
Input Return Loss vs. Temperature



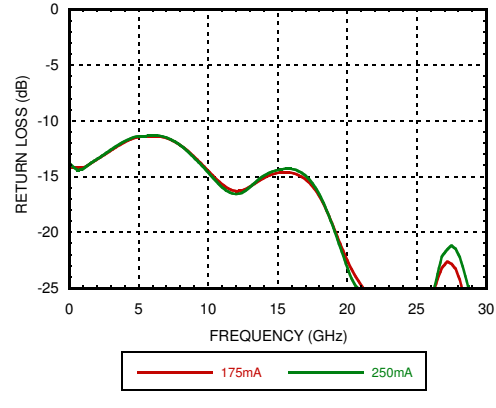
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AMPLIFIERS - LINEAR & POWER - CHIP

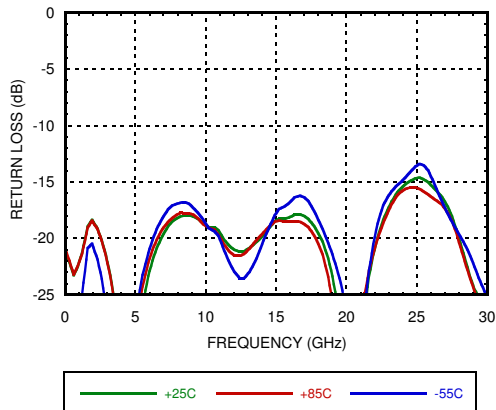
Input Return Loss vs. Vdd



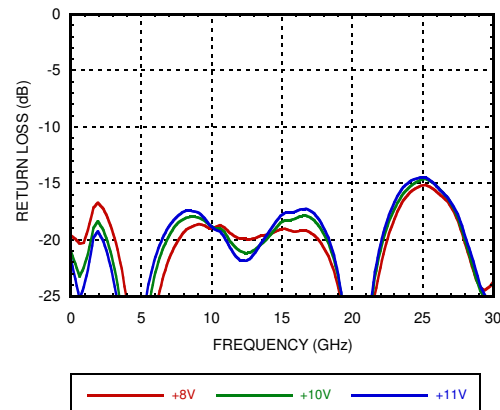
Input Return Loss vs. Idd



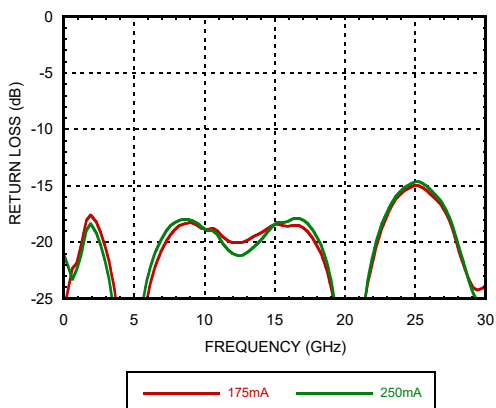
Output Return Loss vs. Temperature



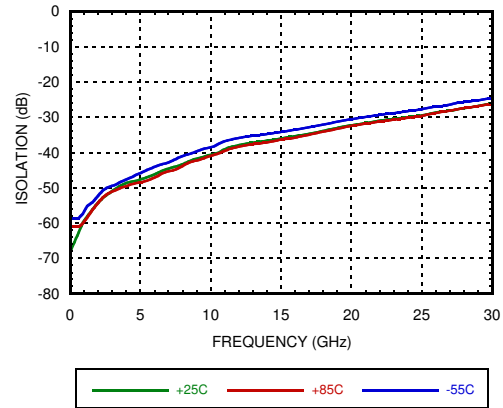
Output Return Loss vs. Vdd



Output Return Loss vs. Idd

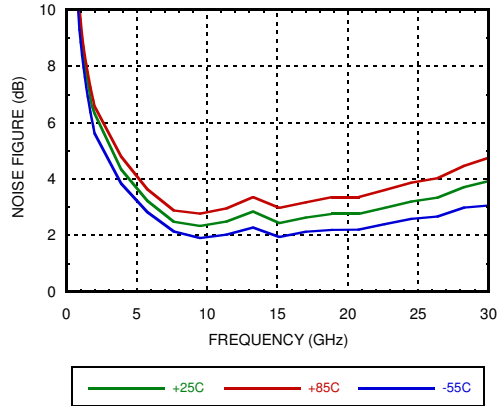


Reverse Isolation vs. Temperature

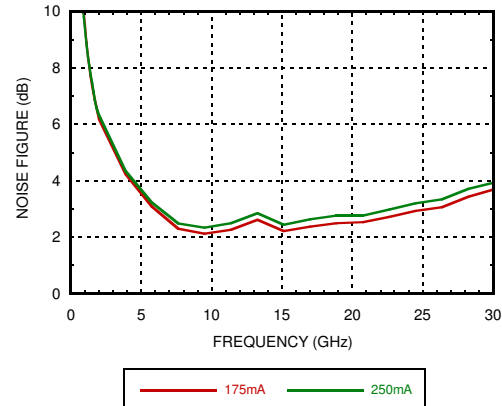


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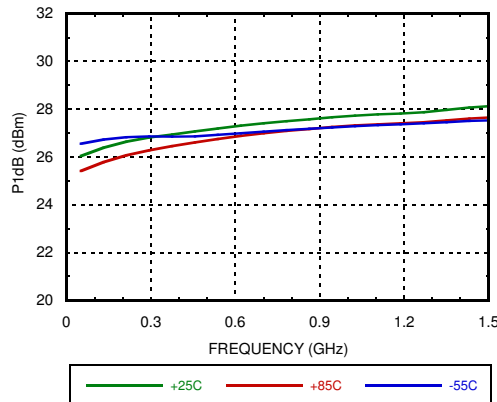
Noise Figure vs. Temperature



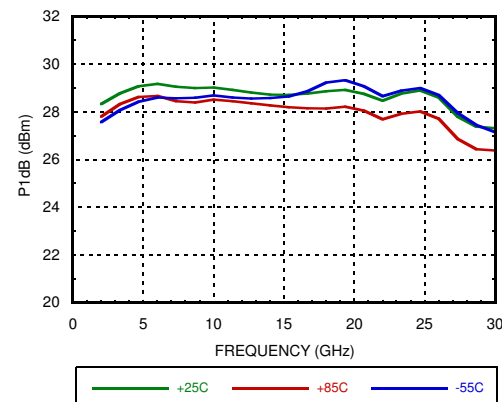
Noise Figure vs Idd



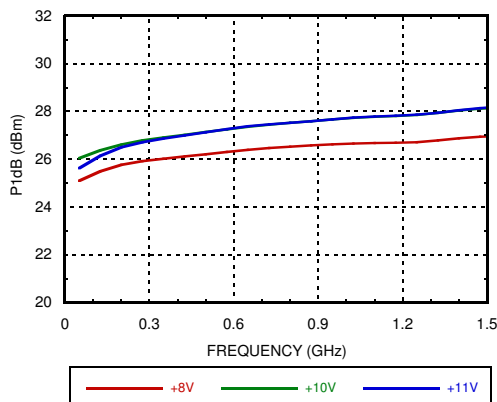
Low Frequency P1dB vs. Temperature



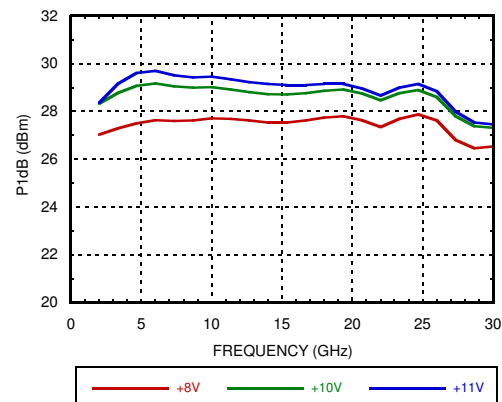
P1dB vs. Temperature



Low Frequency P1dB vs. Vdd

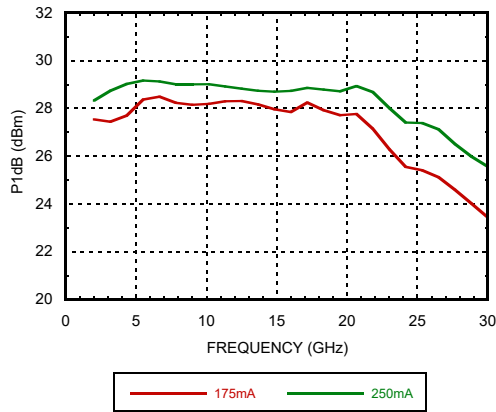


P1dB vs. Vdd

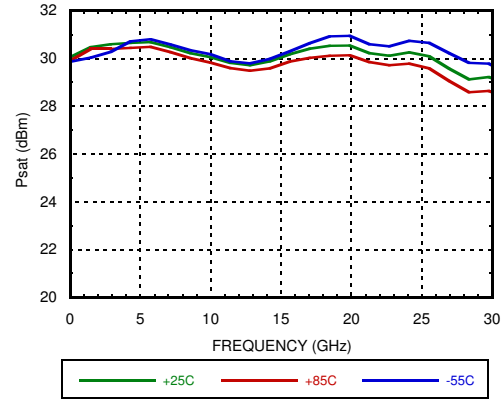


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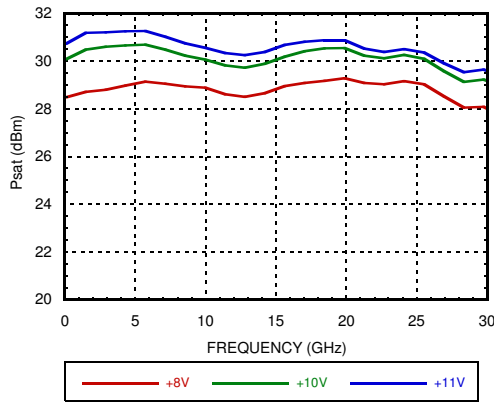
P1dB vs. Idd



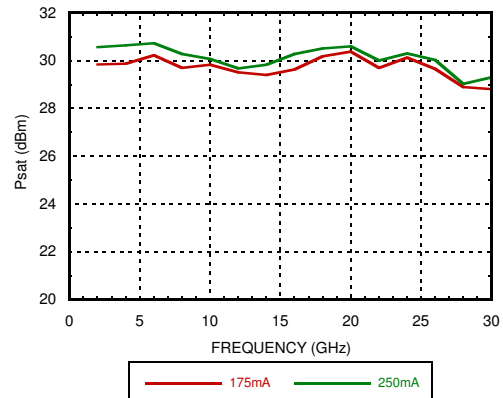
Psat vs Temperature



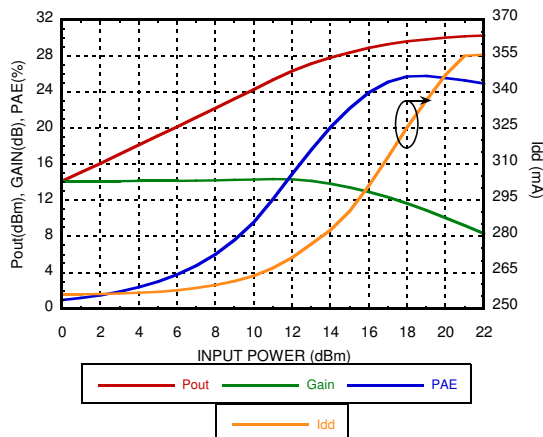
Psat vs. Vdd



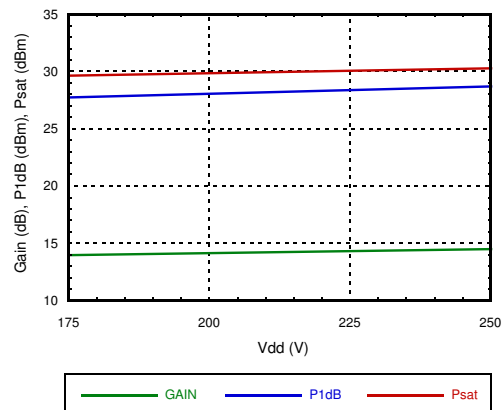
Psat vs Idd



Power Compression @ 16 GHz

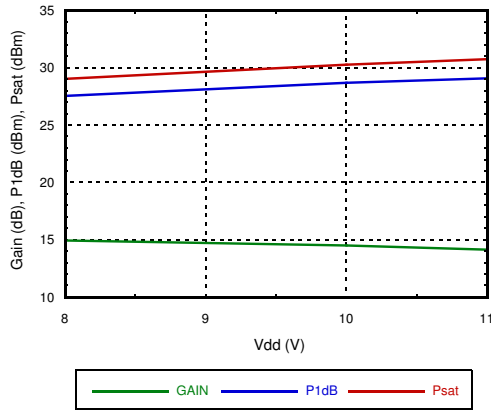


Gain & Power vs. Idd @ 16 GHz

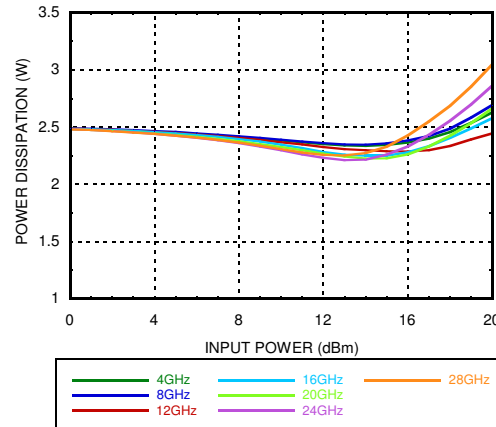


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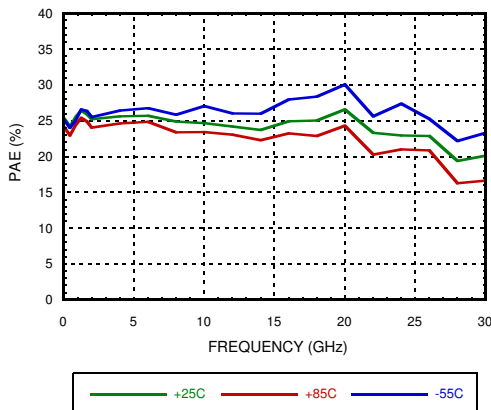
Gain & Power vs Vdd @ 16 GHz



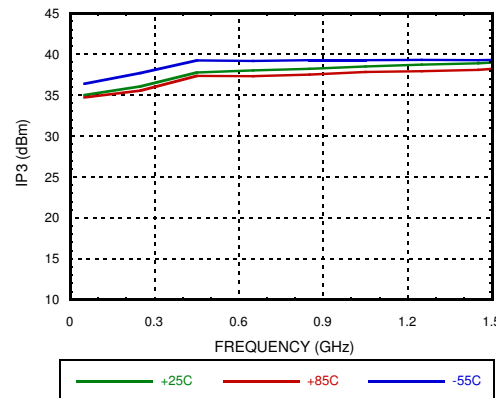
Power Dissipation @ 85C



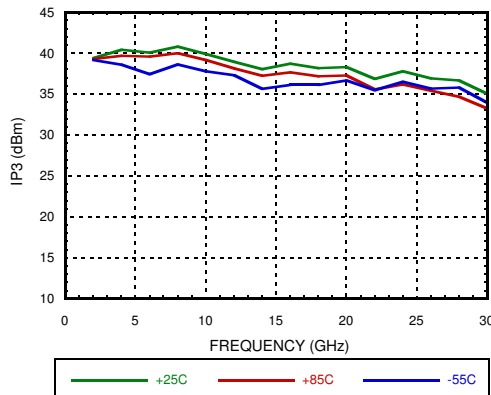
PAE @ Psat vs Temperature



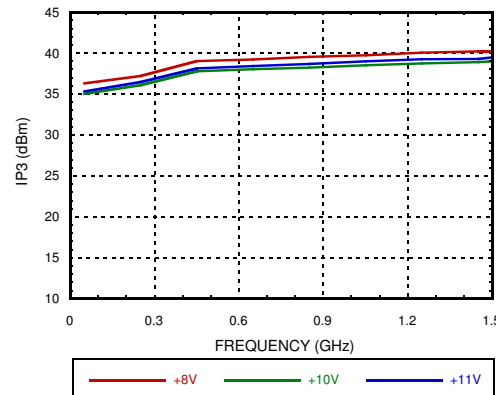
Low Frequency OIP3 vs Temperature @ Pout/tone = +16dBm



OIP3 vs. Temperature @ Pout/tone = +16dBm



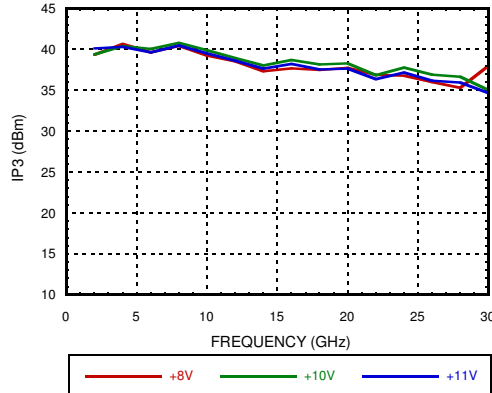
Low Frequency OIP3 vs Vdd @ Pout/tone = +16dBm



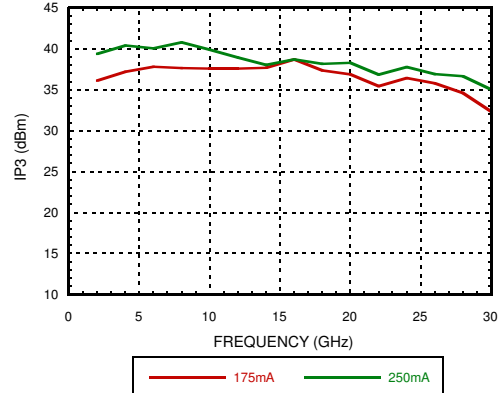
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AMPLIFIERS - LINEAR & POWER - CHIP

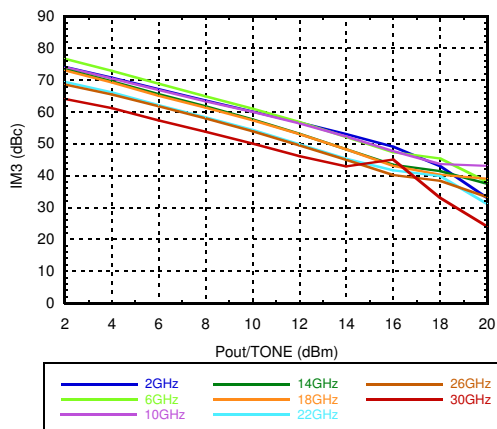
OIP3 vs Vdd
@ Pout/tone = +16dBm



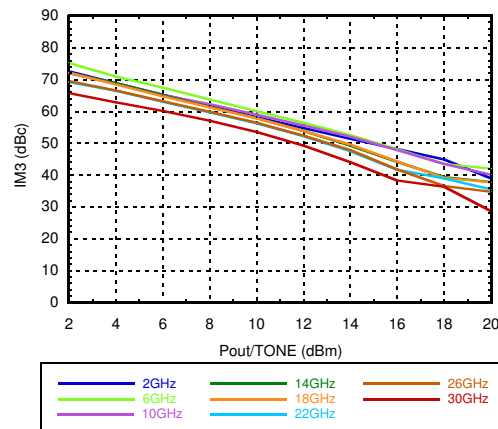
OIP3 vs Idd
@ Pout/tone = +16dBm



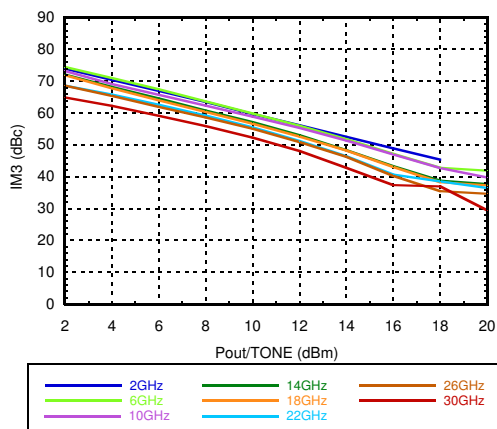
Output IM3 @ Vdd=8V



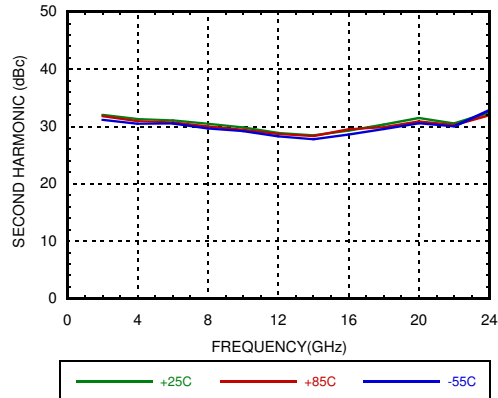
Output IM3 @ Vdd=10V



Output IM3 @ Vdd=11V

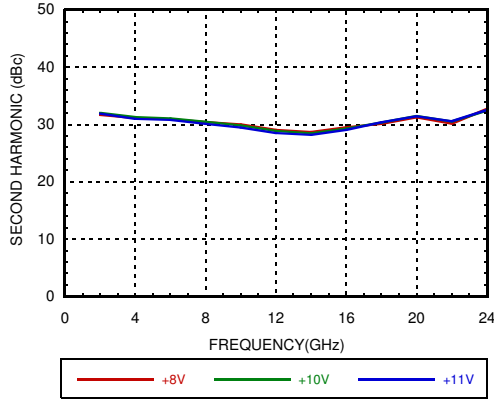


Second Harmonics vs. Temperature
@ Pout = +14 dBm

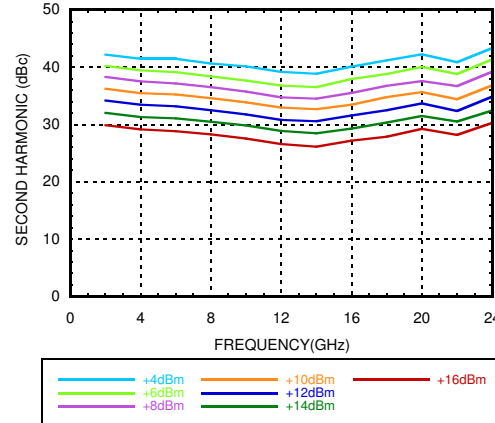


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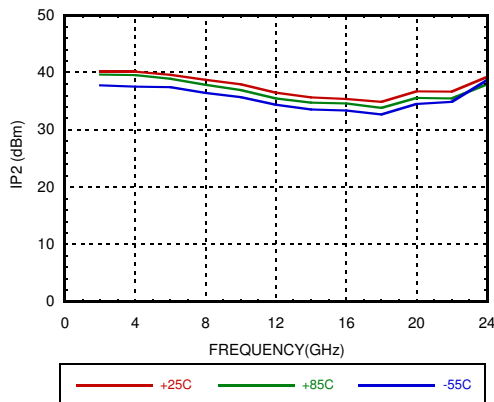
**Second Harmonics vs. Vdd
@ Pout = +14 dBm**



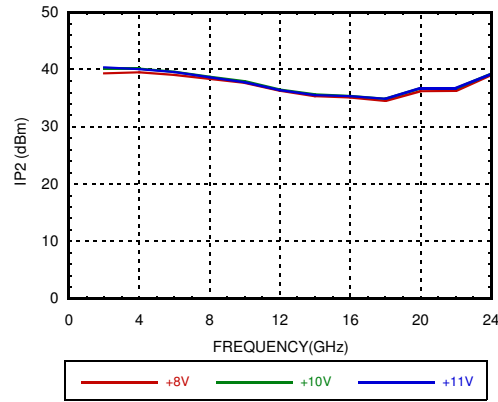
Second Harmonics vs. Pout



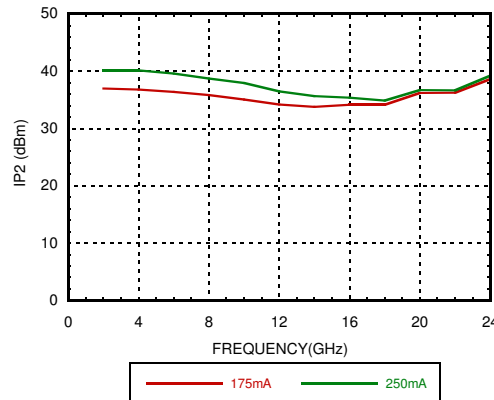
**OIP2 vs. Temperature
@ Pout/tone = +16dBm**



**OIP2 vs. Vdd
@ Pout/tone = +16dBm**

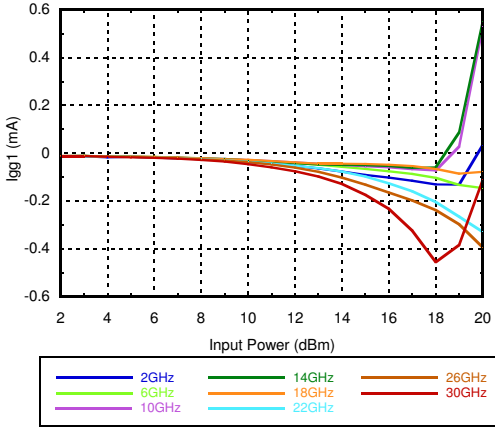


**OIP2 vs. Idd
@ Pout/tone = +16dBm**

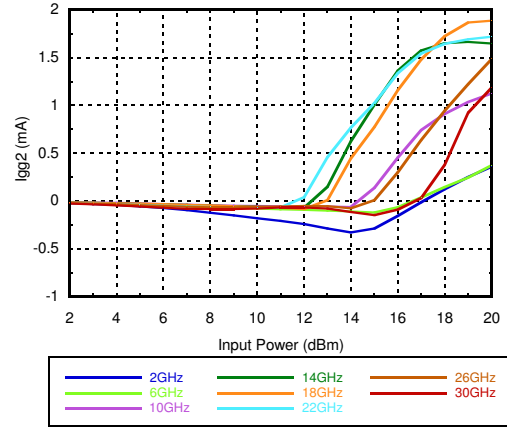


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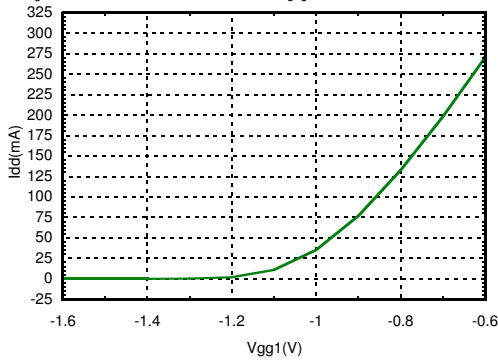
I_{gg1} vs. Input Power



I_{gg2} vs. Input Power



**I_{dd} vs. V_{gg1}
Representative of a Typical Device**



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Absolute Maximum Ratings

Drain Bias Voltage (Vdd)	12V
Gate Bias Voltage (Vgg1)	-3 to 0 Vdc
Gate Bias Voltage (Vgg2)	2.5V min up to (Vdd - 5.5V)
RF Input Power (RFIN)	25 dBm
Output Load VSWR	7:1
Continuous P _{diss} (T= 85 °C) (derate 40.3 mW/°C above 85 °C)	3.62 W
Storage Temperature	-65 to 150 °C
Operating Temperature	-55 to 85 °C
ESD Sensitivity (HBM)	Class 0B - Passed 150V

Reliability Information

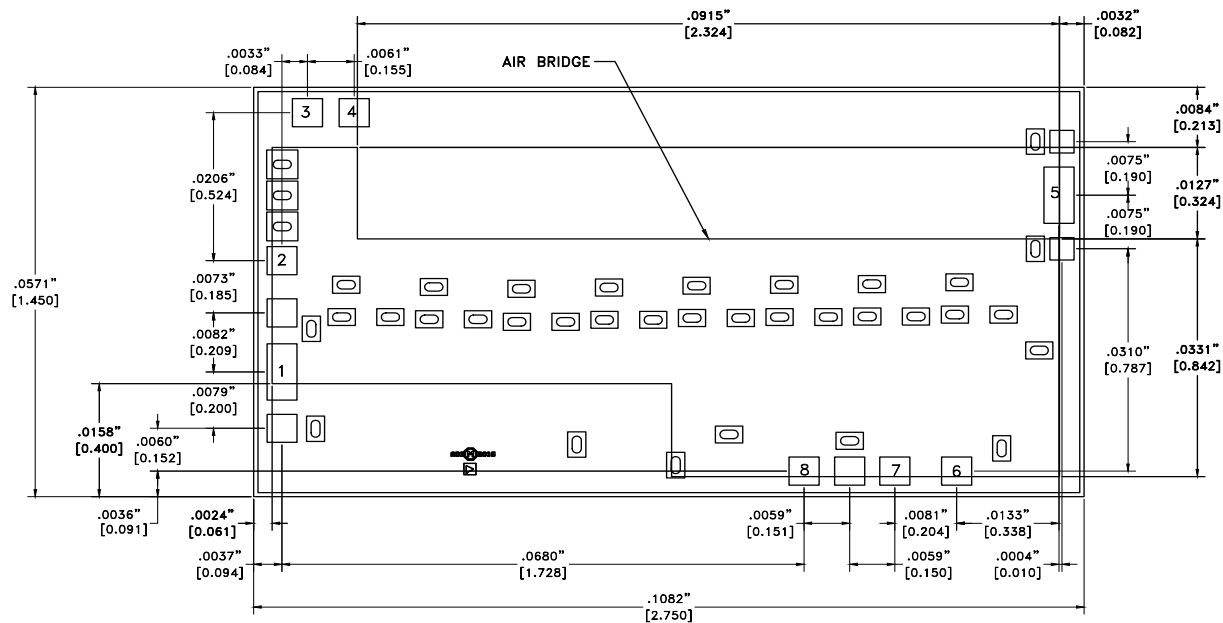
Channel Temperature to Maintain 1 Million Hour MTTF	175 °C
Thermal Resistance (channel to die bottom)	24.8 °C/W

Stresses at or above those listed in the Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating condition for extended periods may affect product reliability.

Outline Drawing



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS



Die Packaging Information [1]

Standard	Alternate
GP-1 (Gel Pack)	[2]

[1] Refer to the "Packaging Information" section on our website for die packaging dimensions.

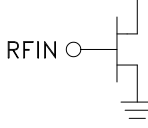
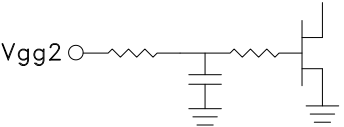
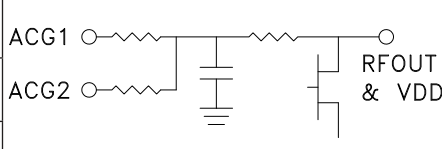
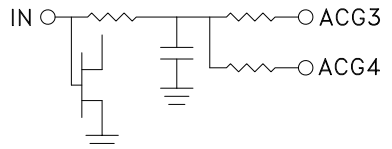
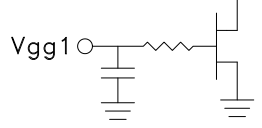

[2] For alternate packaging information contact Analog Devices Inc.

NOTES:

- ALL DIMENSIONS IN INCHES [MILLIMETERS]
- DIE THICKNESS IS 0.004 (0.100)
- TYPICAL BOND PAD IS 0.004 (0.100) SQUARE
- BOND PAD METALIZATION: GOLD
- BACKSIDE METALLIZATION: GOLD
- BACKSIDE METAL IS GROUND
- NO CONNECTION REQUIRED FOR UNLABELED BOND PADS
- OVERALL DIE SIZE IS ±.002

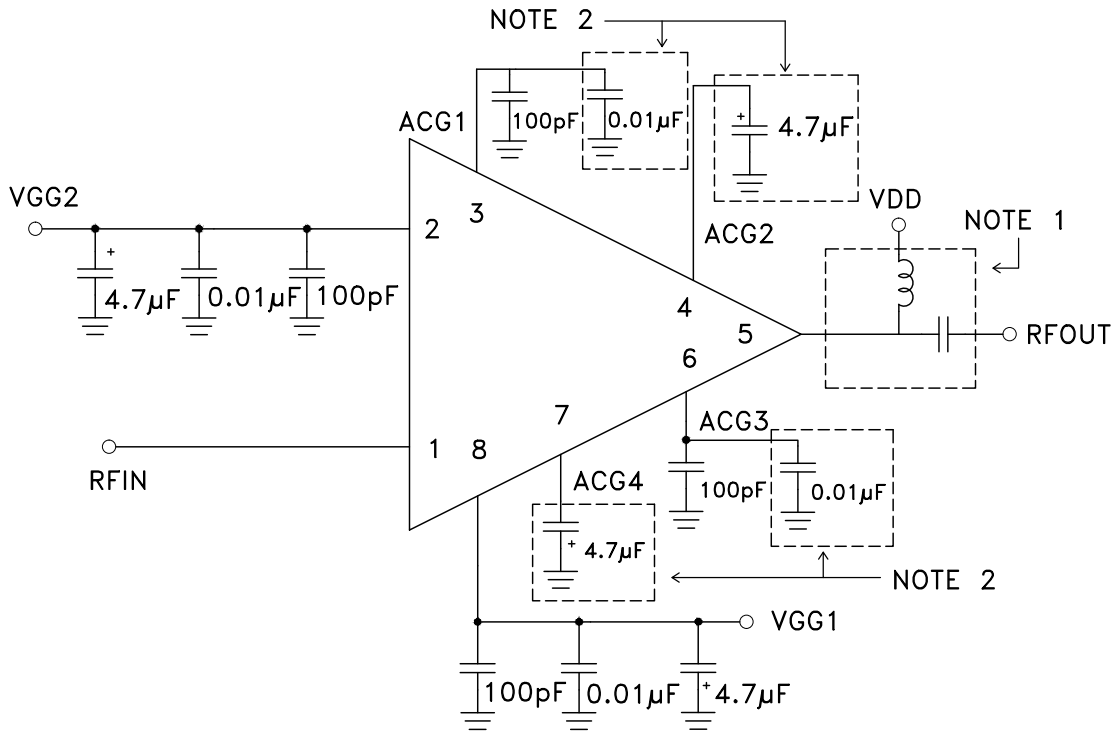
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Pad Descriptions

Pad Number	Function	Description	Interface Schematic
1	RFIN	This pad is DC coupled and matched to 50 Ohms. Blocking capacitor is required.	
2	VGG2	Gate control 2 for amplifier. Attach bypass capacitors per application circuit herein. For nominal operation +3.5V should be applied to Vgg2.	
3	ACG1	Low frequency termination. Attach bypass capacitor per application circuit herein.	
4	ACG2	Low frequency termination. Attach bypass capacitor per application circuit herein.	
5	RFOUT & VDD	RF output for amplifier. Connect DC bias (Vdd) network to provide drain current (Idd). See application circuit herein.	
6	ACG3	Low frequency termination. Attach bypass capacitors per application circuit herein.	
7	ACG4	Low frequency termination. Attach bypass capacitors per application circuit herein.	
8	VGG1	Gate control 1 for amplifier. Attach bypass capacitor per application circuit herein. Please follow "MMIC Amplifier Biasing Procedure" application note.	
Die Bottom	GND	Die bottom must be connected to RF/DC ground.	

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Application Circuit



NOTE 1: Drain Bias (Vdd) must be applied through a broadband bias tee with low series resistance and capable of providing 500 mA.

NOTE 2: Optional capacitors to be used if part is to be operated below 200MHz.

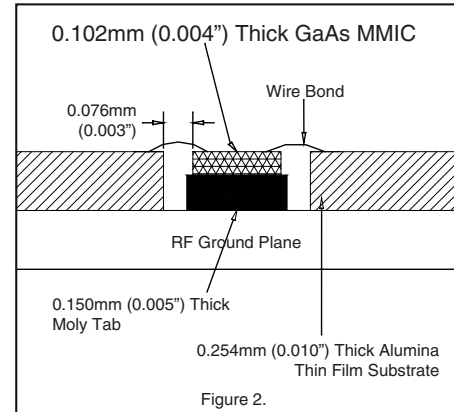
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Mounting & Bonding Techniques for Millimeterwave GaAs MMICs

The die should be attached directly to the ground plane eutectically or with conductive epoxy (see HMC general Handling, Mounting, Bonding Note).

50 Ohm Microstrip transmission lines on 0.127mm (5 mil) thick alumina thin film substrates are recommended for bringing RF to and from the chip (Figure 1). If 0.254mm (10 mil) thick alumina thin film substrates must be used, the die should be raised 0.150mm (6 mils) so that the surface of the die is coplanar with the surface of the substrate. One way to accomplish this is to attach the 0.102mm (4 mil) thick die to a 0.150mm (6 mil) thick molybdenum heat spreader (moly-tab) which is then attached to the ground plane (Figure 2).

Microstrip substrates should be placed as close to the die as possible in order to minimize bond wire length. Typical die-to-substrate spacing is 0.076mm to 0.152 mm (3 to 6 mils).



Handling Precautions

Follow these precautions to avoid permanent damage.

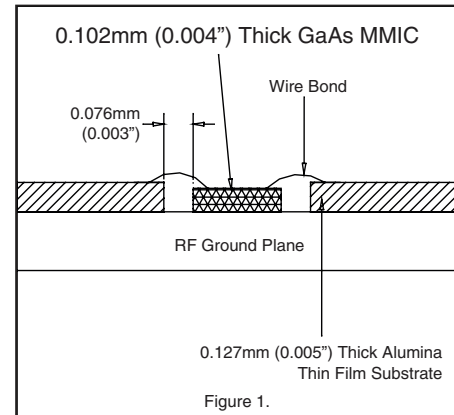
Storage: All bare die are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

Static Sensitivity: Follow ESD precautions to protect against ESD strikes.

Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.

General Handling: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip may have fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.



Mounting

The chip is back-metallized and can be die mounted with AuSn eutectic preforms or with electrically conductive epoxy. The mounting surface should be clean and flat.

Eutectic Die Attach: A 80/20 gold tin preform is recommended with a work surface temperature of 255 °C and a tool temperature of 265 °C. When hot 90/10 nitrogen/hydrogen gas is applied, tool tip temperature should be 290 °C. DO NOT expose the chip to a temperature greater than 320 °C for more than 20 seconds. No more than 3 seconds of scrubbing should be required for attachment.

Epoxy Die Attach: Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's schedule.

Wire Bonding

RF bonds made with two 1 mil wires are recommended. These bonds should be thermosonically bonded with a force of 40-60 grams. DC bonds of 0.001" (0.025 mm) diameter, thermosonically bonded, are recommended. Ball bonds should be made with a force of 40-50 grams and wedge bonds at 18-22 grams. All bonds should be made with a nominal stage temperature of 150 °C. A minimum amount of ultrasonic energy should be applied to achieve reliable bonds. All bonds should be as short as possible, less than 12 mils (0.31 mm).