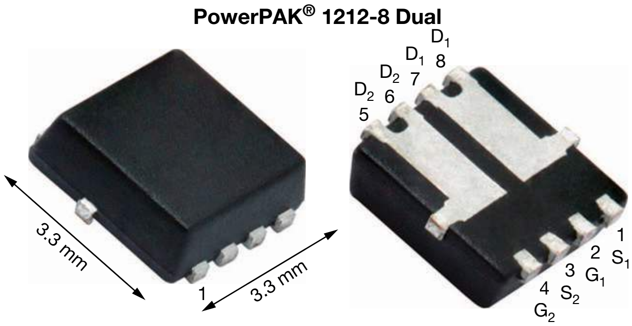
Dual N-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	**$R_{DS(on)}$ (Ω)**	**I_D (A)**	**Q_g (TYP.)**
20	0.0164 at V_{GS} = 4.5 V	25 [f]	12 nC
	0.0200 at V_{GS} = 2.5 V	25 [f]	
	0.0240 at V_{GS} = 1.8 V	24.6	

PowerPAK® 1212-8 Dual



Top View   Bottom View

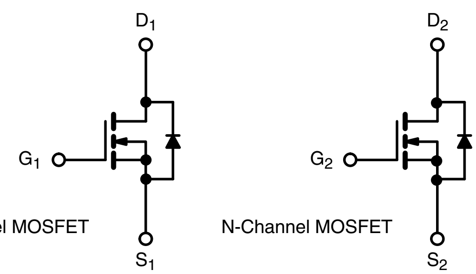
FEATURES

- TrenchFET® power MOSFET
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- DC/DC
- Notebook system power
- POL



N-Channel MOSFET   N-Channel MOSFET

Ordering Information:
Si7232DN-T1-GE3 (Lead (Pb)-free and halogen-free)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	25 [f]	A
	T_C = 70 °C		23.8	
	T_A = 25 °C		10 [a, b]	
	T_A = 70 °C		8 [a, b]	
Pulsed Drain Current		I_{DM}	40	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	19	
	T_A = 25 °C		2.2 [a, b]	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	15	
Single Pulse Avalanche Energy		E_{AS}	11	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	23	W
	T_C = 70 °C		14.8	
	T_A = 25 °C		2.6 [a, b]	
	T_A = 70 °C		1.7 [a, b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150	°C
Soldering Recommendations (Peak Temperature) [c, d]			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		**SYMBOL**	**TYPICAL**	**MAXIMUM**	**UNIT**
Maximum Junction-to-Ambient [a, e]	t ≤ 10 s	R_{thJA}	38	48	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	4.3	5.4	

Notes
a. Surface mounted on 1" x 1" FR4 board.
b. t = 10 s.
c. See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
e. Maximum under steady state conditions is 94 °C/W.
f. Package limited.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	20	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA	-	22	-	mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		-	-3	-	
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 250 µA	0.4	-	1	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55 °C	-	-	10	
On-State Drain Current [a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	20	-	-	A
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 10 A	-	0.0135	0.0164	Ω
		V_{GS} = 2.5 V, I_D = 9 A	-	0.0160	0.0200	
		V_{GS} = 1.8 V, I_D = 8.2 A	-	0.0190	0.0240	
Forward Transconductance [a]	g_{fs}	V_{DS} = 10 V, I_D = 10 A	-	47	-	S
Dynamic [b]						
Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	-	1220	-	pF
Output Capacitance	C_{oss}		-	180	-	
Reverse Transfer Capacitance	C_{rss}		-	80	-	
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 8 V, I_D = 10 A	-	21	32	nC
		V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 10 A	-	12	18	
Gate-Source Charge	Q_{gs}		-	2	-	
Gate-Drain Charge	Q_{gd}		-	1.3	-	
Gate Resistance	R_g	f = 1 MHz	-	1.8	3.6	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 1.25 Ω $I_D \cong$ 8 A, V_{GEN} = 4.5 V, R_g = 1 Ω	-	10	15	ns
Rise Time	t_r		-	10	15	
Turn-Off Delay Time	$t_{d(off)}$		-	35	55	
Fall Time	t_f		-	10	15	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 1.25 Ω $I_D \cong$ 8 A, V_{GEN} = 8 V, R_g = 1 Ω	-	10	15	
Rise Time	t_r		-	10	15	
Turn-Off Delay Time	$t_{d(off)}$		-	25	40	
Fall Time	t_f		-	10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C	-	-	19	A
Pulse Diode Forward Current	I_{SM}		-	-	40	
Body Diode Voltage	V_{SD}	I_S = 8 A, V_{GS} = 0 V	-	0.81	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 8 A, dI/dt = 100 A/µs, T_J = 25 °C	-	20	30	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	15	25	nC
Reverse Recovery Fall Time	t_a		-	12.5	-	ns
Reverse Recovery Rise Time	t_b		-	7.5	-	

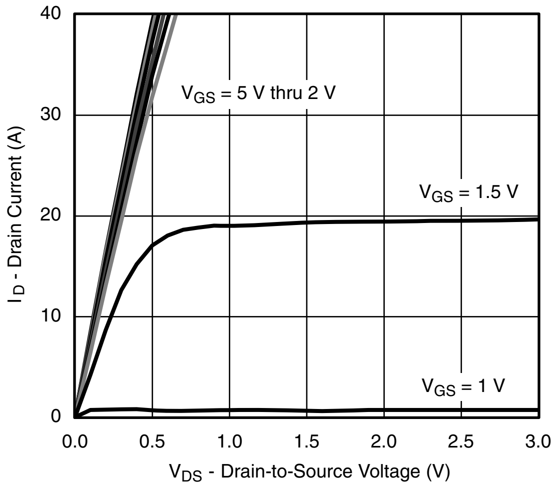
Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

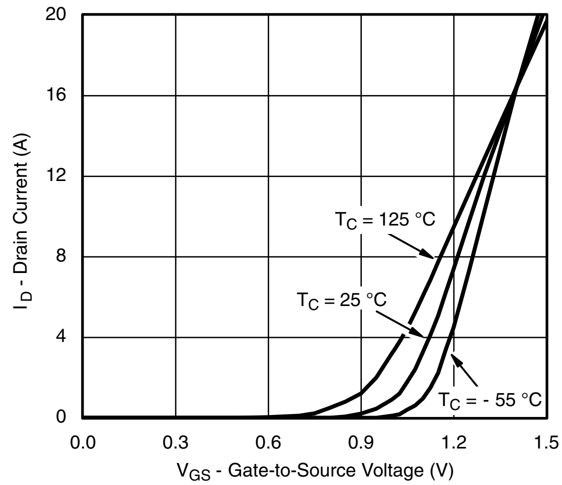
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

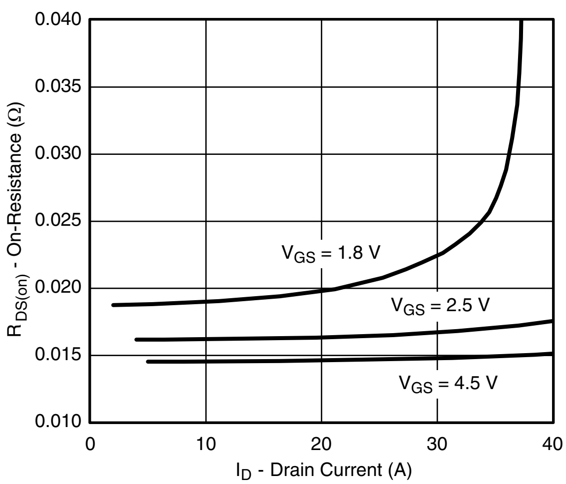
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



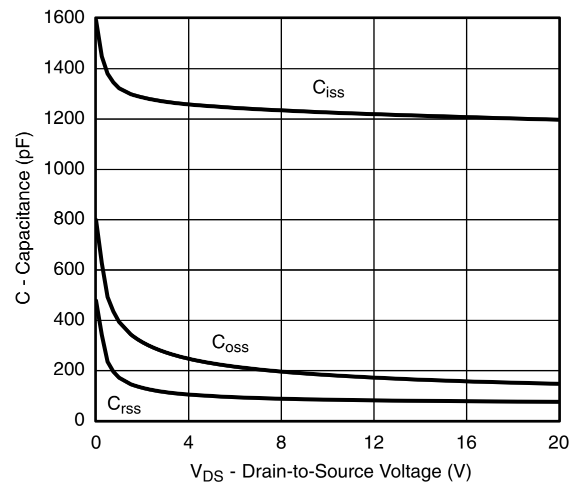
Output Characteristics



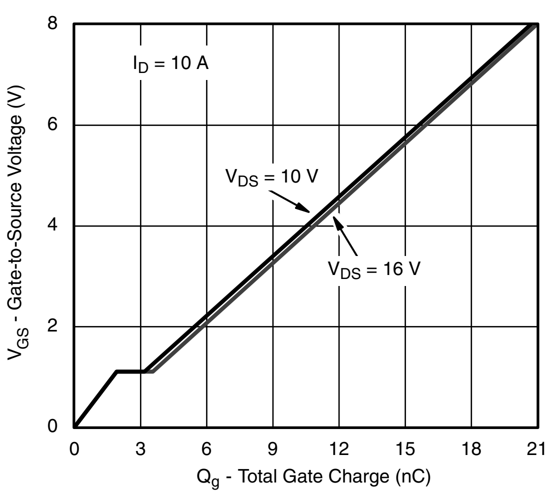
Transfer Characteristics



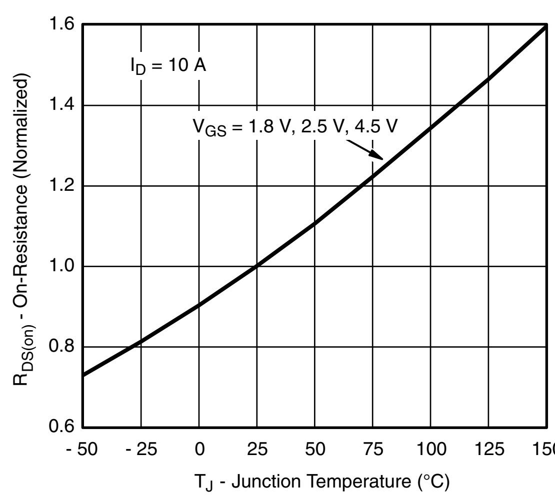
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

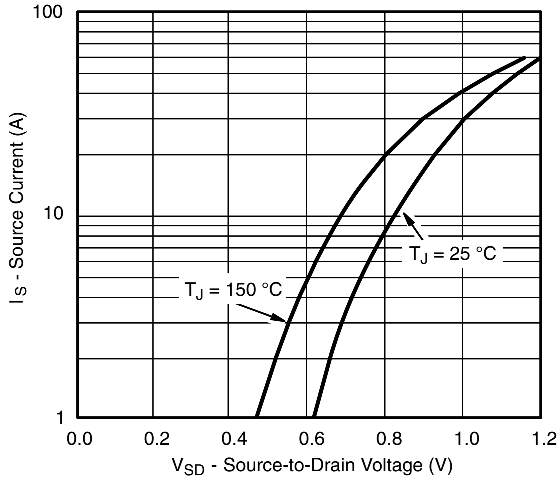


Gate Charge

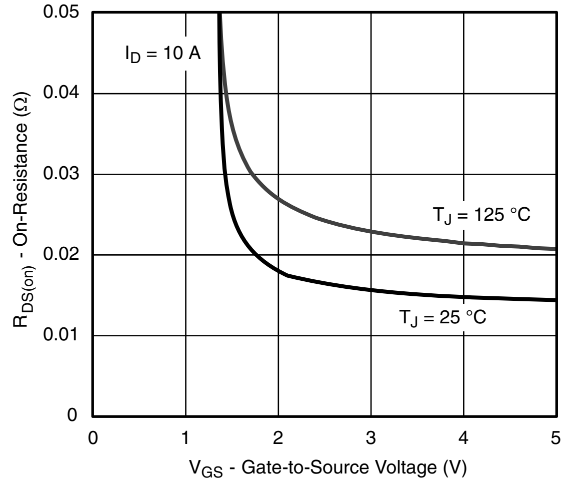


On-Resistance vs. Junction Temperature

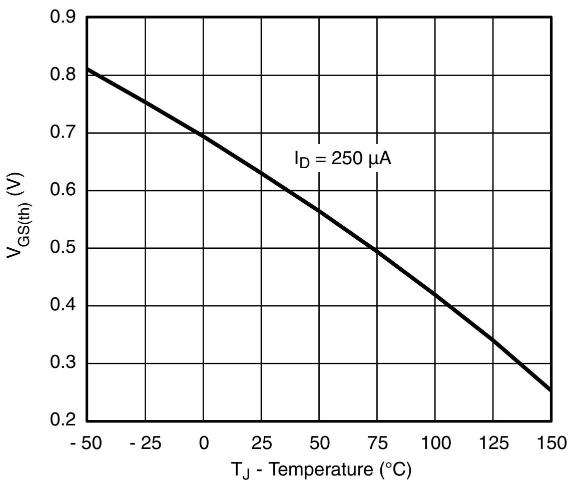
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



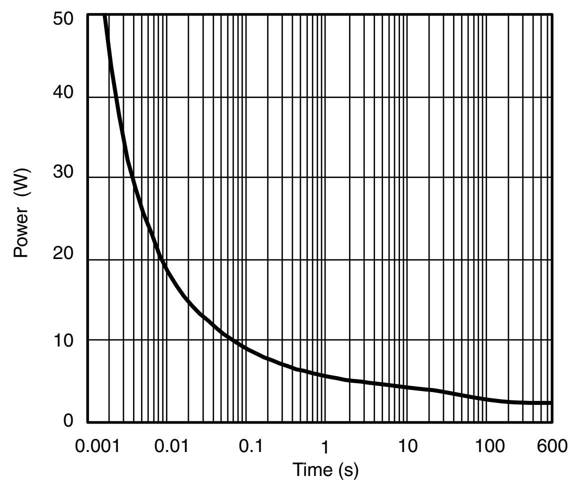
Source-Drain Diode Forward Voltage



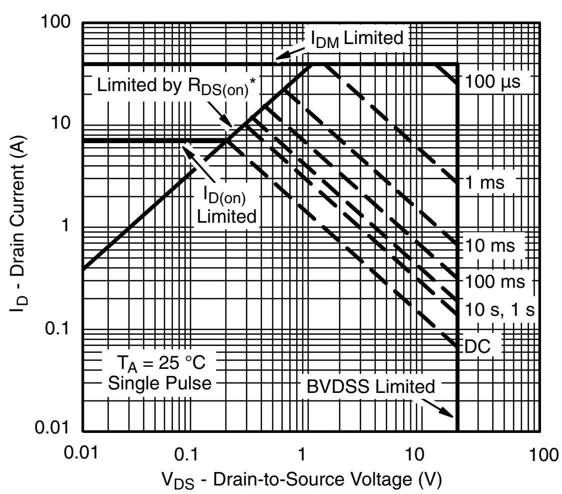
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



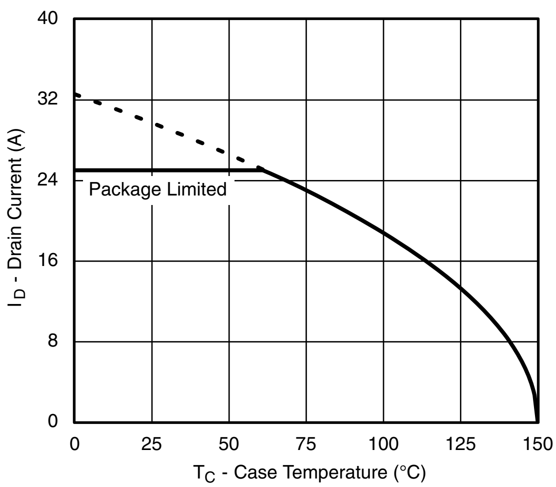
Single Pulse Power, Junction-to-Ambient



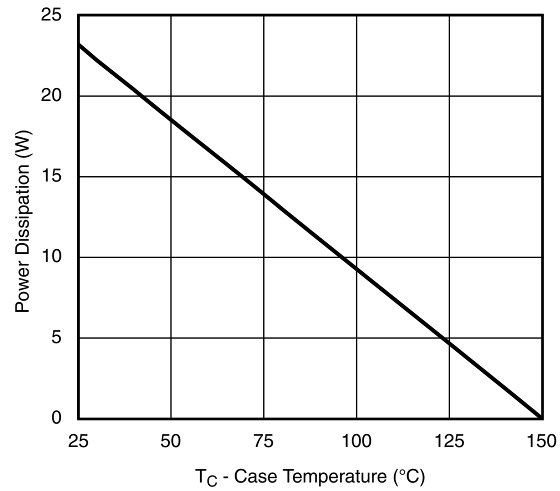
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



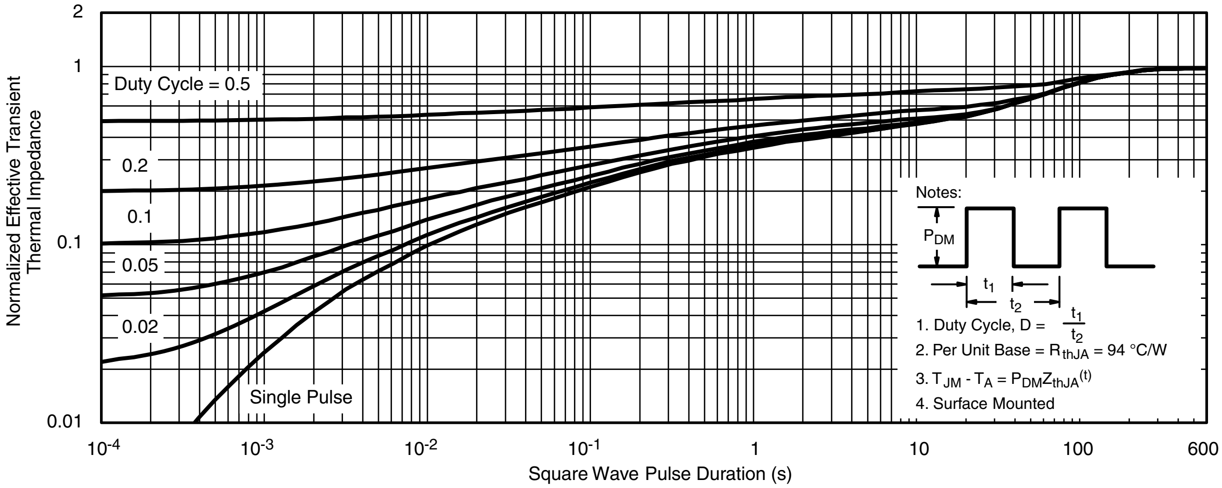
Current Derating*



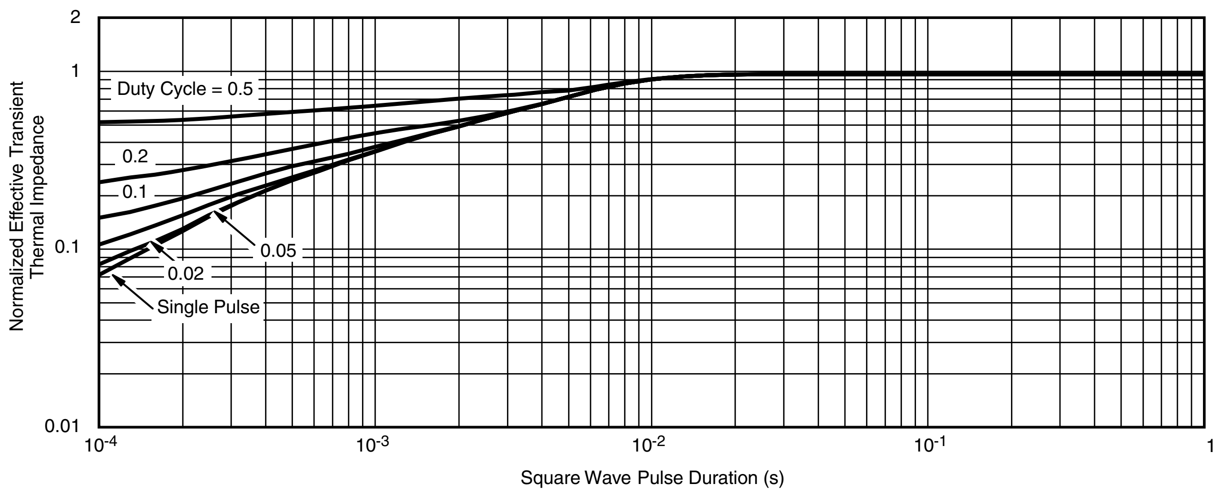
Power Derating

* The power dissipation P_D is based on T_J (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



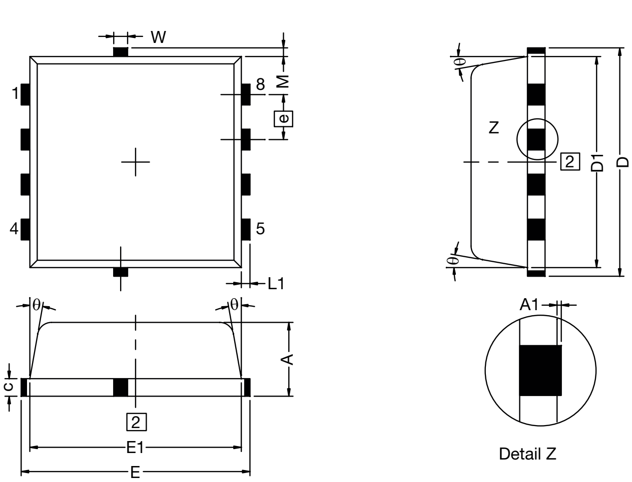
Normalized Thermal Transient Impedance, Junction-to-Ambient

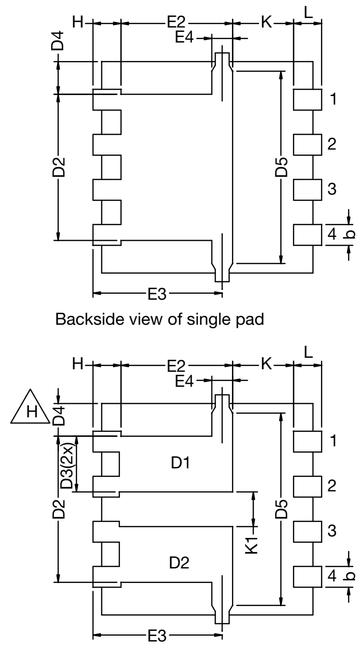


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68986.

PowerPAK® 1212-8, (Single / Dual)





Notes
1. Inch will govern
2. Dimensions exclusive of mold gate burrs
3. Dimensions exclusive of mold flash and cutting burrs

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1	0.00	-	0.05	0.000	-	0.002
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D3	0.48	-	0.89	0.019	-	0.035
D4	0.47 typ.			0.0185 typ		
D5	2.3 typ.			0.090 typ		
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
E4	0.034 typ.			0.013 typ.		
e	0.65 BSC			0.026 BSC		
K	0.86 typ.			0.034 typ.		
K1	0.35	-	-	0.014	-	-
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		

ECN: S16-2667-Rev. M, 09-Jan-17
DWG: 5882

PowerPAK® 1212 Mounting and Thermal Considerations

Johnson Zhao

MOSFETs for switching applications are now available with die on resistances around 1 mΩ and with the capability to handle 85 A. While these die capabilities represent a major advance over what was available just a few years ago, it is important for power MOSFET packaging technology to keep pace. It should be obvious that degradation of a high performance die by the package is undesirable. PowerPAK is a new package technology that addresses these issues. The PowerPAK 1212-8 provides ultra-low thermal impedance in a small package that is ideal for space-constrained applications. In this application note, the PowerPAK 1212-8's construction is described. Following this, mounting information is presented. Finally, thermal and electrical performance is discussed.

THE PowerPAK PACKAGE

The PowerPAK 1212-8 package (Figure 1) is a derivative of PowerPAK SO-8. It utilizes the same packaging technology, maximizing the die area. The bottom of the die attach pad is exposed to provide a direct, low resistance thermal path to the substrate the device is mounted on. The PowerPAK 1212-8 thus translates the benefits of the PowerPAK SO-8 into a smaller package, with the same level of thermal performance.

(Please refer to application note "PowerPAK SO-8 Mounting and Thermal Considerations.")

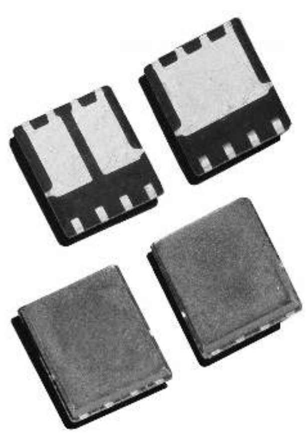


Figure 1. PowerPAK 1212 Devices

The PowerPAK 1212-8 has a footprint area comparable to TSOP-6. It is over 40 % smaller than standard TSSOP-8. Its die capacity is more than twice the size of the standard TSOP-6's. It has thermal performance an order of magnitude better than the SO-8, and 20 times better than TSSOP-8. Its thermal performance is better than all current SMT packages in the market. It will take the advantage of any PC board heat sink capability. Bringing the junction temperature down also increases the die efficiency by around 20 % compared with TSSOP-8. For applications where bigger packages are typically required solely for thermal consideration, the PowerPAK 1212-8 is a good option.

Both the single and dual PowerPAK 1212-8 utilize the same pin-outs as the single and dual PowerPAK SO-8. The low 1.05 mm PowerPAK height profile makes both versions an excellent choice for applications with space constraints.

PowerPAK 1212 SINGLE MOUNTING

To take the advantage of the single PowerPAK 1212-8's thermal performance see Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs.* Click on the PowerPAK 1212-8 single in the index of this document.

In this figure, the drain land pattern is given to make full contact to the drain pad on the PowerPAK package.

This land pattern can be extended to the left, right, and top of the drawn pattern. This extension will serve to increase the heat dissipation by decreasing the thermal resistance from the foot of the PowerPAK to the PC board and therefore to the ambient. Note that increasing the drain land area beyond a certain point will yield little decrease in foot-to-board and foot-to-ambient thermal resistance. Under specific conditions of board configuration, copper weight, and layer stack, experiments have found that adding copper beyond an area of about 0.3 to 0.5 in^2 of will yield little improvement in thermal performance.

PowerPAK 1212 DUAL

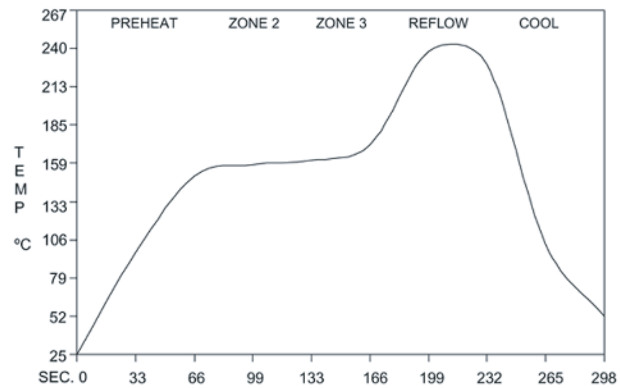
To take the advantage of the dual PowerPAK 1212-8's thermal performance, the minimum recommended land pattern can be found in Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*. Click on the PowerPAK 1212-8 dual in the index of this document.

The gap between the two drain pads is 10 mils. This matches the spacing of the two drain pads on the PowerPAK 1212-8 dual package.

This land pattern can be extended to the left, right, and top of the drawn pattern. This extension will serve to increase the heat dissipation by decreasing the thermal resistance from the foot of the PowerPAK to the PC board and therefore to the ambient. Note that increasing the drain land area beyond a certain point will yield little decrease in foot-to-board and foot-to-ambient thermal resistance. Under specific conditions of board configuration, copper weight, and layer stack, experiments have found that adding copper beyond an area of about 0.3 to 0.5 in^2 of will yield little improvement in thermal performance.

REFLOW SOLDERING

Vishay Siliconix surface-mount packages meet solder reflow reliability requirements. Devices are subjected to solder reflow as a preconditioning test and are then reliability-tested using temperature cycle, bias humidity, HAST, or pressure pot. The solder reflow temperature profile used, and the temperatures and time duration, are shown in Figures 2 and 3. For the lead (Pb)-free solder profile, see http://www.vishay.com/doc?73257.



Ramp-Up Rate	+ 6 °C /Second Maximum
Temperature at 155 ± 15 °C	120 Seconds Maximum
Temperature Above 180 °C	70 - 180 Seconds
Maximum Temperature	240 + 5/- 0 °C
Time at Maximum Temperature	20 - 40 Seconds
Ramp-Down Rate	+ 6 °C/Second Maximum

Figure 2. Solder Reflow Temperature Profile

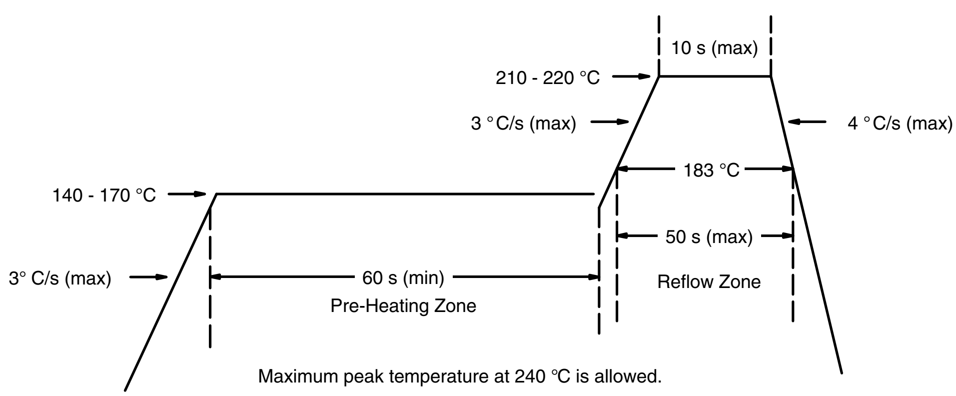


Figure 3. Solder Reflow Temperatures and Time Durations

TABLE 1: EQIVALENT STEADY STATE PERFORMANCE										
Package	**SO-8**		**TSSOP-8**		**TSOP-8**		**PPAK 1212**		**PPAK SO-8**	
Configuration	**Single**	**Dual**	**Single**	**Dual**	**Single**	**Dual**	**Single**	**Dual**	**Single**	**Dual**
Thermal Resiatance R_{thJC}(C/W)	20	40	52	83	40	90	2.4	5.5	1.8	5.5

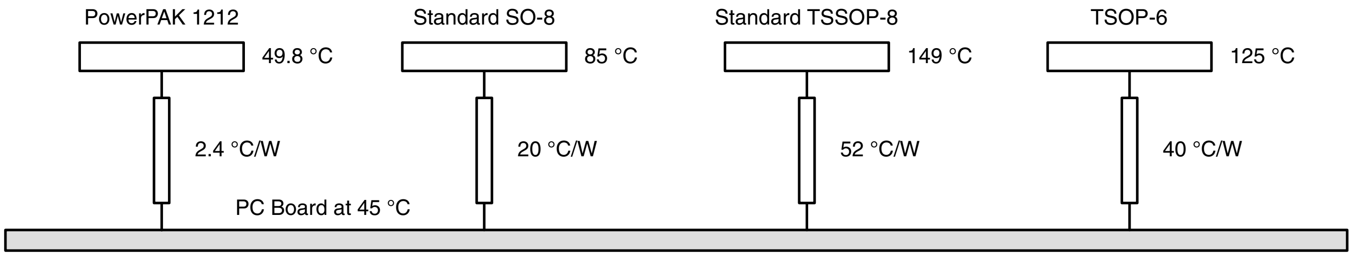


Figure 4. Temperature of Devices on a PC Board

THERMAL PERFORMANCE

Introduction

A basic measure of a device's thermal performance is the junction-to-case thermal resistance, Rθjc, or the junction to- foot thermal resistance, Rθjf. This parameter is measured for the device mounted to an infinite heat sink and is therefore a characterization of the device only, in other words, independent of the properties of the object to which the device is mounted. Table 1 shows a comparison of the PowerPAK 1212-8, PowerPAK SO-8, standard TSSOP-8 and SO-8 equivalent steady state performance.

By minimizing the junction-to-foot thermal resistance, the MOSFET die temperature is very close to the temperature of the PC board. Consider four devices mounted on a PC board with a board temperature of 45 °C (Figure 4).

Suppose each device is dissipating 2 W. Using the junction-to-foot thermal resistance characteristics of the PowerPAK 1212-8 and the other SMT packages, die temperatures are determined to be 49.8 °C for the PowerPAK 1212-8, 85 °C for the standard SO-8, 149 °C for standard TSSOP-8, and 125 °C for TSOP-6. This is a 4.8 °C rise above the board temperature for the PowerPAK 1212-8, and over 40 °C for other SMT packages. A 4.8 °C rise has minimal effect on $r_{DS(ON)}$ whereas a rise of over 40 °C will cause an increase in $r_{DS(ON)}$ as high as 20 %.

Spreading Copper

Designers add additional copper, spreading copper, to the drain pad to aid in conducting heat from a device. It is helpful to have some information about the thermal performance for a given area of spreading copper.

Figure 5 and Figure 6 show the thermal resistance of a PowerPAK 1212-8 single and dual devices mounted on a 2-in. x 2-in., four-layer FR-4 PC boards. The two internal layers and the backside layer are solid copper. The internal layers were chosen as solid copper to model the large power and ground planes common in many applications. The top layer was cut back to a smaller area and at each step junction-to-ambient thermal resistance measurements were taken. The results indicate that an area above 0.2 to 0.3 square inches of spreading copper gives no additional thermal performance improvement. A subsequent experiment was run where the copper on the back-side was reduced, first to 50 % in stripes to mimic circuit traces, and then totally removed. No significant effect was observed.

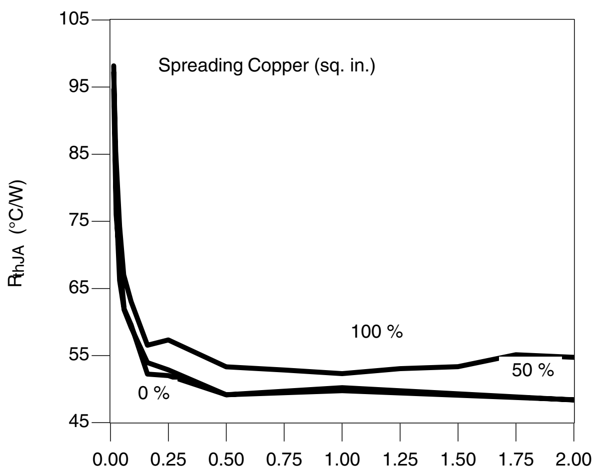


Figure 5. Spreading Copper - Si7401DN

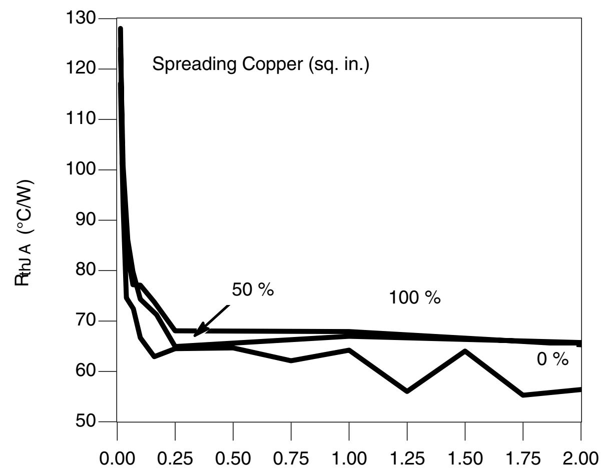


Figure 6. Spreading Copper - Junction-to-Ambient Performance

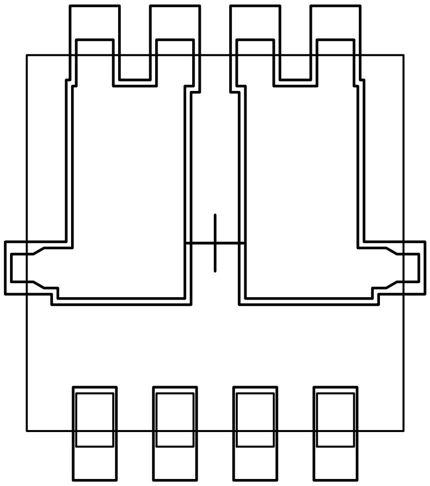
CONCLUSIONS

As a derivative of the PowerPAK SO-8, the PowerPAK 1212-8 uses the same packaging technology and has been shown to have the same level of thermal performance while having a footprint that is more than 40 % smaller than the standard TSSOP-8.

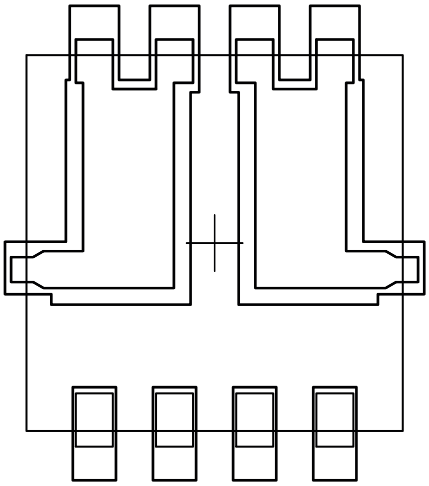
Recommended PowerPAK 1212-8 land patterns are provided to aid in PC board layout for designs using this new package.

The PowerPAK 1212-8 combines small size with attractive thermal characteristics. By minimizing the thermal rise above the board temperature, PowerPAK simplifies thermal design considerations, allows the device to run cooler, keeps $r_{DS(ON)}$ low, and permits the device to handle more current than a same- or larger-size MOSFET die in the standard TSSOP-8 or SO-8 packages.

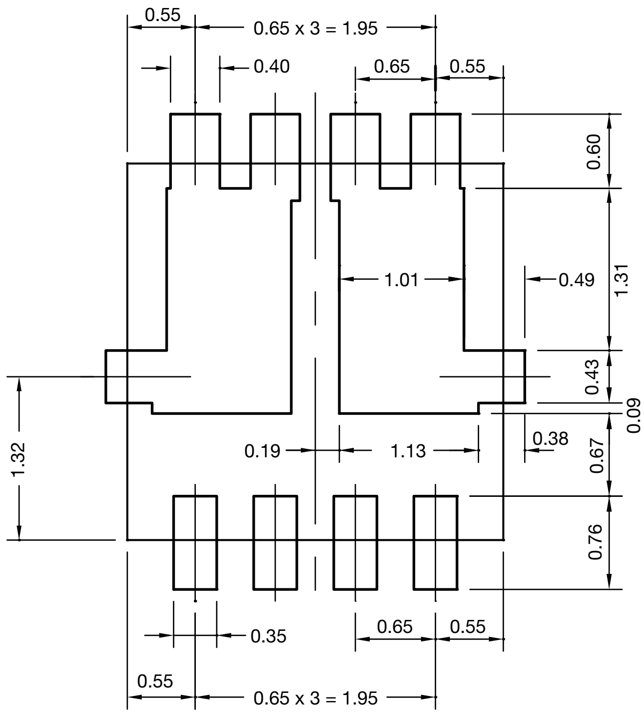
Recommended Land Pattern for PowerPAK® 1212-8 Dual



For BW package



For BWL package



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