Low Phase Noise Clock Evaluation Module — up to 1.5 GHz

1 Features

- Easy-to-use evaluation module to generate low phase noise clocks up to 1.5 GHz
- Easy device programming via host-powered USB port
- Rapid configuration through provided EVM Control Software
- Can be powered from the USB port, or by an external 3.3V power supply
- Single-ended or differential input; external crystal can be used with on-chip oscillator
- Footprint for optional crystal filter on one output

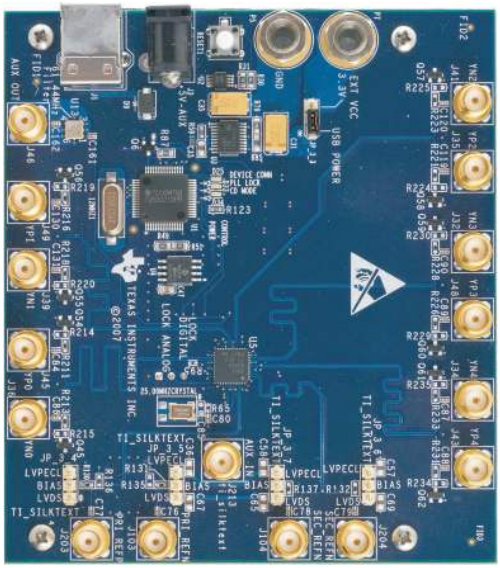


Figure 1. CDCE62005EVM Evaluation Board

2 General Description

The CDCE62005 is a high performance, low phase noise frequency synthesizer and jitter cleaner. It features an on-chip PLL with dual integrated LC Voltage Controlled Oscillators (VCOs) operating from 1.75–2.35 GHz. It provides support for three manually or automatically selected inputs, and provides up to five differential, or ten single-ended, low-jitter outputs.

The CDCE62005 supports single-ended and differential input signals, as well as providing a crystal oscillator circuit that operates in conjunction with an external AT-cut crystal.

The CDCE62005 is programmed through an SPI interface using the supplied EVM programming graphical user interface (GUI).

The evaluation module (EVM) demonstrates the electrical performance of the device. This fully-assembled, factory-tested evaluation board allows complete validation of all device functions. For optimum performance, the board is equipped with 50Ω SMA connectors and well-controlled 50Ω impedance microstrip transmission lines.

3 Signal Path and Control

The CDCE62005 provides three selectable inputs – PRI REF, SEC REF, and AUX IN. The PRI REF and SEC REF inputs can accept up to 1500 MHz in the fan-out mode. In the PLL mode, PRI REF and SEC REF can accept an input at up to 500MHz from a differential signal source, or up to 250MHz from a single

ended CMOS signal source. The AUX IN allows the use of an external crystal in the frequency range of 3.25MHz to 42MHz. The CDCE62005EVM provides a PC-board footprint for mounting a 5mm × 3,2mm SMD crystal. If the AUX IN is driven through the SMA connector, the on-board crystal must be removed, and R65 must be populated with a 0 ohm resistor. The CDCE62005EVM also provides support for driving the PRI REF signals from an on-board 5mm × 7mm crystal oscillator (U12).

The CDCE62005 provides up to five differential (LVDS or LVPECL) or ten single ended (LVCMOS) or any combination of outputs up to 1.5 GHz (LVPECL). It operates as a jitter cleaner, or as a frequency synthesizer, or both. An optional single ended output (AUX OUT) provides an LVCMOS copy of either the third or fourth output. On the CDCE62005EVM the AUX OUT signal path has a footprint for an optional crystal filter (U13).

The CDCE62005 can use either a completely-internal loop filter, or a partially-external loop filter. The loop-filter selection will affect the phase noise and loop stability of the PLL. If the CDCE62005 is to be used only as a frequency synthesizer, the completely internal loop filter option is recommended. If the CDCE62005 is used as a jitter cleaner, the partially external loop filter option is recommended, because this allows for lower loop bandwidths to be obtained using resistors and capacitors which are larger than the ones available on-chip.

The CDCE62005 options are selected by programming the on-chip registers. The CDCE62005 datasheet provides the detailed information needed to configure and use this device.

Each of the five outputs of the CDCE62005 may be configured as an LVPECL, LVDS, or LVCMOS type. The CDCE62005 select/deselect the the 150Ω load resistor required by the LVPECL output. The corresponding load resistor must be selected in the software interface when an output is configured as LVPECL.

The LVCMOS outputs can operate at frequencies up to 250MHz. The LVPECL outputs operate at up to 1.5GHz (fan-out mode). The LVDS outputs operate at up to 800MHz.

4 Software Selectable Options

The provided EVM Control Software (EVMCS) communicates with the CDCE62005 through a USB interface through the CDCE62005 SPI port. The USB controller is normally powered over the USB cable, but can be optionally be powered by an external 5V DC adapter that is plugged into the additional power connector on the EVM. When the USB/SPI programming interface is available for use, the on-board LED D25 is illuminated.

In addition to writing commands to the CDCE62005 SRAM while the board is powered, configurations can also be stored in the on-chip EEPROM. This allows the EVM to start up in the desired configuration upon powerup.

The CDCE62005 has a mode which permanently locks the EEPROM. After this mode is selected, the EEPROM contents within the CDCE62005 cannot be changed. This is useful when setting final configurations.

The CDCE62005 EVMCS also allows device configurations to be saved into a configuration file (.INI), which can be loaded by the EVMCS at a later time to restore the saved settings.

5 Installing the EVM Control Software and USB Driver

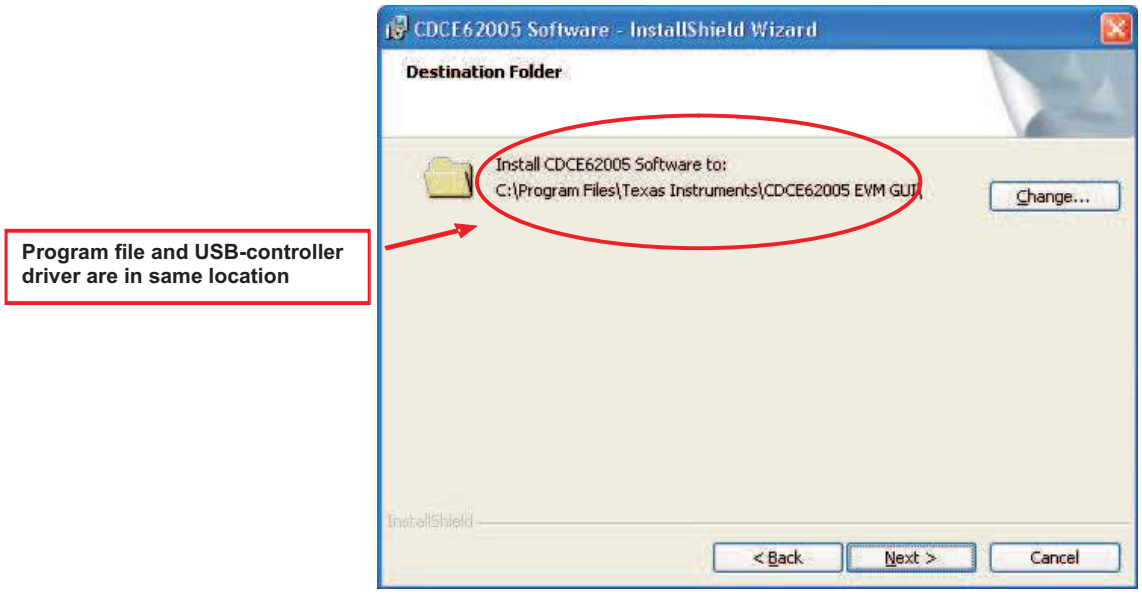
The CDCE62005 EVMCS requires a Java Runtime Environment (JRE) to be installed. The latest JRE is available as a free download at http://java.com. Install the JRE first, before attempting to install the CDCE62005 EVMCS. To start the installation of the EVM software, double-click on the file named “CDCE62005EVM-n_n_n-install.exe”, where n_n_n is the current software version number.

Note that the USB driver must be installed in the same installation folder as the EVMCS program file after the setup completes and the USB cable is connected (first time only).

After the setup wizard completes start the EVMCS from the start menu (Start → Texas Instruments Inc → CDCE62005 Software & Driver → CDCE62005).

Connect the USB cable to the EVM. If a box appears asking for an appropriate driver, **Do not use the automatic search option!** Select a manual installation and when prompted for the driver location browse to the CDCE62005EVM program file folder that was used during instillation. If Windows does not ask for a driver, no action is needed.

After USB driver installation, the EVM software should connect properly and be ready for use. A green light in the USB Status and SPI Bus Status boxes indicates a good USB connection, and a dark light indicates a faulty USB connection or a faulty SPI bus.



5.1 CDCE62005 Control User Interface

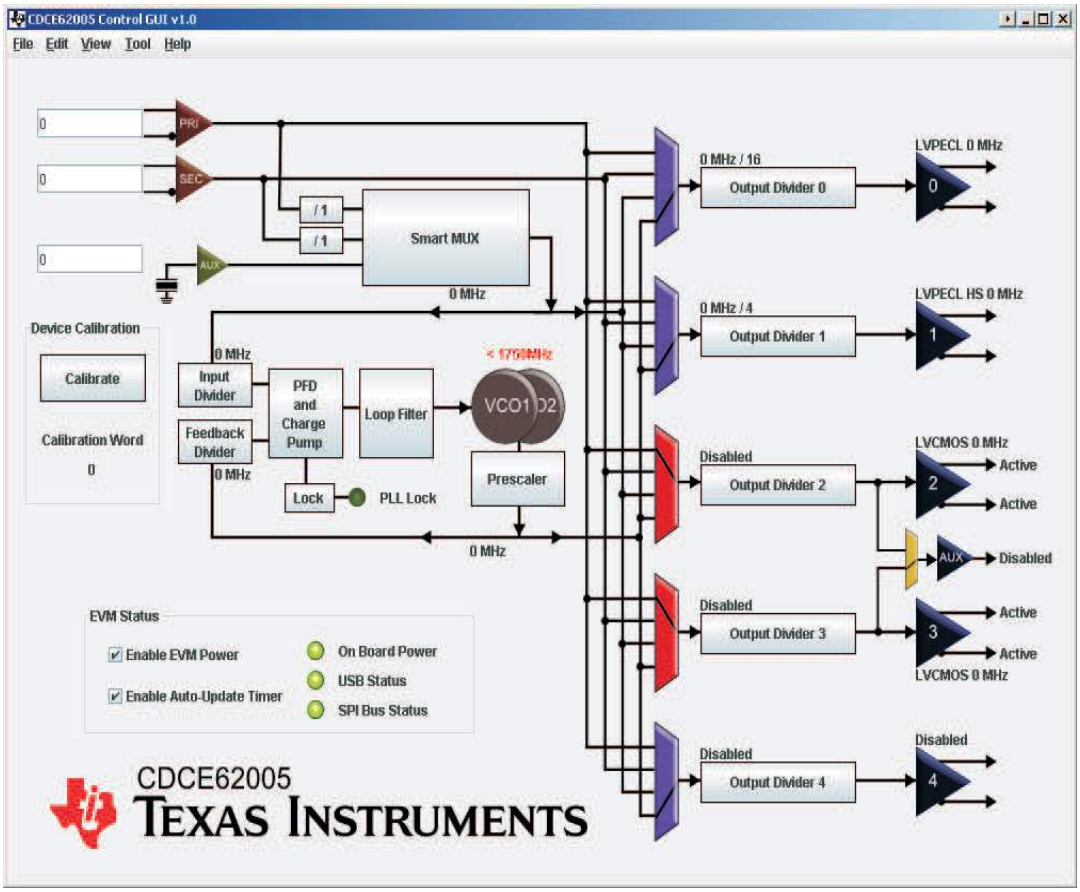


Figure 2. TI CDCE62005 EVMCS Display

5.2 Using the EVM Control Software

The graphical layout of the EVMCS is based on the functional structure of the CDCE62005. Using the EVMCS, the system designer can change the Input Frequency, Input Divider, Input type, Input selection, PFD Charge Pump, Internal/External Loop Filter, Output MUX selection, Output Divider, and Output type. Other configurations are selected by the software with user-selectable options as described in the steps below. If the CDCE62005EVM is USB powered, the “Enable EVM Power” check box must be checked. If the CDCE62005 is powered from an external source, the “Enable EVM Power” check box must be unchecked.

1. **Primary/Secondary Reference**

   The primary or the secondary reference input buffer section on the EVMCS can be clicked for a popup window that opens, as shown in Figure 3, showing selections on the external input signal type (differential or single ended), the external signal connection to the CDCE62005 primary/secondary inputs (AC or DC termination), input-buffer internal termination (enabled or disabled), and the input-buffer VBB voltage polarity (normal or inverted).

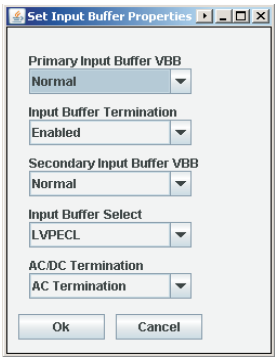


Figure 3. Input Buffer Properties

2. **Reference Input Selection through Smart MUX**

   The Smart MUX section of the EVMCS can be clicked for a popup window that opens, as shown in Figure 4, showing

   - Selections on the EECLKSEL option
     - "0" suggests using the REF_SEL pin for input selection and disabling the auto-select feature
     - "1" suggests using the auto-select feature and disabling the REF_SEL feature)
     - the Smart MUX reshaping (reshaping either or both of the primary and secondary input signals, introducing short delay to either or both of the primary and secondary input signals for fast operation)
   - Selection of the reference divider of the primary or the secondary input signal after the first of the two Smart MUX-es

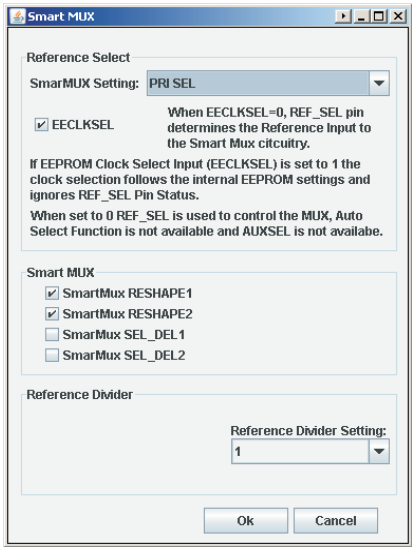


Figure 4. Smart MUX

3. **PFD and Charge Pump Selection**

The PFD and Charge Pump section of the EVMCS can be clicked for a popup window that opens, as shown in Figure 5, showing selections for the charge pump current and charge pump pulse width. For the internal loop filter, lower charge pump currents work well and for the external loop filter, higher charge pump currents work well.

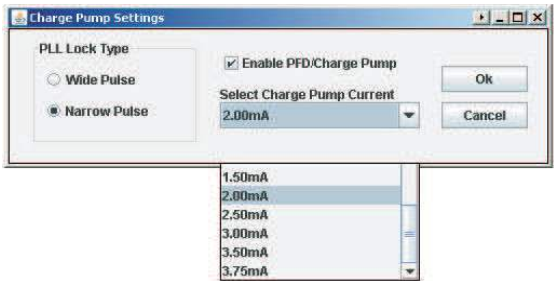


Figure 5. Charge Pump

4. **Loop Filter Selection**

The Loop Filter section of the EVMCS can be clicked for a popup window that shows the internal loop-filter configuration, where the values of the resistors and capacitors of the active loop filter can be selected from the allowable dropdown list for each component.

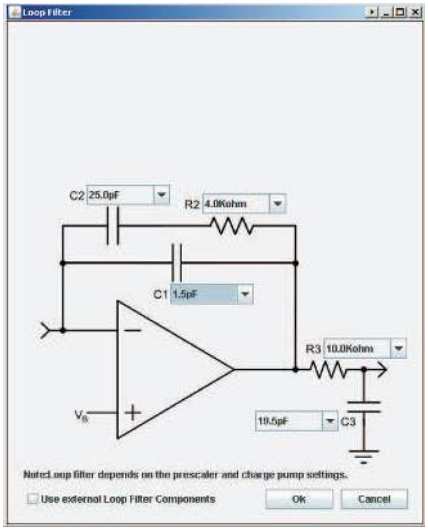


Figure 6. Loop Filter, Internal Only

Alternately, the loop filter with additional external components can be enabled by clicking the “Use External Loop Filter Components” button and by enabling the appropriate DIPswitches (SW9 and SW10) on the bottom of the CDCE62005EVM as described in the “Configuring the Board” section of this User’s Guide. The external loop filter components (C4, R4 and C5) are in green in the picture displayed below. The component values entered into the text boxes are saved when a configuration file is saved, and displayed when that configuration file is reloaded. However, the external component values are not used by the EVMCS for calculations.

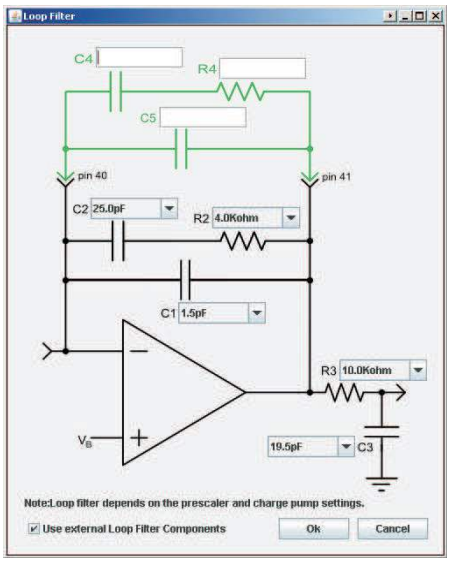


Figure 7. Loop Filter, Additional External Components

5. **Output MUX Selection**

   The Output MUX section of the EVMCS for each of the five outputs can be clicked to open a popup window, shown in Figure 8, showing each Output MUX clock source. These are selectable between the primary input, secondary input, Smart MUX output or the PLL VCO core output.

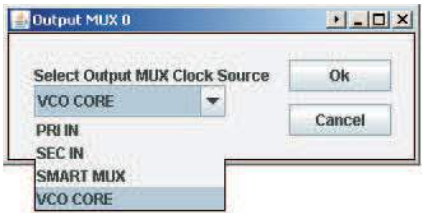


Figure 8. Output MUX (each output channel)

6. **Output Type Selection**

   The Output buffer section of the EVMCS for each of the five outputs can be clicked to open a popup window that shows options for each output clock source. These are selectable between LVPECL, High Swing LVPECL (in which cases the output 150Ω termination is automatically enabled), Reduced Range Link LVDS, General Purpose Link LVDS, LVCMOS (in which case each of the P and N act as two separate LVCMOS outputs with the same frequency that can either be active, inverting, tri-state or low) or each output can be disabled.

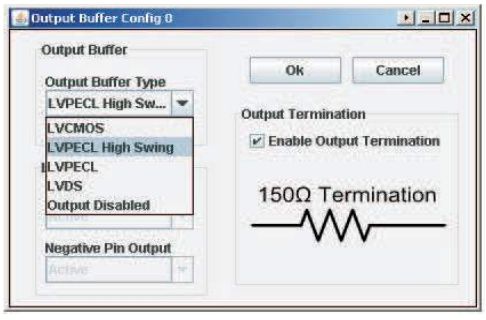


Figure 9. Output Buffer Config (each output)

7. **PLL Dividers Selection**

   The input, feedback and prescaler dividers can be selected by clicking on tabs in the EVMCS which

opens a popup window displaying all the possible selections of those dividers. Care must be taken in choosing these dividers, along with the VCO, charge pump and loop filter, such that the on-chip PLL of the CDCE62005 can operate in a stable closed-loop manner. Refer to the CDCE62005 data sheet for further information on appropriate configuration of the PLL for closed-loop operation. After the dividers are set accordingly, the PLL LOCK indicator display on the EVMCS are a bright green color. Also, the on-board LED D33 illuminates to indicate PLL lock. The output dividers for each output can also be chosen from possible selections displayed in the popup window, opened by clicking the output-divider tab in the EVMCS. Each output divider can also be disabled.

8. **Write to CDCE62005 EEPROM**

To write any particular setting to the EEPROM (locked or unlocked), the menu item at the top of the EVMCS titled “Tool” must be clicked. This highlights the items “Write EEPROM Unlocked” and “Write EEPROM Locked” as part of a drop-down menu. Choosing the appropriate one after setting the desired PLL configurations writes to the EEPROM in its appropriate mode.

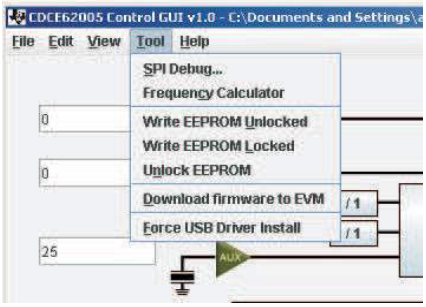
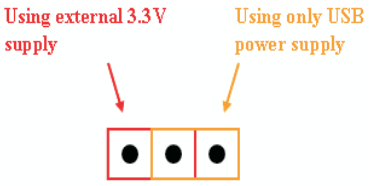


Figure 10. Tools – Write to EEPROM

6 Configuring the Board

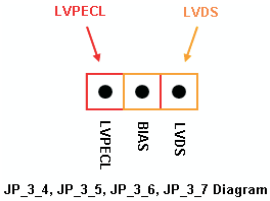
Configuration for Programming and Testing (with USB cable attached) (Default Configuration)
The CDCE62005EVM is configured by default to operate with the USB cable attached and a 3.3V power supply added to EXT VDD and GND. In this configuration the USB microcontroller is powered by the USB port 5V supply, while the CDCE62005 is powered by the 3.3V external supply. This configuration is best for programming the CDCE62005 while also taking measurements. This configuration removes the power variation found in USB power supplies by isolating the CDCE62005 from the USB supply.

Configuration for Programming (using USB power)
The CDCE62005EVM can use power supplied through the USB cable as its sole power source. (Not recommended for measurements) This capability is intended for saving configuration settings to the CDCE62005 and later powering the device from its internal memory (useful during performance testing of the device). In this configuration JP_3_3 must be moved from its default position to the new position shown below. Also the “Enable EVM Power” box must be checked on the EVM display.



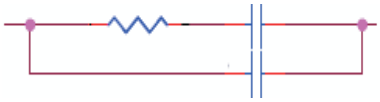
JP_3_3 Diagram

Configuration for On-board Reference Input Biasing
If the CDCE62005 on-chip biasing is not used for AC-coupled reference input signals for PRI_REF or SEC_REF, the CDCE62005EVM can alternately be set up to provide on-board biasing for LVPECL or LVDS inputs. These bias voltages of 1.2V for LVDS and 1.9V for LVPECL are derived from the on-board voltage regulator (U3). The bias points are available for every leg of the differential signals at both PRI_REF and SEC_REF and can be enabled by using the jumpers on the CDCE62005EVM, JP_3_4 and JP_3_5 for PRI_REF and JP_3_6 and JP_3_7 for SEC_REF. Each of these jumpers can be configured as shown below for either LVPECL or LVDS bias.



Configuration for On-board External Loop Filter

If the CDCE62005 is configured as a jitter cleaner, it requires the use of the partially-external loop filter, located on the bottom side of the CDCE62005EVM PC board. There are four external loop filter options provided on the EVM. The external loop filter topology is as shown below.



The external loop filter can be chosen by selecting one from the four available options on the CDCE62005EVM using the dip switches, SW9 and SW10, located at the bottom side of the EVM and shown below.

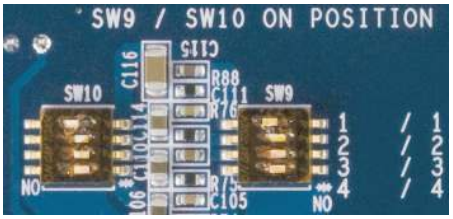


Figure 11. External Loop Filter Selection Switches

Configuration for PLL Lock Detect

The CDCE62005 PLL lock detect can be chosen on the CDCE62005EVM as either an analog lock detect or a digital lock detect using the jumper, JP_3_12, located at the back side of the CDCE62005EVM. This jumper can be configured as shown in Figure 12 for either analog or digital lock detect.

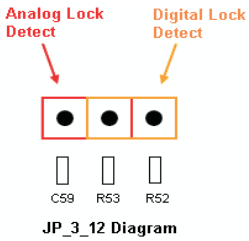
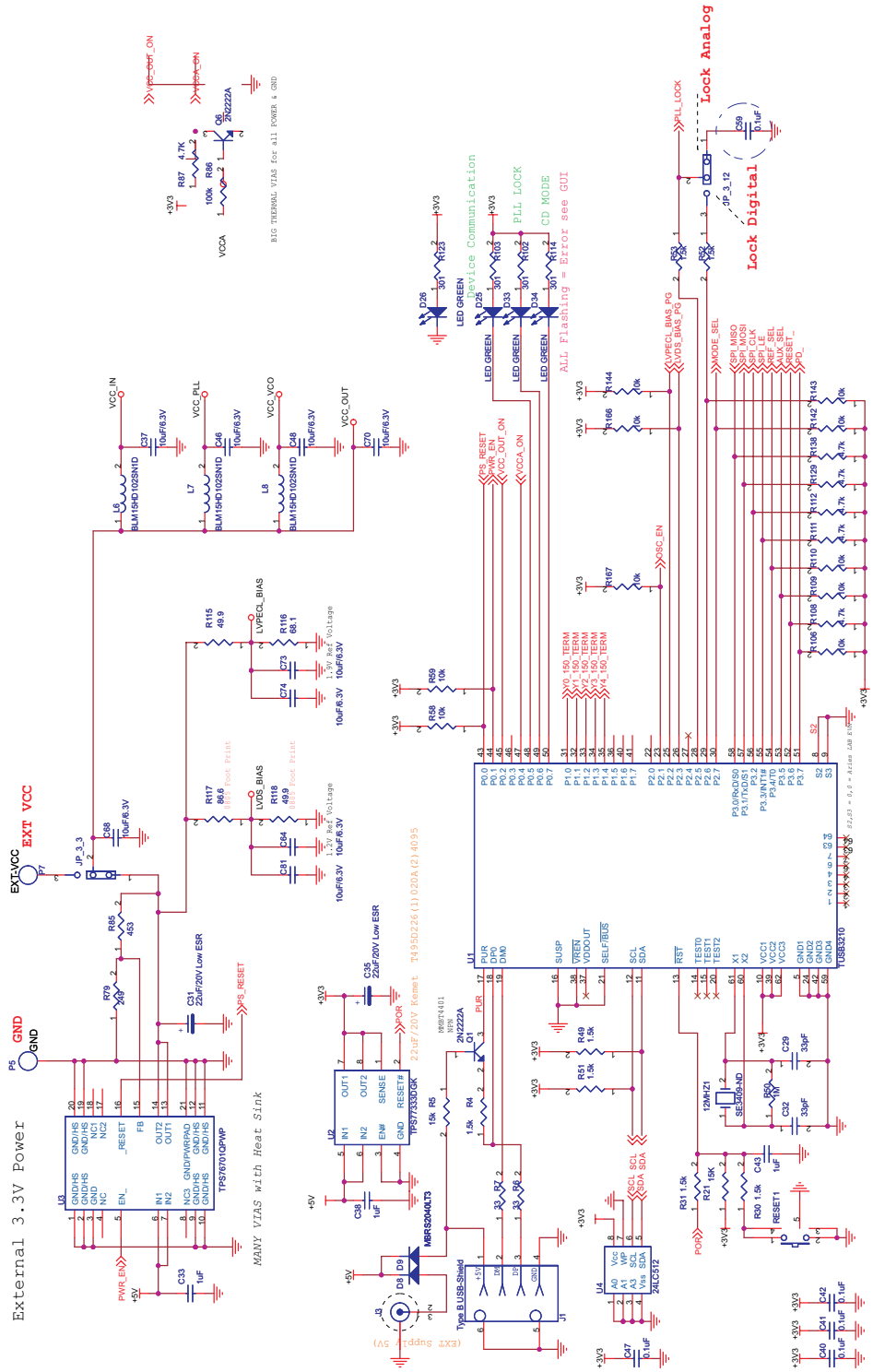
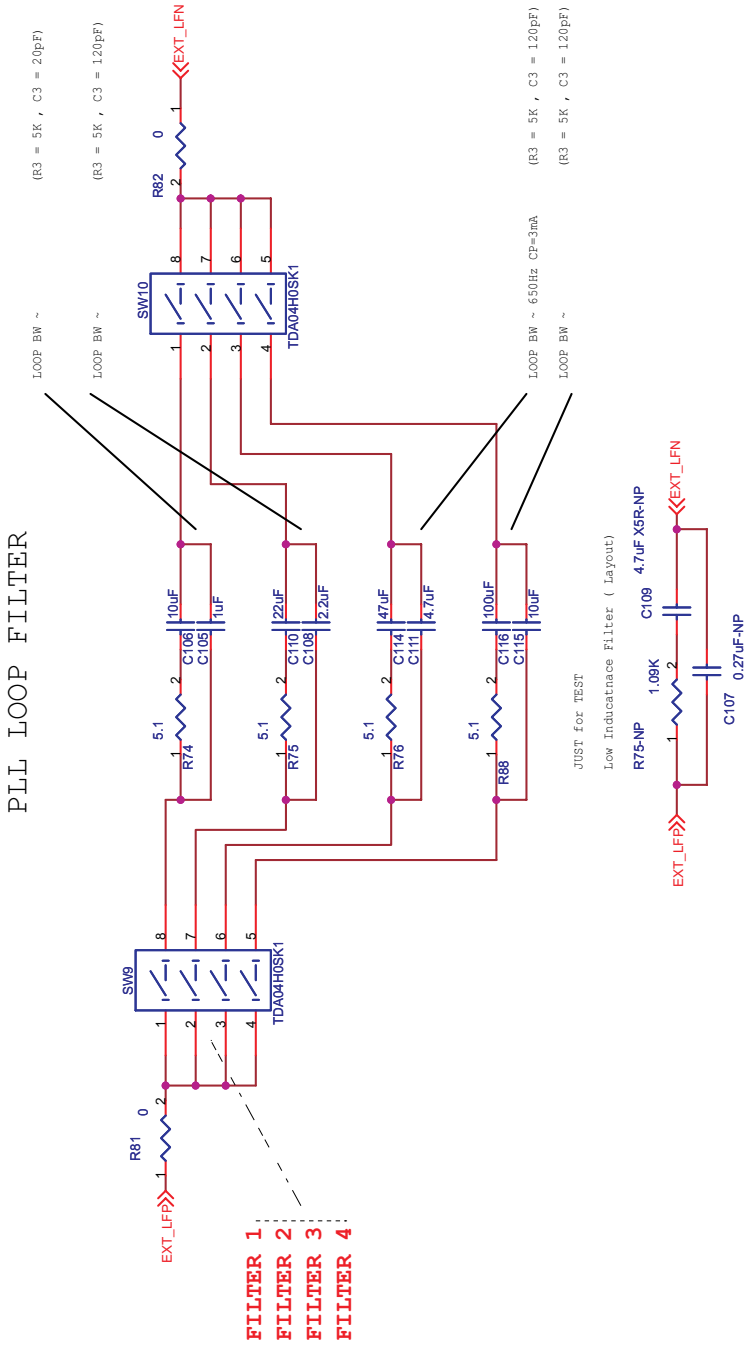
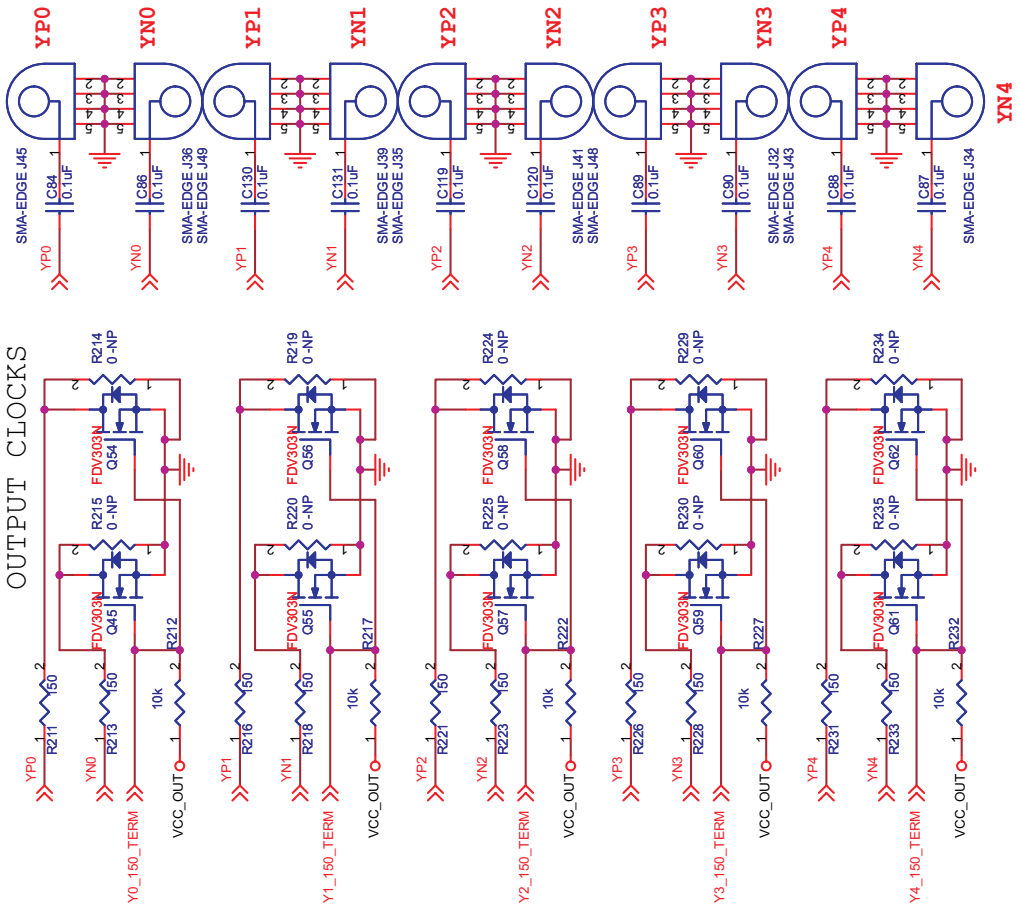


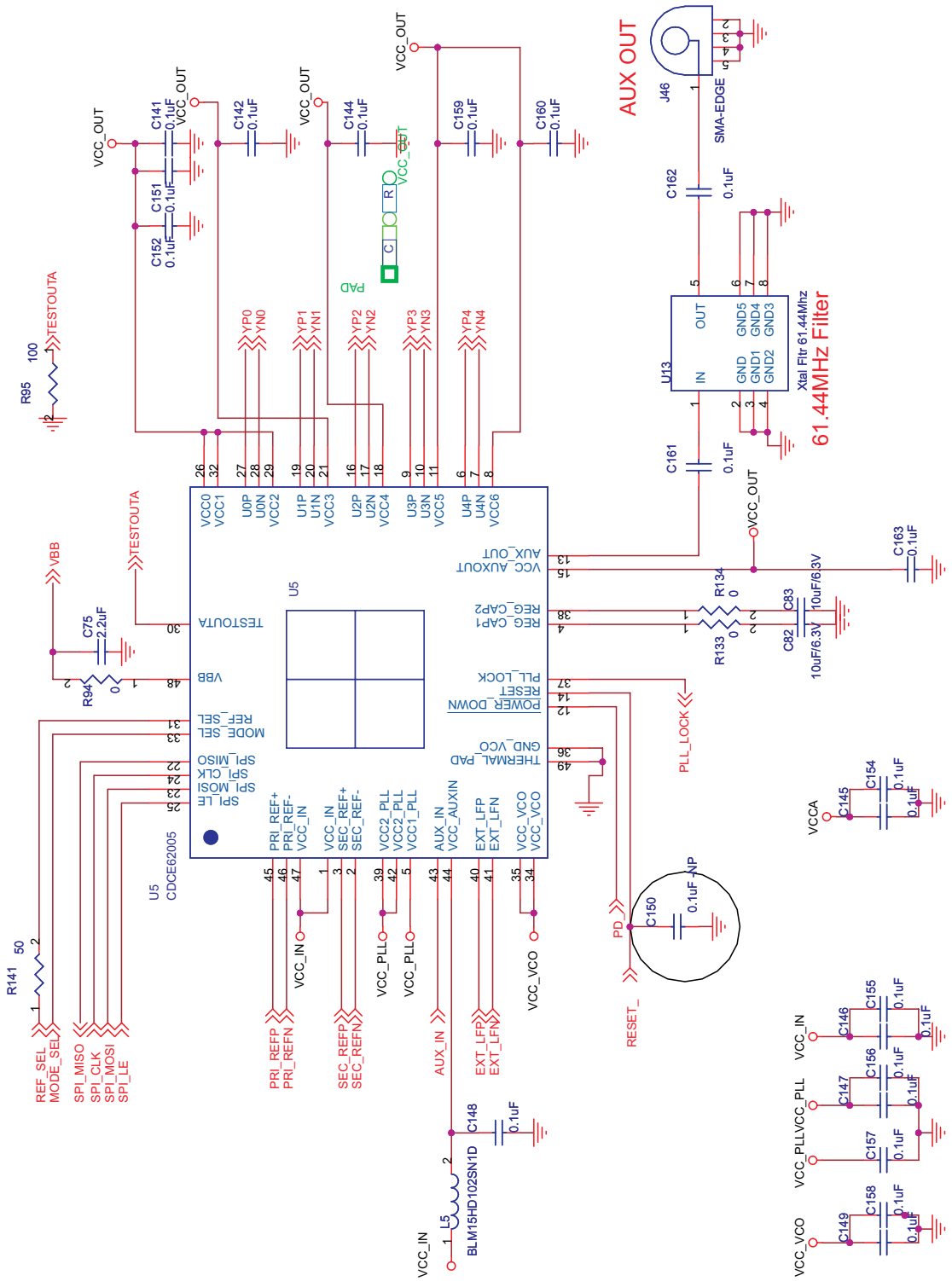
Figure 12. Lock Detect Select Jumper

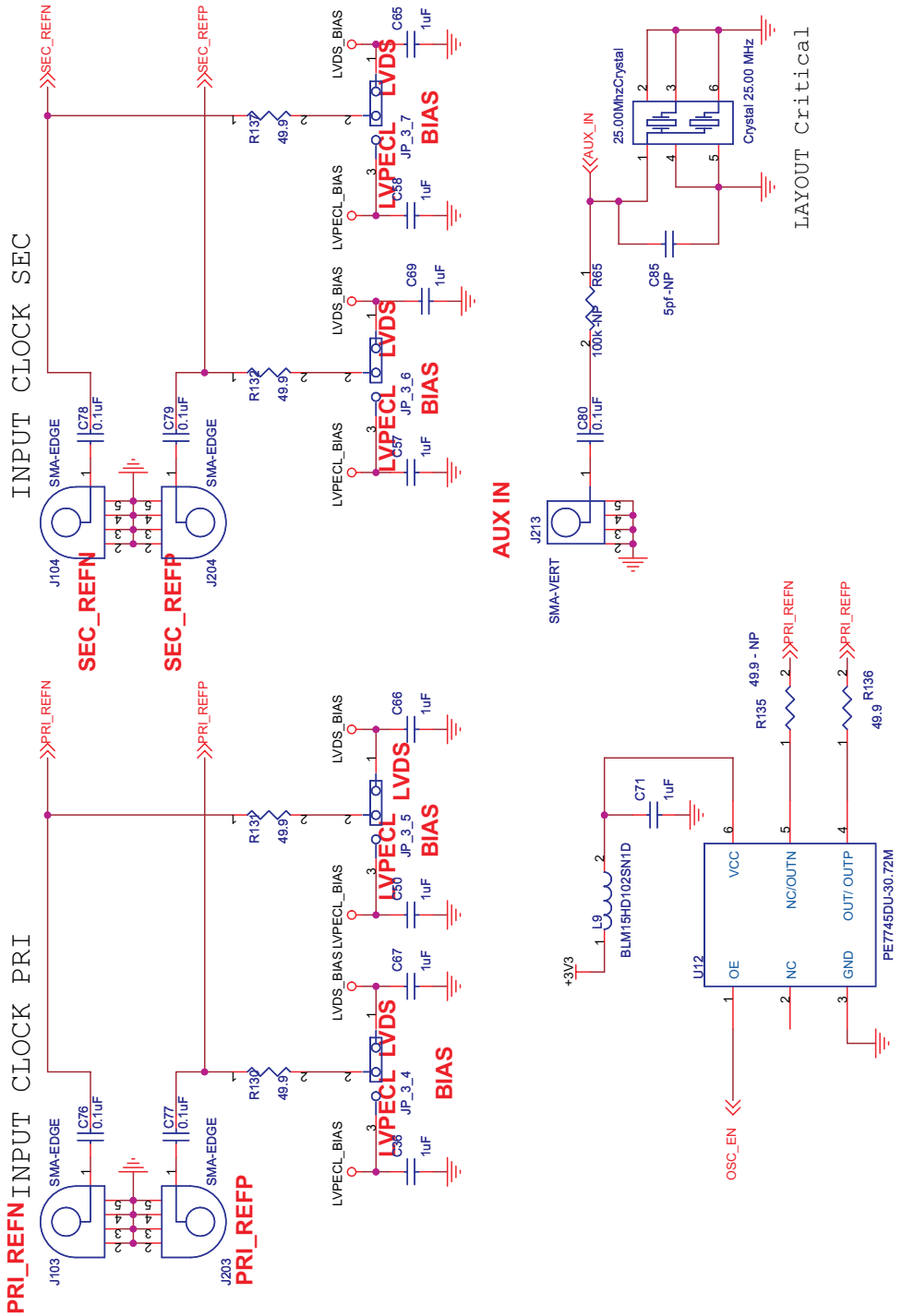
7 CDCE62005EVM Board Schematic Diagram




PLL LOOP FILTER
LOOP BW ~ (R3 = 5K , C3 = 20pF)
LOOP BW ~ (R3 = 5K , C3 = 120pF)
LOOP BW ~ 650Hz CP=3mA (R3 = 5K , C3 = 120pF)
LOOP BW ~ (R3 = 5K , C3 = 120pF)
EXT_LFN
R82 0
SW10
TDA04H0SK1
10uF
1uF
22uF
2.2uF
47uF
4.7uF
100uF
10uF
C106
C105
C110
C108
C114
C111
C116
C115
5.1
R74
R75
R76
R88
SW9
TDA04H0SK1
R81 0
EXT_LFP
FILTER 1
FILTER 2
FILTER 3
FILTER 4
JUST for TEST
Low Inducatnace Filter (Layout)
R75-NP
1.09K
C109
4.7uF X5R-NP
C107
0.27uF-NP
EXT_LFN
EXT_LFP


YP0
YN0
YP1
YN1
YP2
YN2
YP3
YN3
YP4
YN4
SMA-EDGE J45
C84 0.1uF
SMA-EDGE J36
SMA-EDGE J49
C86 0.1uF
C130 0.1uF
SMA-EDGE J39
SMA-EDGE J35
C131 0.1uF
C119 0.1uF
SMA-EDGE J41
SMA-EDGE J48
C120 0.1uF
C89 0.1uF
SMA-EDGE J32
SMA-EDGE J43
C90 0.1uF
C88 0.1uF
SMA-EDGE J34
C87 0.1uF
OUTPUT CLOCKS
R214 0 -NP
R215 0 -NP
FDV303N Q54
FDV303N Q45
R211 50
R213 50
R212 10k
VCC_OUT
Y0_150_TERM
R219 0 -NP
R220 0 -NP
FDV303N Q56
FDV303N Q55
R216 50
R218 50
R217 10k
Y1_150_TERM
R224 0 -NP
R225 0 -NP
FDV303N Q58
FDV303N Q57
R221 50
R223 50
R222 10k
Y2_150_TERM
R229 0 -NP
R230 0 -NP
FDV303N Q60
FDV303N Q59
R226 50
R228 50
R227 10k
Y3_150_TERM
R234 0 -NP
R235 0 -NP
FDV303N Q62
FDV303N Q61
R231 50
R233 50
R232 10k
Y4_150_TERM


AUX OUT
J46
SMA-EDGE
61.44MHz Filter
Xtal Fltr 61.44Mhz
U13
U5
CDCE62005
VCC_OUT
TESTOUTA
VBB
PLL_LOCK
RESET_
PD_
REF_SEL
MODE_SEL
SPI_MISO
SPI_CLK
SPI_MOSI
SPI_LE
PRI_REFP
PRI_REFN
SEC_REFP
SEC_REFN
VCC_IN
VCC_PLL
AUX_IN
EXT_LFP
EXT_LFN
VCC_VCO
VCCA
VCC_PLLVCC_PLL
BLM15HD102SN1D
PAD


INPUT CLOCK SEC
INPUT CLOCK PRI
LAYOUT Criticial
AUX IN
SEC_REFN
SEC_REFP
PRI_REFN
PRI_REFP
LVPECL
LVDS
BIAS
SMA-EDGE
SMA-VERT
LVDS_BIAS
LVPECL_BIAS
25.00MhzCrystal
Crystal 25.00 MHz
5pf-NP
100k-NP
49.9 - NP
49.9
BLM15HD102SN1D
PE7745DU-30.72M
OSC_EN
+3V3

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 3 V to 3.6 V and the output voltage range of 0 V to 3.6 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 120°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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