DATA SHEET

TDA8929T
Controller class-D audio amplifier

Preliminary specification
File under Integrated Circuits, IC01

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Philips
Semiconductors

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CONTENTS

1 FEATURES

- Operating voltage from ±15 to ±30 V
- Very low quiescent current
- Low distortion
- Fixed gain of 30 dB Single-Ended (SE) or 36 dB Bridge-Tied Load (BTL)
- Good ripple rejection
- Internal switching frequency can be overruled by an external clock
- No switch-on or switch-off plop noise
- Diagnostic input for short-circuit and temperature protection
- Usable as a stereo Single-Ended (SE) amplifier or as a mono amplifier in Bridge-Tied Load (BTL)
- Start-up safety test, to protect for short-circuits at the output of the power stage to supply lines
- Electrostatic discharge protection (pin to pin).

2 APPLICATIONS

- Television sets
- Home-sound sets
- Multimedia systems
- All mains fed audio systems
- Car audio (boosters).

3 GENERAL DESCRIPTION

The TDA8929T is the controller of a two-chip set for a high efficiency class-D audio power amplifier system. The system is divided into two chips:

- TDA8929T; the analog controller chip in a SO24 package
- TDA8926J/ST/TH or TDA8927J/ST/TH; a digital power stage in a DBS17P, RDBS17P or HSOP24 power package.

With this chip set a compact 2×50 W or 2×100 W audio amplifier system can be built, operating with high efficiency and very low dissipation. No heatsink is required, or depending on supply voltage and load, a very small one. The system operates over a wide supply voltage range from ±15 up to ±30 V and consumes a very low quiescent current.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8929T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

5 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
General; note 1					
V_P	supply voltage	±15	±25	±30	V
$I_{q(tot)}$	total quiescent current	–	20	30	mA
Stereo single-ended configuration					
$G_{v(cl)}$	closed-loop voltage gain	29	30	31	dB
$\lvert Z_i \rvert$	input impedance	45	68	–	kΩ
$V_{n(o)}$	noise output voltage	–	220	400	μV
SVRR	supply voltage ripple rejection	40	50	–	dB
α_{cs}	channel separation	–	70	–	dB
$\lvert V_{OO} \rvert$	DC output offset voltage	–	–	150	mV
Mono bridge-tied load configuration					
$G_{v(cl)}$	closed-loop voltage gain	35	36	37	dB
$\lvert Z_i \rvert$	input impedance	23	34	–	kΩ
$V_{n(o)}$	noise output voltage	–	280	–	μV
SVRR	supply voltage ripple rejection	–	44	–	dB
$\lvert V_{OO} \rvert$	DC output offset voltage	–	–	200	mV

Note

1. V_P = ±25 V.

6 BLOCK DIAGRAM

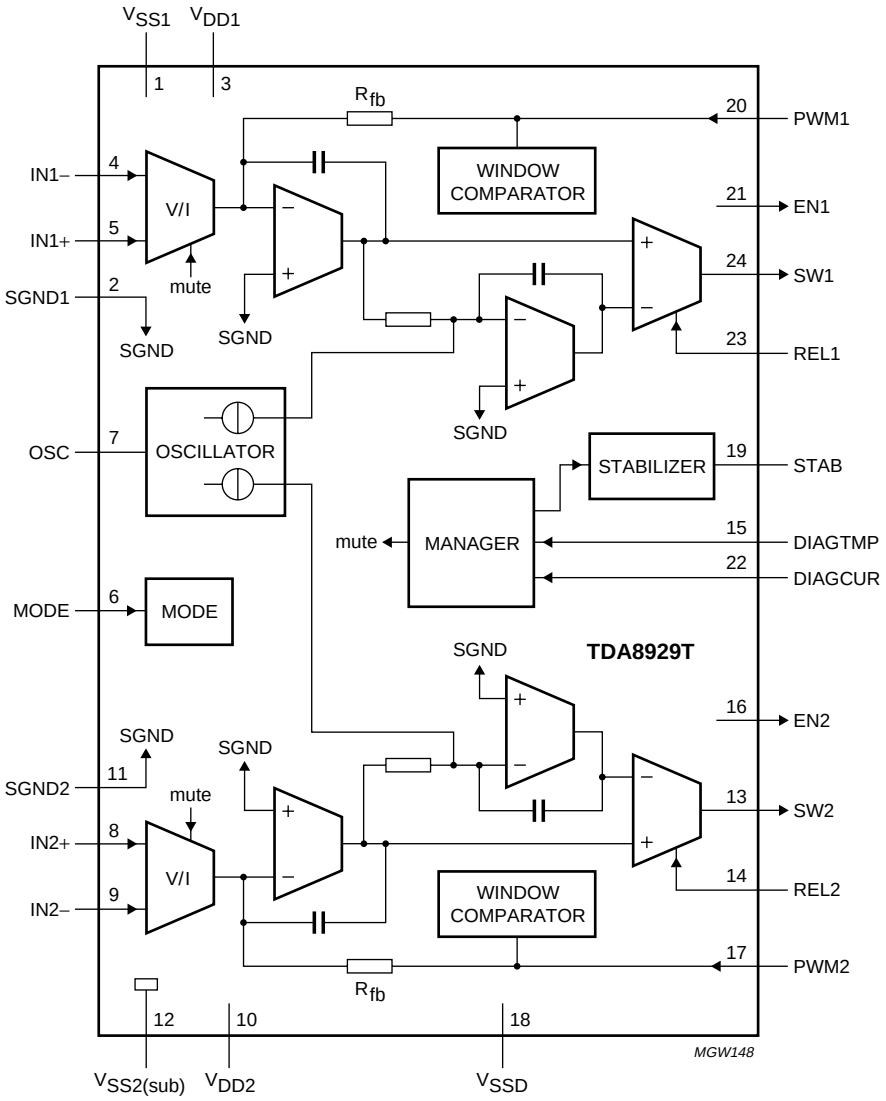


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	DESCRIPTION
V_{SS1}	1	negative analog supply voltage channel 1
SGND1	2	signal ground channel 1
V_{DD1}	3	positive analog supply voltage channel 1
IN1–	4	negative audio input channel 1
IN1+	5	positive audio input channel 1
MODE	6	mode select input (standby/mute/operating)
OSC	7	oscillator frequency adjustment, or tracking input
IN2+	8	positive audio input channel 2
IN2–	9	negative audio input channel 2
V_{DD2}	10	positive analog supply voltage channel 2
SGND2	11	signal ground channel 2
$V_{SS2(sub)}$	12	negative analog supply voltage channel 2 (substrate)
SW2	13	digital switch output channel 2
REL2	14	digital control input channel 2
DIAGTMP	15	digital input for temperature limit error report from power stage
EN2	16	digital control output for enable channel 2 of power stage
PWM2	17	input for feedback from PWM output power stage channel 2
V_{SSD}	18	negative digital supply voltage; reference for digital interface to power stage
STAB	19	pin for a decoupling capacitor for internal stabilizer
PWM1	20	input for feedback from PWM output power stage channel 1
EN1	21	digital control output for enable channel 1 of power stage
DIAGCUR	22	digital input for current error report from power stage
REL1	23	digital control input channel 1
SW1	24	digital switch output channel 1

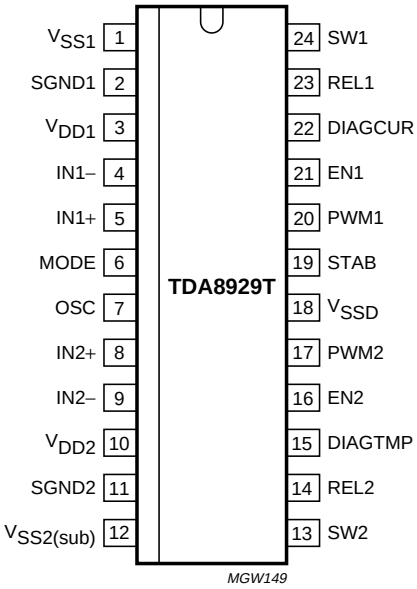


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

The combination of the TDA8926J and the TDA8929T produces a two-channel audio power amplifier system using the class-D technology (see Fig.4).

In the TDA8929T controller device the analog audio input signal is converted into a digital Pulse Width Modulation (PWM) signal. The digital power stage (TDA8926) is used for driving the low-pass filter and the loudspeaker load. It performs a level shift from the low-power digital PWM signal, at logic levels, to a high-power PWM signal that switches between the main supply lines.
A second-order low-pass filter converts the PWM signal into an analog audio signal across the loudspeaker.

For a description of the power stage see the specification of the TDA8926.

The TDA8926 can be used for an output power of 2×50 W. The TDA8927 should be used for a higher output power of 2×100 W.

8.1 Controller

The controller contains (for two audio channels) two Pulse Width Modulators (PWMs), two analog feedback loops and two differential input stages. This chip also contains circuits common to both channels such as the oscillator, all reference sources, the mode functionality and a digital timing manager.

The pinning of the TDA8929T and the power stage devices are designed to have very short and straight connections between the packages. For optimum performance the interconnections between the packages must be as short as possible.

Using this two-chip set an audio system with two independent amplifier channels with high output power, high efficiency (90%) for the system, low distortion and a low quiescent current is obtained. The amplifiers channels can be connected in the following configurations:

- Mono Bridge-Tied Load (BTL) amplifier
- Stereo Single-Ended (SE) amplifier.

The amplifier system can be switched in three operating modes via the mode select pin:

- Standby: with a very low supply current
- Mute: the amplifiers are operational, but the audio signal at the output is suppressed
- On: amplifier fully operational with output signal.

For suppressing pop noise the amplifier will remain automatically for approximately 220 ms in the mute mode before switching to operating mode. In this time the coupling capacitors at the input are fully charged.

Figure 3 shows an example of a switching circuit for driving pin MODE.

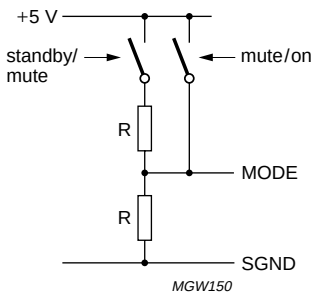


Fig.3 Mode select switch circuitry.

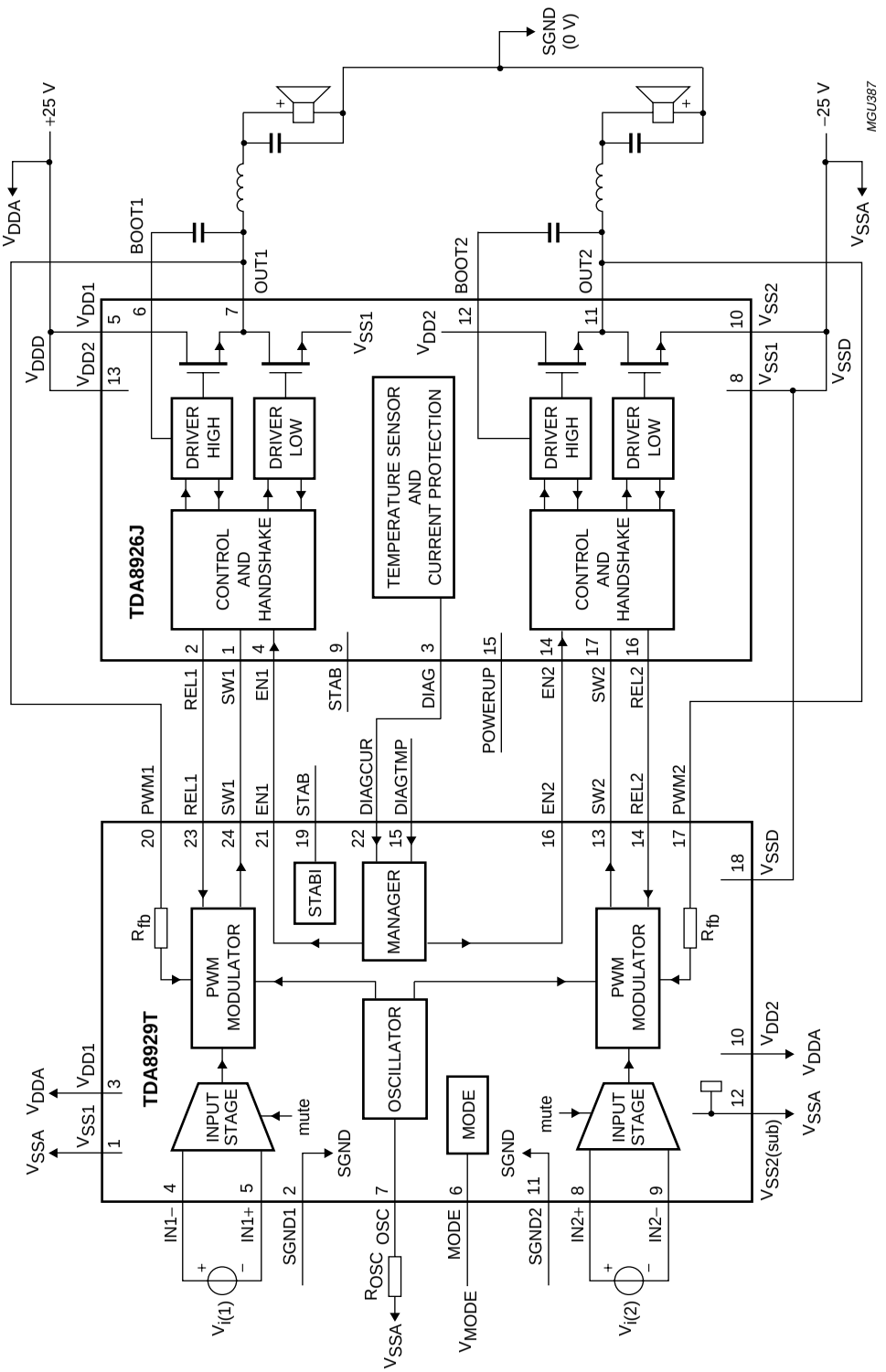


Fig.4 Typical application schematic of the class-D system using TDA8929T and the TDA8926J.

8.2 Pulse width modulation frequency

The output signal of the power stage is a PWM signal with a carrier frequency of approximately 300 kHz. Using a second-order LC demodulation filter in the application results in an analog audio signal across the loudspeaker. This switching frequency is fixed by an external resistor R_{OSC} connected between pin OSC and V_{SS}. With the resistor value given in the application diagram, the carrier frequency is typical 317 kHz. The carrier frequency can be calculated using: $f_{osc} = \frac{9 \times 10^9}{R_{OSC}}$ [Hz]

If two or more class-D systems are used in the same audio application, it is advised to have all devices working at the same switching frequency. This can be realized by connecting all OSC pins together and feed them from an external oscillator. Using an external oscillator it is necessary to force pin OSC to a DC-level above SGND for switching from the internal to an external oscillator. In this case the internal oscillator is disabled and the PWM will switch on the external frequency. The frequency range of the external oscillator must be in the range as specified in the switching characteristics.

Application in a practical circuit:

- Internal oscillator: R_{OSC} connected between pin OSC and V_{SS}
- External oscillator: connect oscillator signal between pin OSC and pin SGND; delete R_{OSC}.

8.3 Protections

The controller is provided with two diagnostic inputs. One or both pins can be connected to the diagnostic output of one or more power stages.

8.3.1 DIAGNOSTIC TEMPERATURE

A LOW level on pin DIAGTMP will immediately force both pins EN1 and EN2 to a LOW level. The power stage shuts down and the temperature is expected to drop. If pin DIAGTMP goes HIGH, pins EN1 and EN2 will immediately go HIGH and normal operation will be maintained.

Temperature hysteresis, a delay before enabling the system again, is arranged in the power stage. Internally there is a pull-up resistance to 5 V at the diagnostic input of the controller. Because the diagnostic output of the power stage is an open-drain output, diagnostic lines can be connected together (wired-OR). It should be noted that the TDA8929T itself has no temperature protection.

8.3.2 DIAGNOSTIC CURRENT

This input is intended to protect against short-circuits across the loudspeaker load. In the event that the current limit in the power stage is exceeded, pin DIAGCUR must be pulled to a LOW level. A LOW level on the diagnostic current input will immediately force the output pins EN1 and EN2 to a LOW level. The power stage will shut down within less than 1 μs and the high current is switched off. In this state the dissipation is very low. Every 220 ms the controller will attempt to restart the system. If there is still a short-circuit across the loudspeaker load, the system is switched off again as soon as the maximum current is exceeded. The average dissipation will be low because of this low duty factor. The actual current limiting value is set by the power stage.

Depending on the type of power stage which is used, several values are possible:

- TDA8926TH: limit value can be externally adjusted with a resistor; maximum is 5 A
- TDA8927TH: limit value can be externally adjusted with a resistor; maximum is 7.5 A
- TDA8926J and TDA8926ST: limit value is fixed at 5 A
- TDA8927J and TDA8927ST: limit value is fixed at 7.5 A.

8.3.3 START-UP SAFETY TEST

During the start-up sequence, when pin MODE is switched from standby to mute, the condition at the output terminals of the power stage are checked. These are the same lines as the feedback inputs of the controller. In the event of a short-circuit of one of the output terminals to V_{DD} or V_{SS} the start-up procedure is interrupted and the system waits for non-shorted outputs. Because the test is done before enabling the power stages, no large currents will flow in the event of a short-circuit. This system protects against short-circuits at both sides of the output filter to both supply lines. When there is a short-circuit from the outputs of the power stage to one of the supply lines, before the demodulation filter, it will also be detected by the start-up safety test. Practical use from this test feature can be found in detection of short-circuits on the printed-circuit board.

Remark: this test is only operational prior to or during the start-up sequence, and not during normal operating.

8.4 Differential audio inputs

For a high common mode rejection and a maximum flexibility of application, the audio inputs are fully differential. By connecting the inputs anti-parallel the phase of one of the channels is inverted, so that a load can be connected between the two output filters. In this case the system operates as a mono BTL amplifier (see Fig.5).

Also in the stereo single-ended configuration it is recommended to connect the two differential inputs in anti-phase. This has advantages for the current handling of the power supply at low signal frequencies.

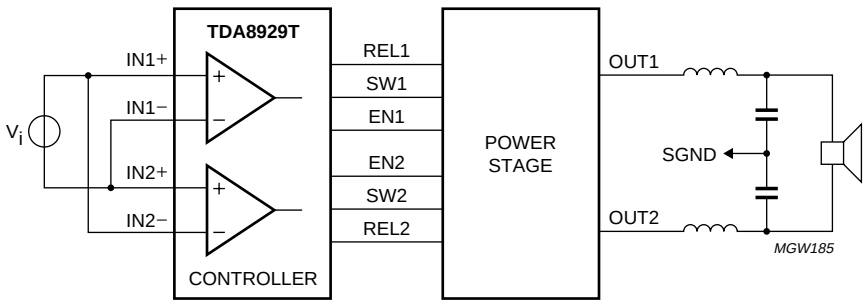


Fig.5 Mono BTL application.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rate System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	±30	V
$V_{MODE(sw)}$	mode select switch voltage	referenced to SGND	0	5.5	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_{vj}	virtual junction temperature		–	150	°C
$V_{es(HBM)}$	electrostatic discharge voltage (HBM)	note 1			
		all pins with respect to V_{DD} (class A)	–500	+500	V
		all pins with respect to V_{SS} (class A1)	–1000	+1000	V
		all pins with respect to GND (class B)	–2500	+2500	V
		all pins with respect to each other (class B)	–2000	+2000	V
$V_{es(MM)}$	electrostatic discharge voltage (MM)	note 2			
		all pins with respect to V_{DD} (class A)	–100	+100	V
		all pins with respect to V_{SS} (class B)	–100	+100	V
		all pins with respect to GND (class B)	–300	+300	V
		all pins with respect to each other (class B)	–200	+200	V

Notes

1. Human Body Model (HBM); R_S = 1500 Ω and C = 100 pF.
2. Machine Model (MM); R_S = 10 Ω; C = 200 pF and L = 0.75 μH.

10 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	65	K/W

11 QUALITY SPECIFICATION

In accordance with *"SNW-FQ611-part D"* if this device is used as an audio amplifier.

12 DC CHARACTERISTICS

V_P = ±25 V; T_{amb} = 25 °C; measured in Fig.10; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	±15	±25	±30	V
$I_{q(tot)}$	total quiescent current		–	20	30	mA
I_{stb}	standby current	V_{MODE} = 0 V	–	30	100	μA
Offset						
$\lvert V_{OO} \rvert$	output offset voltage in system	on and mute	–	–	150	mV
$\lvert \Delta V_{OO} \rvert$	delta output offset voltage in system	on ↔ mute	–	–	80	mV
Mode select input (pin MODE); see Figs 6, 7 and 8						
V_{MODE}	input voltage	note 2	0	–	5.5	V
I_{MODE}	input current	V_{MODE} = 5.5 V	–	–	1000	μA
V_{th1+}	positive threshold voltage 1	standby → mute; note 2	–	1.6	2.0	V
V_{th1-}	negative threshold voltage 1	mute → standby; note 2	0.8	1.0	–	V
$V_{MODE(hys1)}$	hysteresis voltage 1	$\lvert (V_{th1+}) - (V_{th1-}) \rvert$	–	600	–	mV
V_{th2+}	positive threshold voltage 2	mute → on; note 2	–	3.8	4.0	V
V_{th2-}	negative threshold voltage 2	on → mute; note 2	3.0	3.2	–	V
$V_{MODE(hys2)}$	hysteresis voltage 2	$\lvert (V_{th2+}) - (V_{th2-}) \rvert$	–	600	–	mV
Audio inputs (pins IN1+, IN1–, IN2+ and IN2–)						
V_I	DC input voltage	note 2	–	0	–	V
Internal stabilizer (pin STAB)						
$V_{O(STAB)}$	stabilizer output voltage	mute and on; note 3	11	13	15	V
$I_{STAB(max)}$	maximum current on pin STAB	mute and on	10	–	–	mA
Enable outputs (pins EN1 and EN2)						
V_{OH}	HIGH-level output voltage	referenced to V_{SS}	V_{STAB} – 1.6	V_{STAB} – 0.7	–	V
V_{OL}	LOW-level output voltage	referenced to V_{SS}	0	–	0.8	V
Current diagnose input (pin DIAGCUR with internal pull-up resistance)						
V_{IH}	HIGH-level input voltage	no errors; note 3	–	V_{STAB}	–	V
V_{IL}	LOW-level input voltage	note 3	0	–	1.5	V
$R_{pu(int)}$	internal pull-up resistance to internal digital supply		–	12	–	kΩ
Temperature diagnose input (pin DIAGTMP with internal pull-up resistance)						
V_{IH}	HIGH-level input voltage	no errors; note 3	4	5.5		V
V_{IL}	LOW-level input voltage	note 3	0	–	1.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{pu(int)}$	internal pull-up resistance to internal digital supply		–	12	–	kΩ
Switch outputs (pins SW1 and SW2)						
V_{OH}	HIGH-level output voltage	note 3	V_{STAB} – 1.6	V_{STAB} – 0.7	–	V
V_{OL}	LOW-level output voltage	note 3	0	–	0.8	V
Control inputs (pins REL1 and REL2)						
V_{IH}	HIGH-level input voltage	note 3	10	–	V_{STAB}	V
V_{IL}	LOW-level input voltage	note 3	0	–	2	V

Notes

1. The circuit is DC adjusted at V_P = ±15 to ±30 V.
2. Referenced to SGND (0 V).
3. Referenced to V_{SS}.

13 AC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Stereo single-ended application; note 1						
THD	total harmonic distortion	P_o = 1 W; note 2				
		f_i = 1 kHz	–	0.01	0.05	%
		f_i = 10 kHz	–	0.1	–	%
$G_{v(cl)}$	closed-loop voltage gain		29	30	31	dB
SVRR	supply voltage ripple rejection	on; f_i = 100 Hz; note 3	–	55	–	dB
		on; f_i = 1 kHz; note 3	40	50	–	dB
		mute; f_i = 100 Hz; note 3	–	55	–	dB
		standby; f_i = 100 Hz; note 3	–	80	–	dB
$\lvert Z_i \rvert$	input impedance		45	68	–	kΩ
$V_{n(o)}$	noise output voltage	on; R_s = 0 Ω; B = 22 Hz to 22 kHz	–	220	400	μV
		on; R_s = 10 kΩ; B = 22 Hz to 22 kHz	–	230	–	μV
		mute; note 4	–	220	–	μV
α_{cs}	channel separation	P_o = 10 W; R_s = 0 Ω	–	70	–	dB
$\lvert \Delta G_v \rvert$	channel unbalance		–	–	1	dB
V_o	output signal	mute; $V_i = V_{i(max)}$ = 1 V (RMS)	–	–	400	μV
CMRR	common mode rejection ratio	V_i = 1 V (RMS)	–	75	–	dB
Mono BTL application; note 5						
THD	total harmonic distortion	P_o = 1 W; note 2				
		f_i = 1 kHz	–	0.01	0.05	%
		f_i = 10 kHz	–	0.1	–	%
$G_{v(cl)}$	closed-loop voltage gain		35	36	37	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SVRR	supply voltage ripple rejection	on; f_i = 100 Hz; note 3	–	49	–	dB
		on; f_i = 1 kHz; note 3	36	44	–	dB
		mute; f_i = 100 Hz; note 3	–	49	–	dB
		standby; f_i = 100 Hz; note 3	–	80	–	dB
$\lvert Z_i \rvert$	input impedance		23	34	–	kΩ
$V_{n(o)}$	noise output voltage	on; R_s = 0 Ω; B = 22 Hz to 22 kHz	–	280	500	μV
		on; R_s = 10 kΩ; B = 22 Hz to 22 kHz	–	300	–	μV
		mute; note 4	–	280	–	μV
V_o	output signal	mute; $V_i = V_{i(max)}$ = 1 V (RMS)	–	–	500	μV
CMRR	common mode rejection ratio	V_i = 1 V (RMS)	–	75	–	dB

Notes

1. V_P = ±25 V; f_i = 1 kHz; T_{amb} = 25 °C; measured in Fig.10; unless otherwise specified.
2. THD is measured in a bandwidth of 22 Hz to 22 kHz. When distortion is measured using a low-order low-pass filter a significantly higher value will be found, due to the switching frequency outside the audio band.
3. $V_{ripple} = V_{ripple(max)}$ = 2 V (p-p); R_s = 0 Ω.
4. B = 22 Hz to 22 kHz and independent of R_s.
5. V_P = ±25 V; f_i = 1 kHz; T_{amb} = 25 °C; measured in reference design in Fig.12; unless otherwise specified.

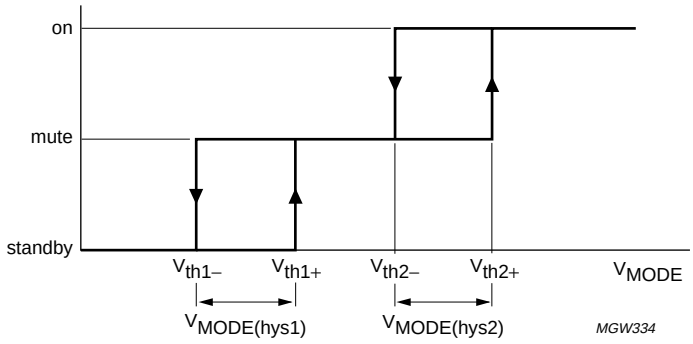
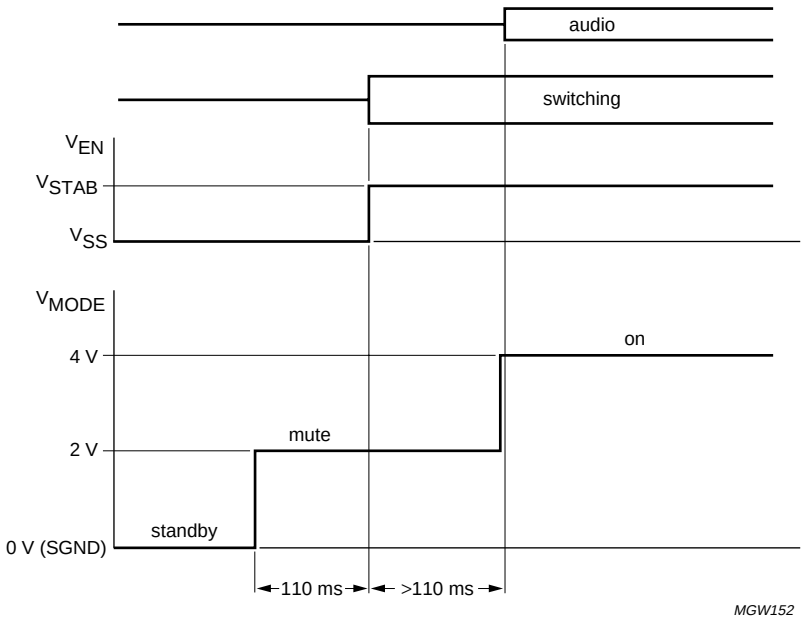
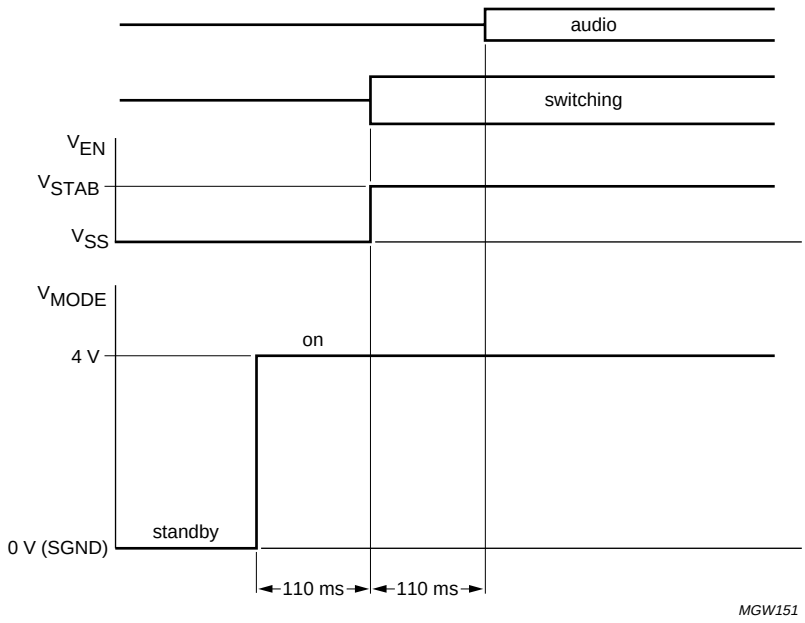


Fig.6 Mode pin selection.



When switching from standby to mute there is a delay of 110 ms before the output starts switching. The audio signal is available after the mode pin has been set to on, but not earlier than 220 ms after switching to mute.

Fig.7 Mode pin timing from standby to on via mute.



When switching from standby to on there is a delay of 110 ms before the output starts switching.
After a second delay of 110 ms the audio signal is available.

Fig.8 Mode pin timing from standby to on.

14 SWITCHING CHARACTERISTICS

V_P = ±25 V; T_{amb} = 25 °C; measured in Fig.10; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching frequency						
f_{osc}	oscillator frequency	R_{OSC} = 30.0 kΩ	309	317	329	kHz
		R_{OSC} = 27 kΩ; see Fig.12	–	360	–	kHz
$f_{osc(r)}$	oscillator frequency range	note 1	210	–	600	kHz
V_{OSC}	maximum voltage at pin OSC	frequency tracking	–	–	SGND + 12	V
$V_{OSC(trip)}$	trip level at pin OSC for tracking	frequency tracking	–	SGND + 2.5	–	V
f_{track}	frequency range for tracking	frequency tracking	200	–	600	kHz
$V_{OSC(ext)}$	voltage at pin OSC for tracking	note 2	–	5	–	V

Notes

1. Frequency set with R_{OSC}, according to the formula in the functional description.
2. For tracking the external oscillator has to switch around SGND + 2.5 V with a minimum voltage of $V_{OSC(ext)}$.

14.1 Minimum pulse width

The minimum obtainable pulse width of the PWM output signal of a class-D system, sets the maximum output voltage swing after the demodulation filter and also the maximum output power. Delays in the power stages are the main cause for the minimum pulse width being not equal to zero. The TDA8926 and TDA8927 power stages have a minimum pulse width of $t_{W(min)}$ = 220 ns (typical). Using the TDA8929T controller, the effective minimum pulse is reduced by a factor of two during clipping. For the calculation of the maximum output power at clipping the effective minimum pulse width during clipping is $0.5t_{W(min)}$.

For the practical useable minimum and maximum duty factor (δ) which determines the maximum output power:

$$\frac{t_{W(min)} \times f_{osc}}{2} \times 100\% < \delta < \left(1 - \frac{t_{W(min)} \times f_{osc}}{2}\right) \times 100\%$$

Using the typical values of the TDA8926 and TDA8927 power stages:

3.5% < δ < 96.5%.

15 TEST AND APPLICATION INFORMATION

15.1 Test circuit

The test diagram in Fig.10 can be used for stand alone testing of the controller. Audio and mode input pins are configured as in the application. For the simulation of a switching output power stage a simple level shifter can be used. It converts the digital PWM signal from the controller (switching between V_{SS} and V_{SS} + 12 V level) to a PWM signal switching between V_{DD} and V_{SS}.

A proposal for a simple level shifting circuit is given in Fig.9.

The low-pass filter performs the demodulation, so that the audio signal can be measured with an audio analyzer. For measuring low distortion values, the speed of the level shifter is important. Special care has to be taken at a sufficient supply decoupling and output waveforms without ringing.

The handshake with the power stage is simulated by a direct connection of the release inputs (REL1 and REL2) with the switch outputs (SW1 and SW2) of the controller. The enable outputs (EN1 and EN2) for waking-up the power stage are not used here, only the output level and timing are measured.

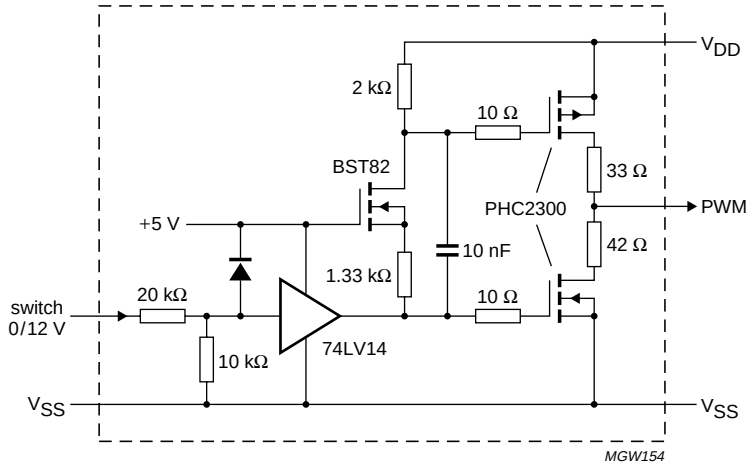


Fig.9 Level shifter.

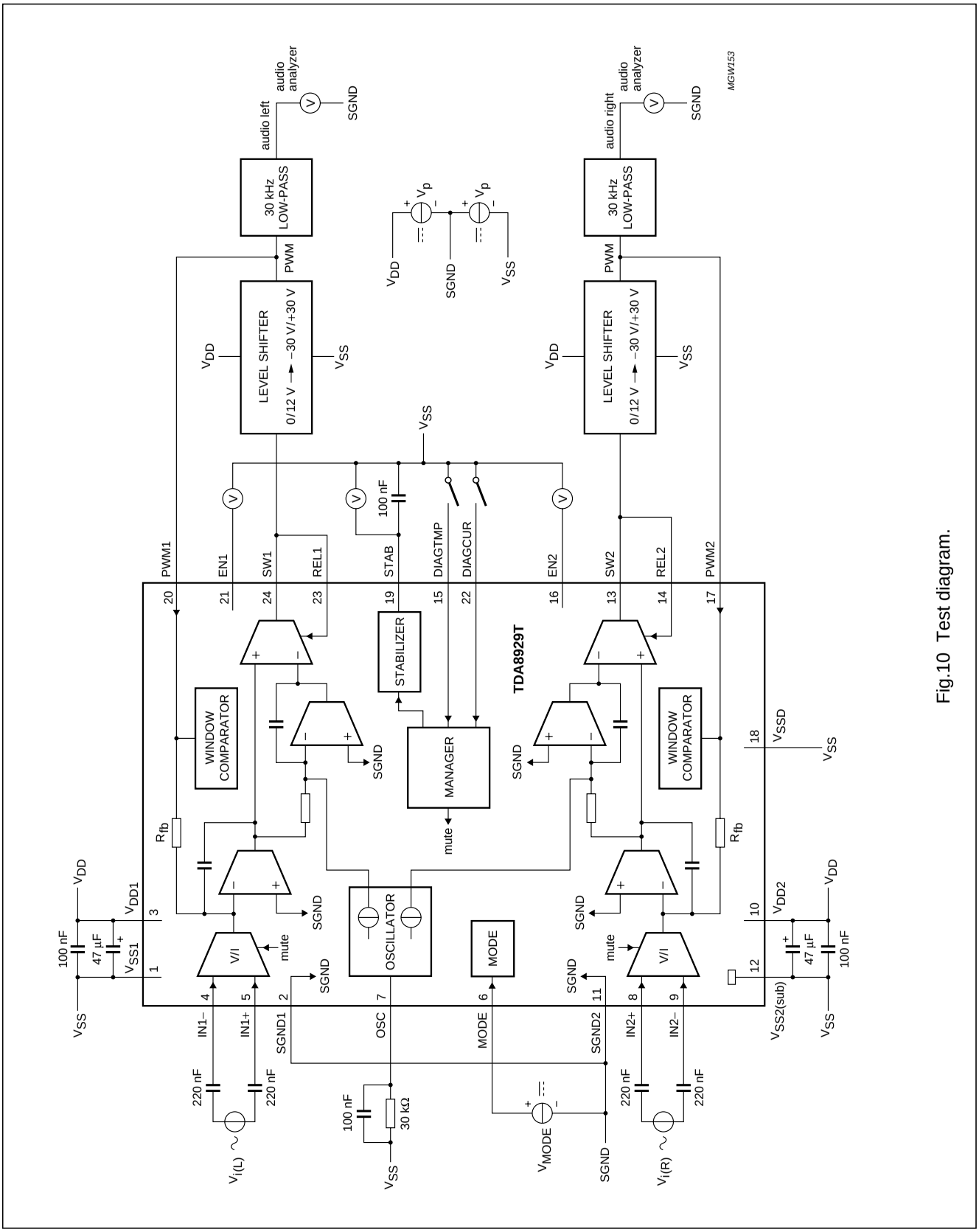


Fig.10 Test diagram.

15.2 BTL application

When using the system in a mono BTL application (for more output power), the inputs of both channels must be connected in parallel. The phase of one the inputs must be inverted (see Fig.5). In principle the loudspeaker can be connected between the outputs of the two single-ended demodulation filters. For improving the common mode behavior of the filter, the configuration in Fig.12 is advised.

15.3 Mode pin

For correct operation the switching voltage on pin MODE should be de-bounced. If this pin is driven by a mechanical switch an appropriate de-bouncing low-pass filter should be used. If pin MODE is driven by an electronic circuit or microcontroller then it should remain, for at least 100 ms, at the mute voltage level (V_{th1+}) before switching back to the standby voltage level.

15.4 External clock

Figure 11 shows an external clock oscillator circuit.

15.5 Reference designs

The reference design for a two-chip class-D audio amplifier for TDA8926J or TDA8927J and TDA8929T is shown in Fig.12. The Printed-Circuit Board (PCB) layout is shown in Fig.13. The bill of materials is given in Table 1.

The reference design for a two-chip class-D audio amplifier for TDA8926TH or TDA8927TH and TDA8929T is shown in Fig.14. The PCB layout is shown in Fig.15.

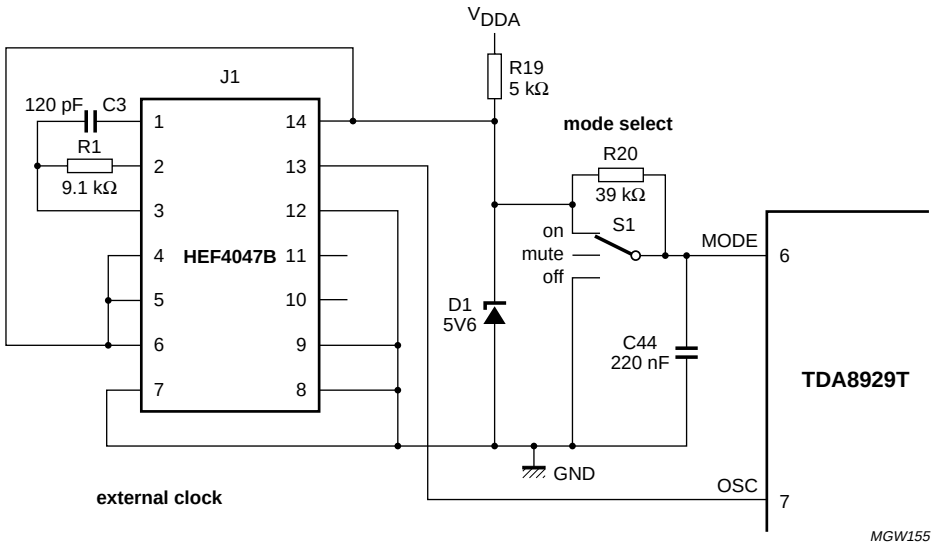
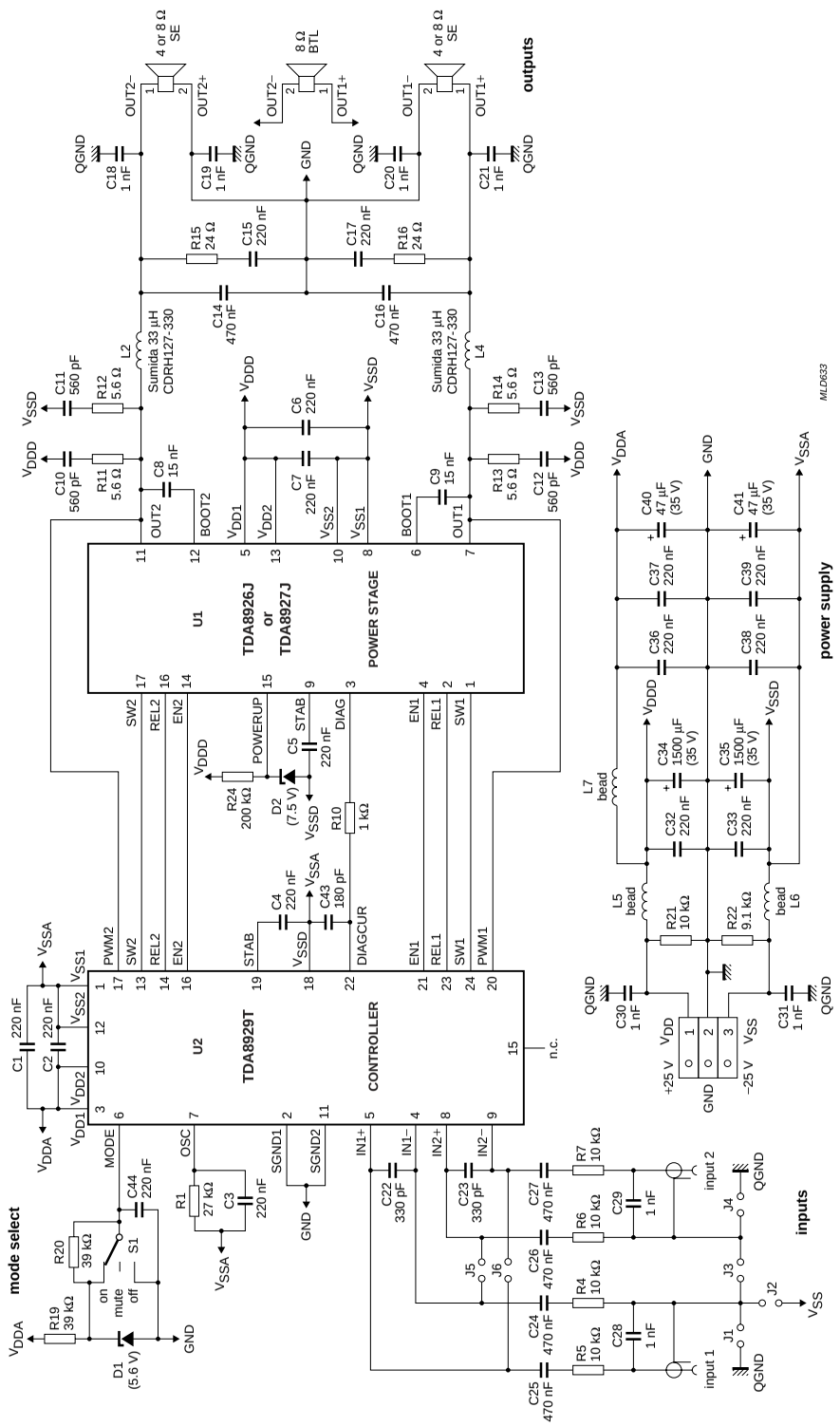


Fig.11 External oscillator circuit.



R21 and R22 are only necessary in BTL applications with asymmetrical supply.

BTL: remove R6, R7, C23, C26 and C27 and close J5 and J6.

C22 and C23 influence the low-pass frequency response and should be tuned with the real load (loudspeaker).

Inputs floating or inputs referenced to QGND (close J1 and J4) or referenced to V_{SS} (close J2 and J3) for an input signal ground reference.

Fig.12 Two-chip class-D audio amplifier application diagram for TDA8926J or TDA8927J and TDA8929T.

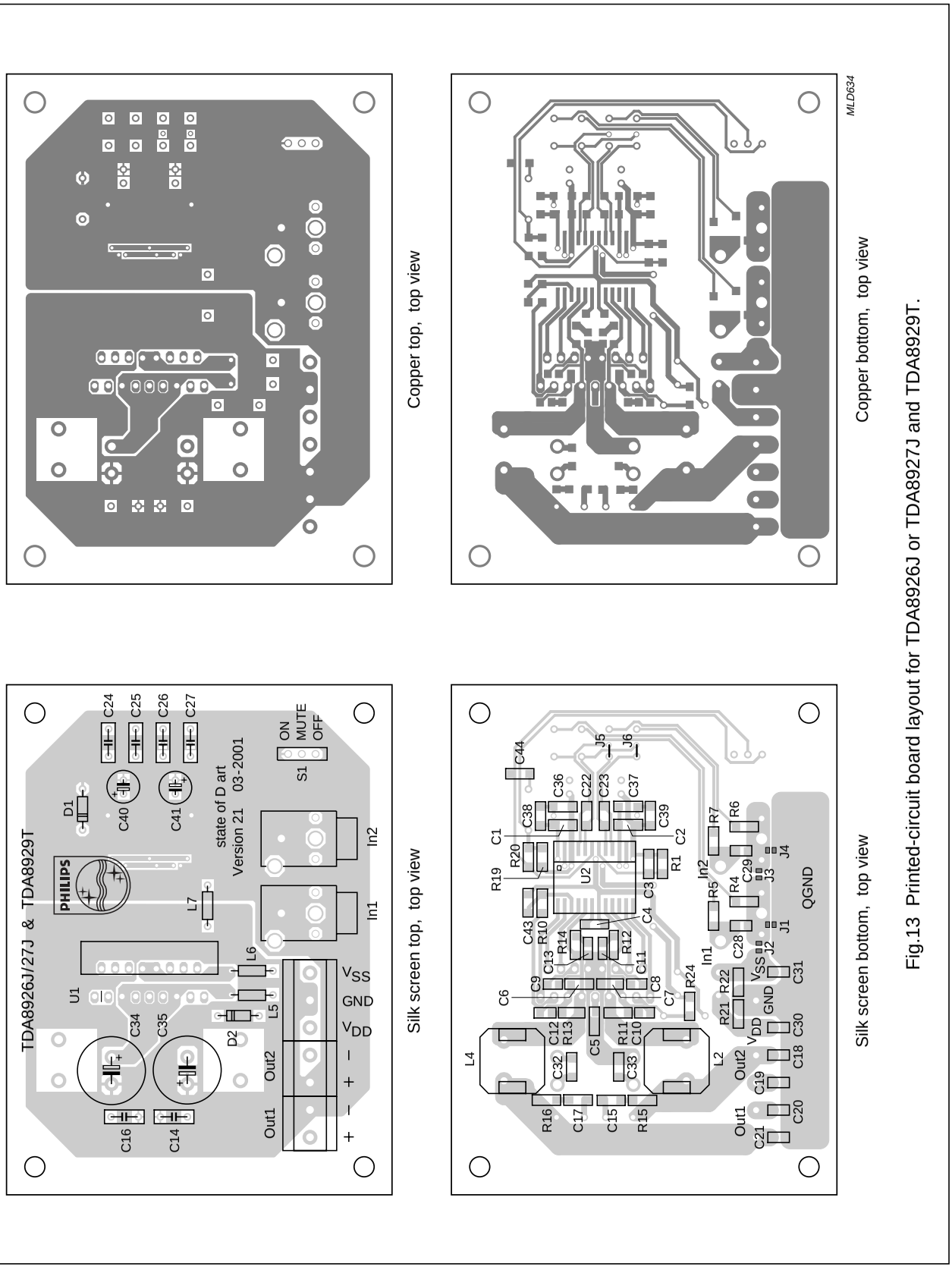


Fig.13 Printed-circuit board layout for TDA8926J or TDA8927J and TDA8929T.

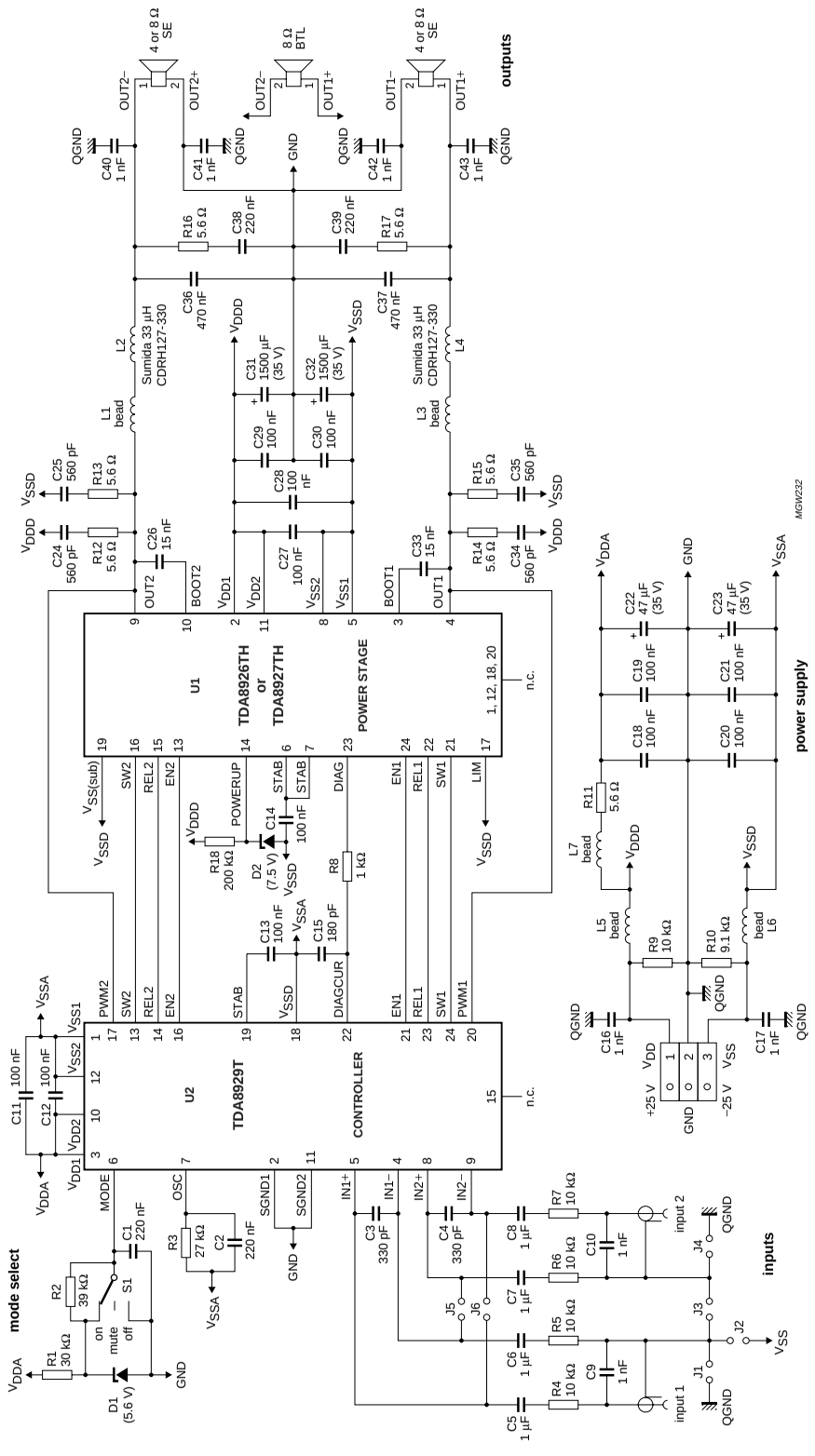


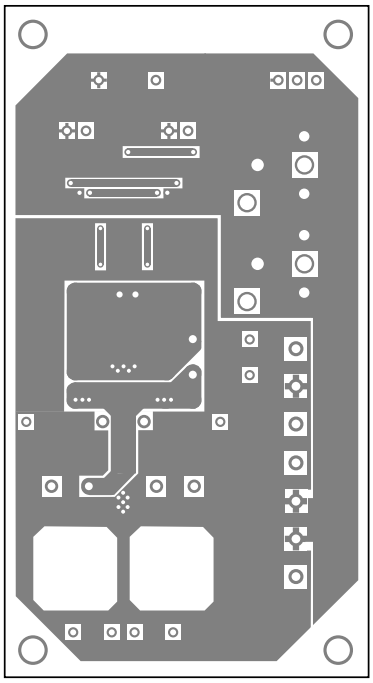
Fig.14 Two-chip class-D audio amplifier application diagram for TDA8926TH or TDA8927TH and TDA8929T.

R9 and R10 are only necessary in BTL applications with asymmetrical supply.

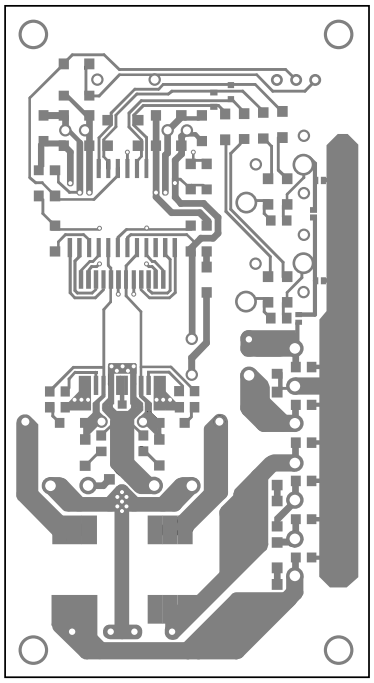
BTL: remove R6, R7, C4, C7 and C8 and close J5 and J6.

Demodulation coils L2 and L4 should be matched in BTL.

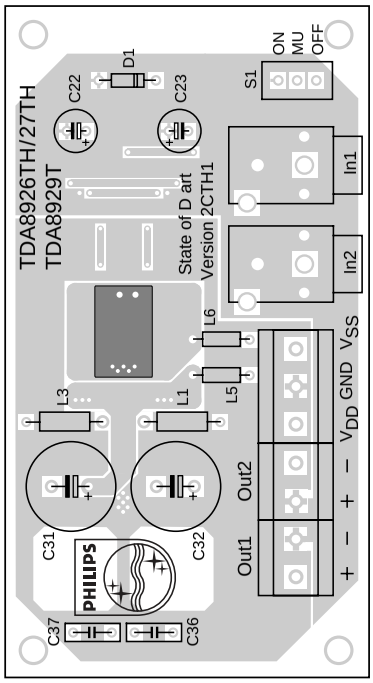
Inputs floating or inputs referenced to QGND (close J1 and J4) or referenced to V_{SS} (close J2 and J3).



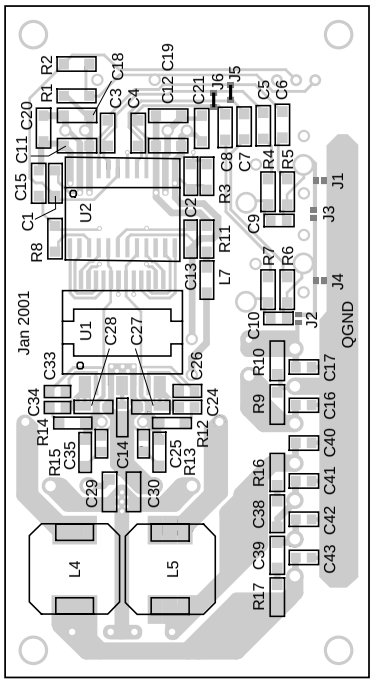
Copper top, top view



Copper bottom, top view



Silk screen top, top view



Silk screen bottom, top view

Fig.15 Printed-circuit board layout for TDA8926TH or TDA8927TH and TDA8929T.

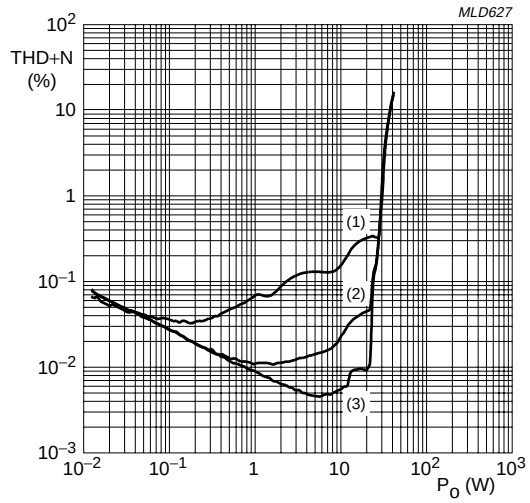
15.6 Reference design bill of material

Table 1 Two-chip class-D audio amplifier PCB (Version 2.1; 03-2001) for TDA8926J or TDA8927J and TDA8929T (see Figs 12 and 13)

COMPONENT	DESCRIPTION	VALUE	COMMENTS
In1 and In2	Cinch input connectors		2 × Farnell: 152-396
Out1, Out2, V_{DD}, GND and V_{SS}	supply/output connectors		2 × Augat 5KEV-02; 1 × Augat 5KEV-03
S1	on/mute/off switch		PCB switch Knitter ATE 1 E M-O-M
U1	power stage IC	TDA8926J/27J	DBS17P package
U2	controller IC	TDA8929T	SO24 package
L2 and L4	demodulation filter coils	33 μH	2 × Sumida CDRH127-330
L5, L6 and L7	power supply ferrite beads		3 × Murata BL01RN1-A62
C1 and C2	supply decoupling capacitors for V_{DD} to V_{SS} of the controller	220 nF/63 V	2 × SMD1206
C3	clock decoupling capacitor	220 nF/63 V	SMD1206
C4	12 V decoupling capacitor of the controller	220 nF/63 V	SMD1206
C5	12 V decoupling capacitor of the power stage	220 nF/63 V	SMD1206
C6 and C7	supply decoupling capacitors for V_{DD} to V_{SS} of the power stage	220 nF/63 V	SMD1206
C8 and C9	bootstrap capacitors	15 nF/50 V	2 × SMD0805
C10, C11, C12 and C13	snubber capacitors	560 pF/100 V	4 × SMD0805
C14 and C16	demodulation filter capacitors	470 nF/63 V	2 × MKT
C15 and C17	resonance suppress capacitors	220 nF/63 V	2 × SMD1206
C18, C19, C20 and C21	common mode HF coupling capacitors	1 nF/50 V	4 × SMD0805
C22 and C23	input filter capacitors	330 pF/50 V	2 × SMD1206
C24, C25, C26 and C27	input capacitors	470 nF/63 V	4 × MKT
C28, C29, C30 and C31	common mode HF coupling capacitors	1 nF/50 V	2 × SMD0805
C32 and C33	power supply decoupling capacitors	220 nF/63 V	2 × SMD1206
C34 and C35	power supply electrolytic capacitors	1500 μF/35 V	2 × Rubycon ZL very low ESR (large switching currents)
C36, C37, C38 and C39	analog supply decoupling capacitors	220 nF/63 V	4 × SMD1206
C40 and C41	analog supply electrolytic capacitors	47 μF/35 V	2 × Rubycon ZA low ESR
C43	diagnostic capacitor	180 pF/50 V	SMD1206
C44	mode capacitor	220 nF/63 V	SMD1206
D1	5.6 V zener diode	BZX79C5V6	DO-35
D2	7.5 V zener diode	BZX79C7V5	DO-35
R1	clock adjustment resistor	27 kΩ	SMD1206

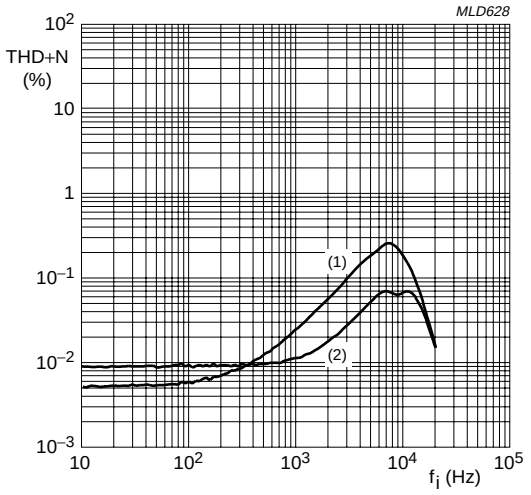
COMPONENT	DESCRIPTION	VALUE	COMMENTS
R4, R5, R6 and R7	input resistors	10 kΩ	4 × SMD1206
R10	diagnostic resistor	1 kΩ	SMD1206
R11, R12, R13 and R14	snubber resistors	5.6 Ω; >0.25 W	4 × SMD1206
R15 and R16	resonance suppression resistors	24 Ω	2 × SMD1206
R19	mode select resistor	39 kΩ	SMD1206
R20	mute select resistor	39 kΩ	SMD1206
R21	resistor needed when using an asymmetrical supply	10 kΩ	SMD1206
R22	resistor needed when using an asymmetrical supply	9.1 kΩ	SMD1206
R24	bias resistor for powering-up the power stage	200 kΩ	SMD1206

15.7 Curves measured in reference design



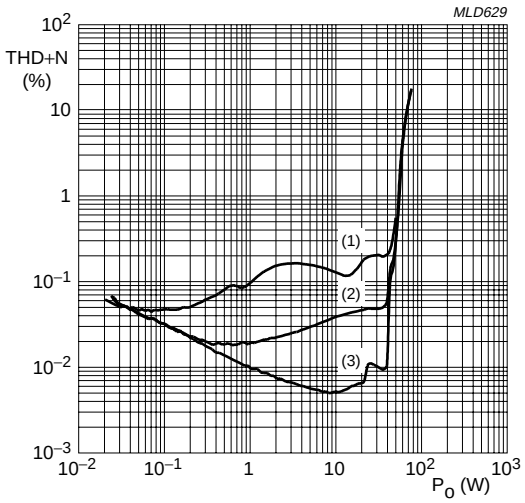
2 × 8 Ω SE; V_P = ±25 V:
(1) 10 kHz.
(2) 1 kHz.
(3) 100 Hz.

Fig.16 THD + N as a function of output power.



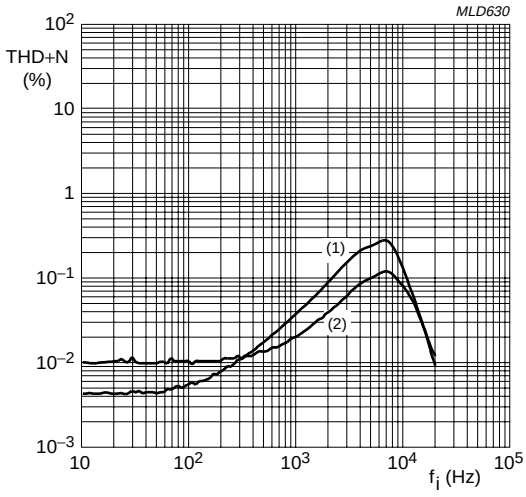
2 × 8 Ω SE; V_P = ±25 V:
(1) P_o = 10 W.
(2) P_o = 1 W.

Fig.17 THD + N as a function of input frequency.



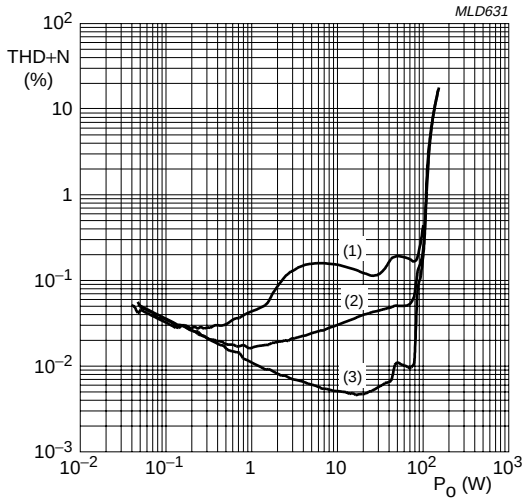
$2 \times 4\ \Omega$ SE; $V_P = \pm 25$ V:
(1) 10 kHz.
(2) 1 kHz.
(3) 100 Hz.

Fig.18 THD + N as a function of output power.



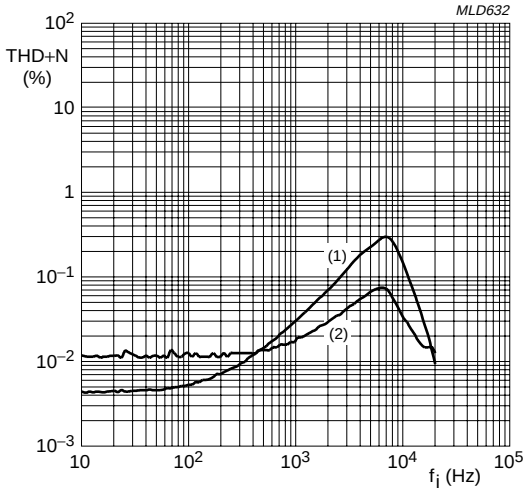
$2 \times 4\ \Omega$ SE; $V_P = \pm 25$ V:
(1) P_o = 10 W.
(2) P_o = 1 W.

Fig.19 THD + N as a function of input frequency.



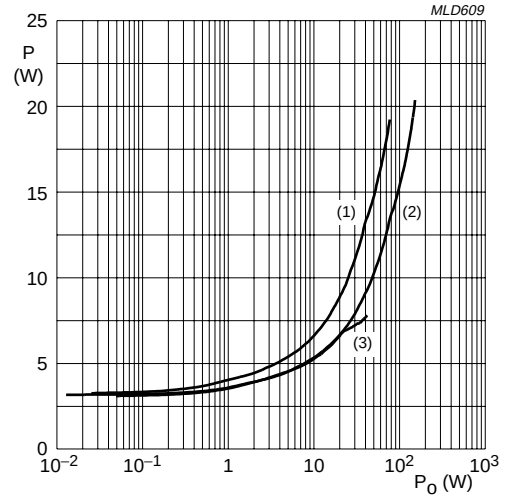
$1 \times 8\ \Omega$ BTL; $V_P = \pm 25$ V:
(1) 10 kHz.
(2) 1 kHz.
(3) 100 Hz.

Fig.20 THD + N as a function of output power.



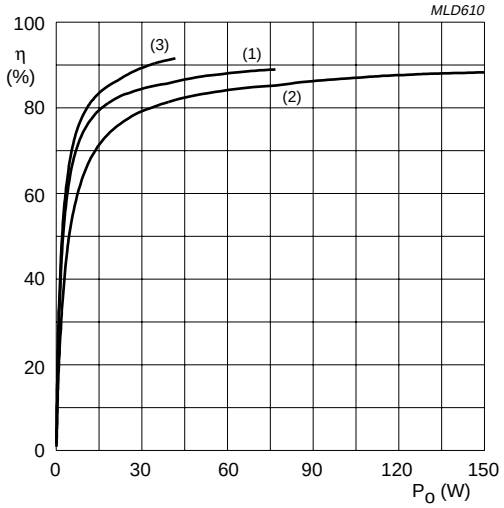
$1 \times 8\ \Omega$ BTL; $V_P = \pm 25$ V:
(1) P_o = 10 W.
(2) P_o = 1 W.

Fig.21 THD + N as a function of input frequency.



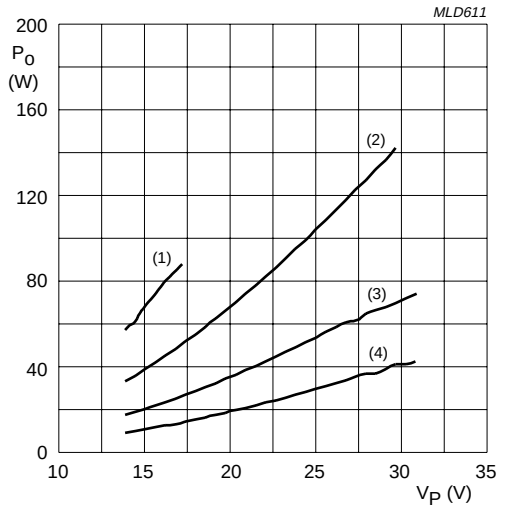
V_P = ±25 V; f_i = 1 kHz:
(1) 2 × 4 Ω SE.
(2) 1 × 8 Ω BTL.
(3) 2 × 8 Ω SE.

Fig.22 Power dissipation as a function of output power.



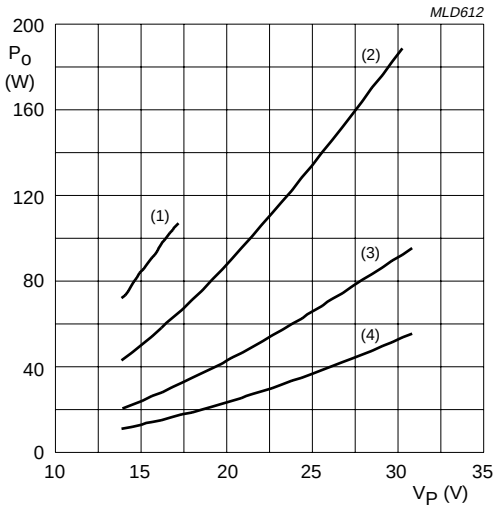
V_P = ±25 V; f_i = 1 kHz:
(1) 2 × 4 Ω SE.
(2) 1 × 8 Ω BTL.
(3) 2 × 8 Ω SE.

Fig.23 Efficiency as a function of output power.



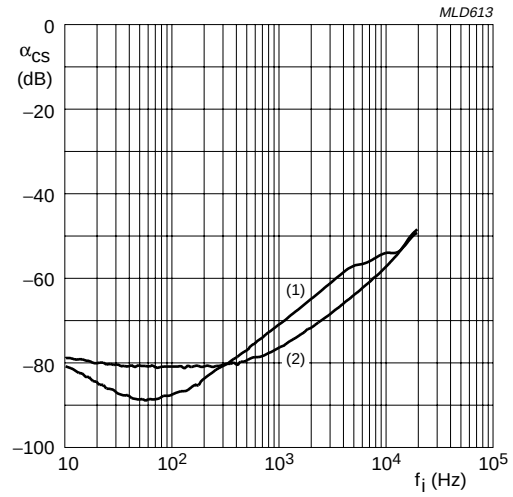
THD + N = 0.5%; f_i = 1 kHz:
(1) 1 × 4 Ω BTL.
(2) 1 × 8 Ω BTL.
(3) 2 × 4 Ω SE.
(4) 2 × 8 Ω SE.

Fig.24 Output power as a function of supply voltage.



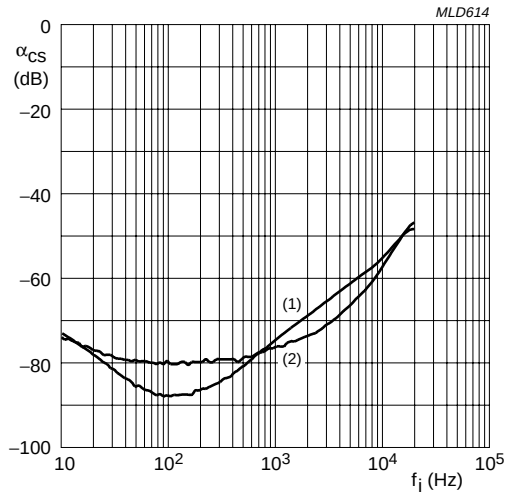
THD + N = 10%; f_i = 1 kHz:
(1) 1 × 4 Ω BTL.
(2) 1 × 8 Ω BTL.
(3) 2 × 4 Ω SE.
(4) 2 × 8 Ω SE.

Fig.25 Output power as a function of supply voltage.



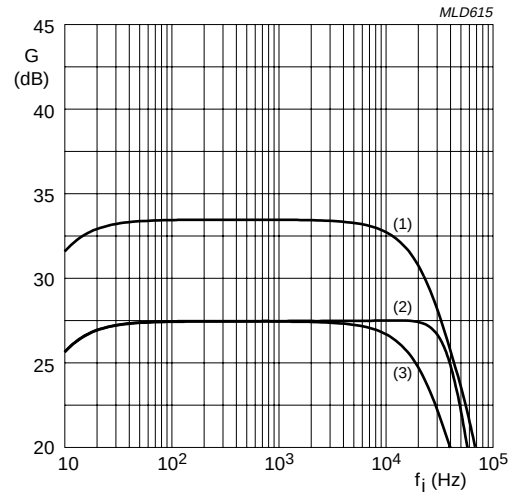
$2 \times 8\ \Omega$ SE; $V_P = \pm 25$ V:
(1) $P_o = 10$ W.
(2) $P_o = 1$ W.

Fig.26 Channel separation as a function of input frequency.



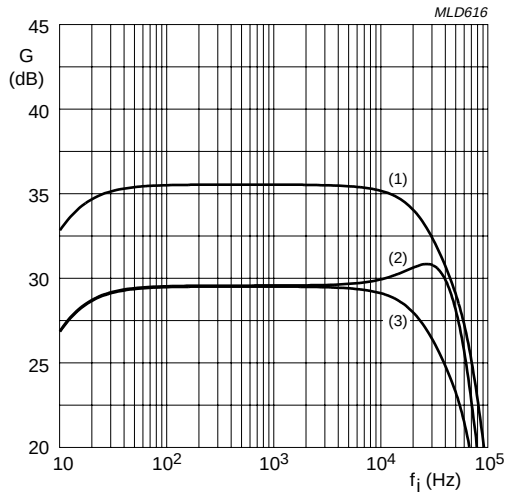
$2 \times 4\ \Omega$ SE; $V_P = \pm 25$ V:
(1) $P_o = 10$ W.
(2) $P_o = 1$ W.

Fig.27 Channel separation as a function of input frequency.



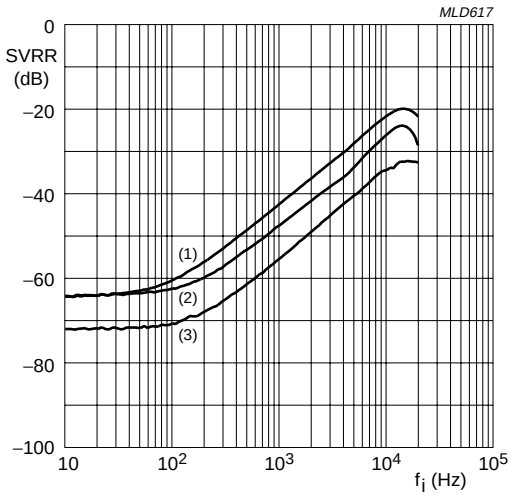
$V_P = \pm 25$ V; $V_i = 100$ mV;
$R_s = 10\ k\Omega / C_i = 330$ pF:
(1) $1 \times 8\ \Omega$ BTL.
(2) $2 \times 8\ \Omega$ SE.
(3) $2 \times 4\ \Omega$ SE.

Fig.28 Gain as a function of input frequency.



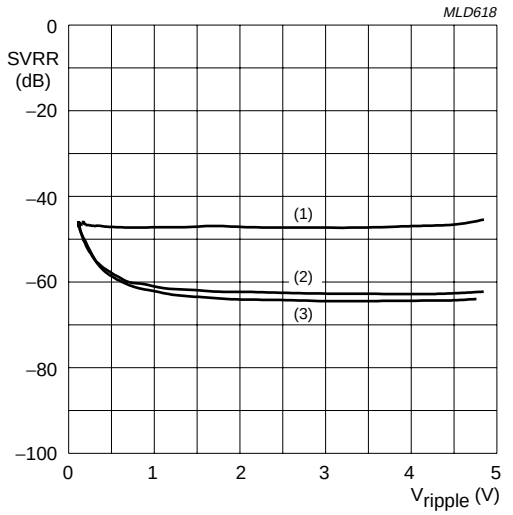
$V_P = \pm 25$ V; $V_i = 100$ mV;
$R_s = 0\ \Omega$:
(1) $1 \times 8\ \Omega$ BTL.
(2) $2 \times 8\ \Omega$ SE.
(3) $2 \times 4\ \Omega$ SE.

Fig.29 Gain as a function of input frequency.



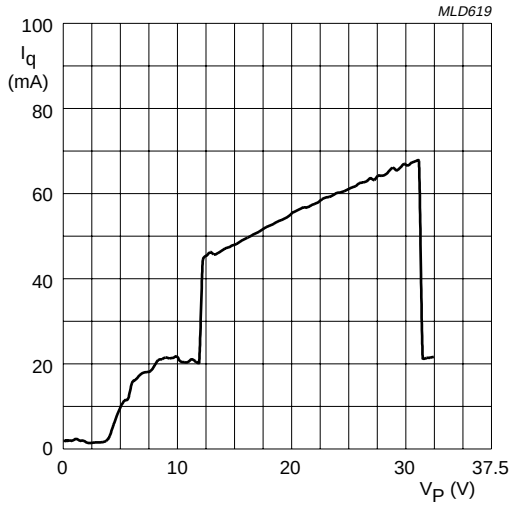
V_P = ±25 V; V_{ripple} = 2 V (p-p) with respect to GND:
(1) Both supply lines in anti-phase.
(2) Both supply lines in phase.
(3) One supply line rippled.

Fig.30 SVRR as a function of input frequency.



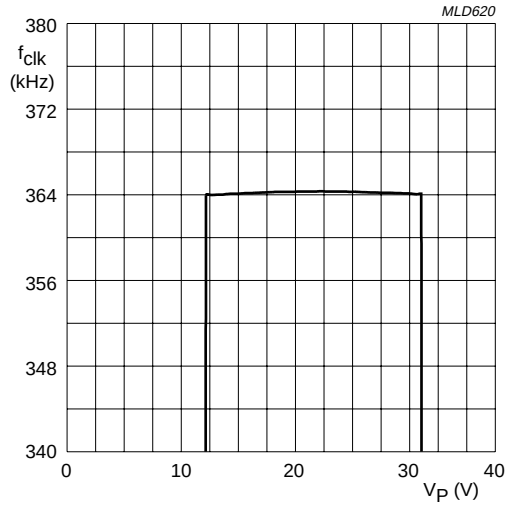
V_P = ±25 V; V_{ripple} with respect to GND:
(1) f_{ripple} = 1 kHz.
(2) f_{ripple} = 100 Hz.
(3) f_{ripple} = 10 Hz.

Fig.31 SVRR as a function of V_{ripple} (p-p).



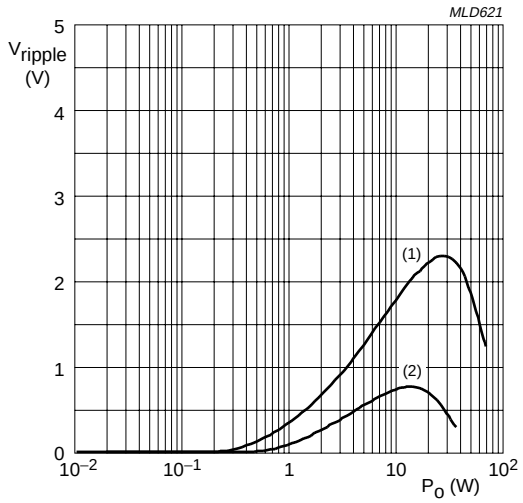
R_L = open.

Fig.32 Quiescent current as a function of supply voltage.



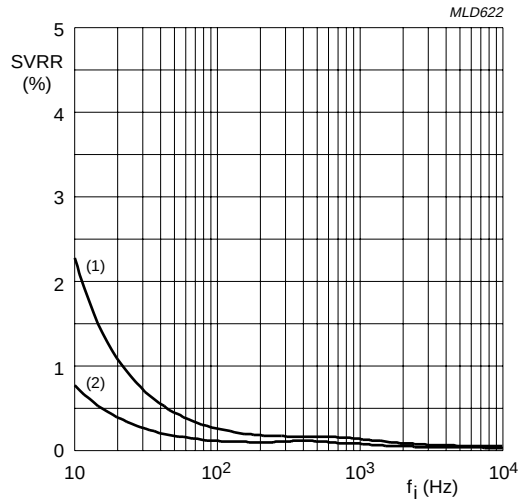
R_L = open.

Fig.33 Clock frequency as a function of supply voltage.



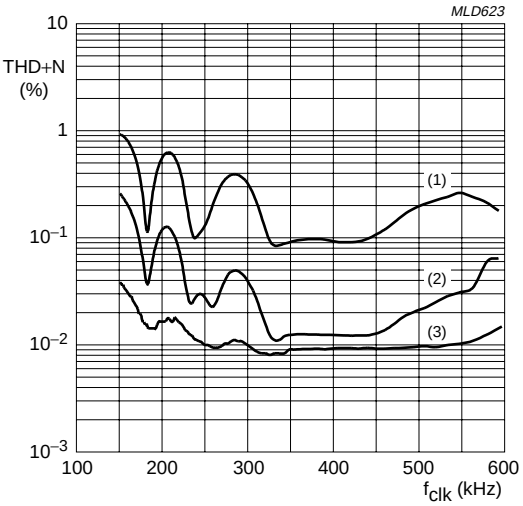
V_P = ±25 V; 1500 μF per supply line; f_i = 10 Hz:
(1) 1 × 4 Ω SE.
(2) 1 × 8 Ω SE.

Fig.34 Supply voltage ripple as a function of output power.



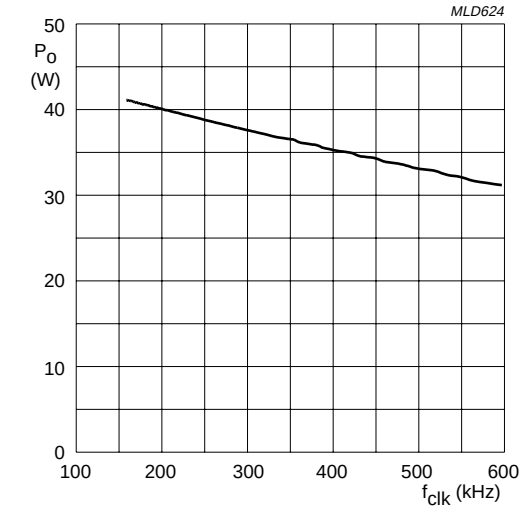
V_P = ±25 V; 1500 μF per supply line:
(1) P_o = 30 W into 1 × 4 Ω SE.
(2) P_o = 15 W into 1 × 8 Ω SE.

Fig.35 SVRR as a function of input frequency.



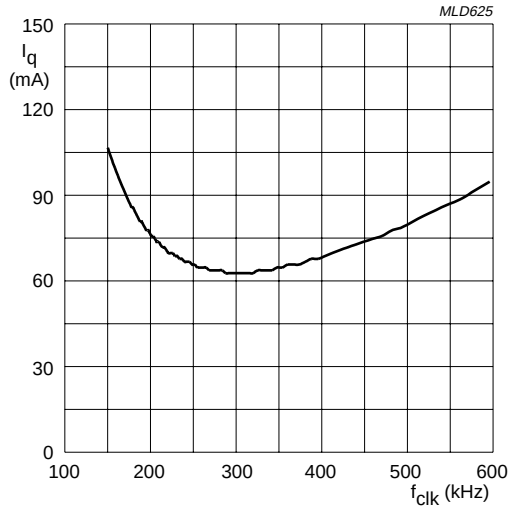
V_P = ±25 V; P_o = 1 W in 2 × 8 Ω:
(1) 10 kHz.
(2) 1 kHz.
(3) 100 Hz.

Fig.36 THD + N as a function of clock frequency.



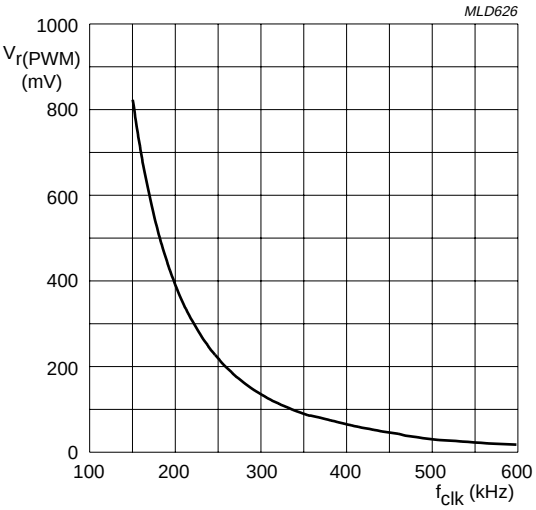
V_P = ±25 V; R_L = 2 × 8 Ω; f_i = 1 kHz; THD + N = 10%.

Fig.37 Output power as a function of clock frequency.



V_P = ±25 V; R_L = open.

Fig.38 Quiescent current as a function of clock frequency.

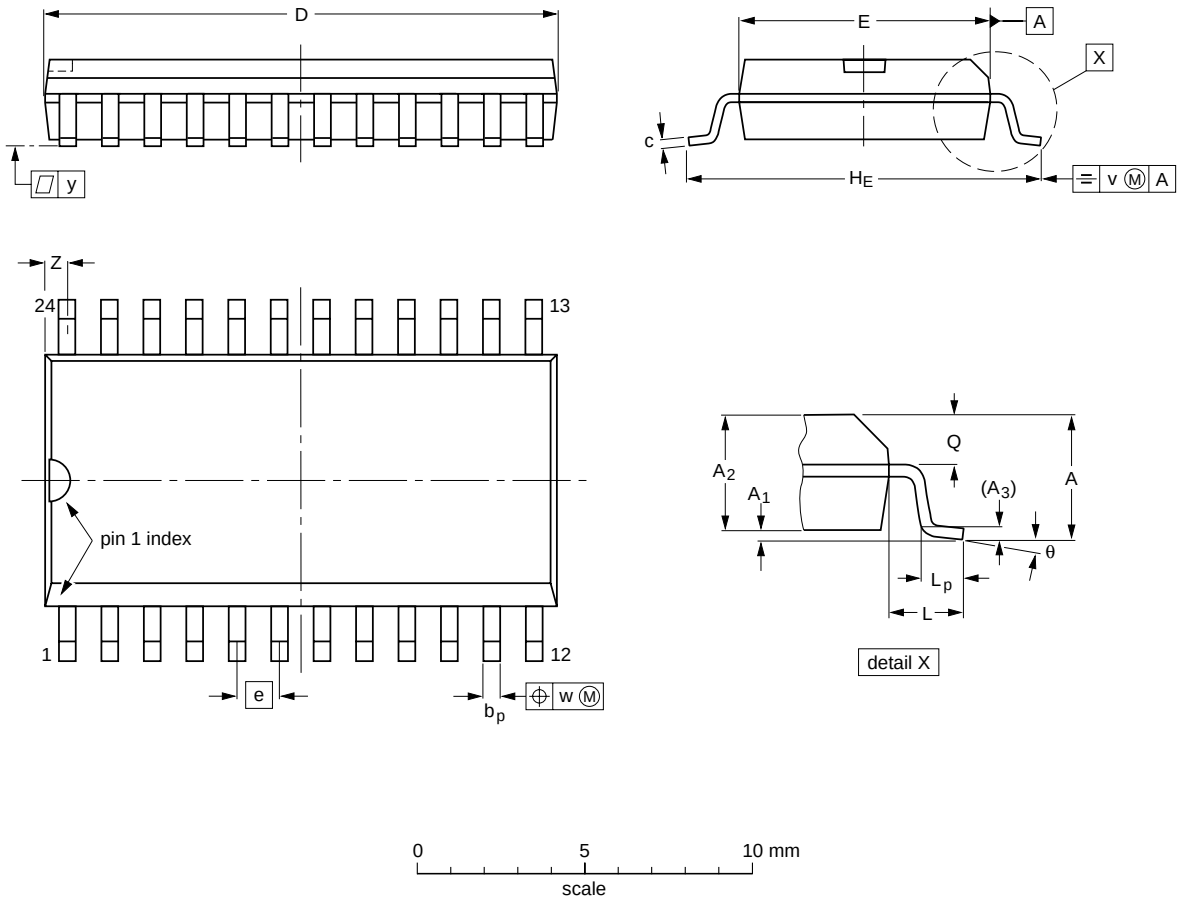


V_P = ±25 V; R_L = 2 × 8 Ω.

Fig.39 PWM residual voltage as a function of clock frequency.

16 PACKAGE OUTLINE

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013				~~97-05-22~~ 99-12-27

17 SOLDERING

17.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

17.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

17.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

17.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

17.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

18 DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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