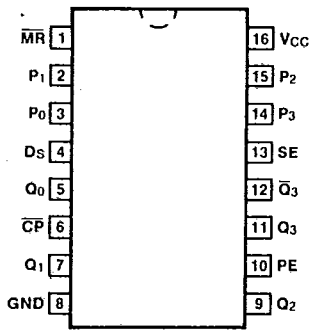
54/74179

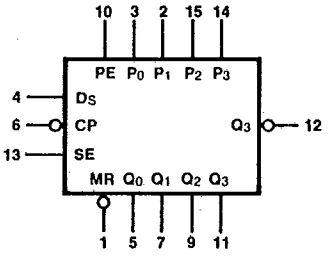
4-BIT SHIFT REGISTER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '179 features synchronous parallel or serial entry, asynchronous reset and parallel outputs, with the complement output of the fourth stage also available. The flip-flops are fully edge-triggered, with state changes initiated by a HIGH-to-LOW transition of the clock. Parallel Enable and Serial Enable inputs are used to select Load, Shift and Hold modes of operation. A LOW signal on the Master Reset input overrides all other inputs and forces the Q outputs to the LOW state.

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		VCC = +5.0 V ±5%, TA = 0°C to +70°C	VCC = +5.0 V ±10%, TA = -55°C to +125°C	
Plastic DIP (P)	A	74179PC		9B
Ceramic DIP (D)	A	74179DC	54179DM	6B
Flatpak (F)	A	74179FC	54179FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
PE	Parallel Enable Input	1.0/1.0
P0 — P3	Parallel Data Inputs	1.0/1.0
DS	Serial Data Input	1.0/1.0
SE	Shift Enable Input	1.0/1.0
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	1.0/1.0
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0
Q0 — Q3	Flip-flop Outputs	20/10
$\overline{Q}_3$	Fourth Stage Complement Output	20/10

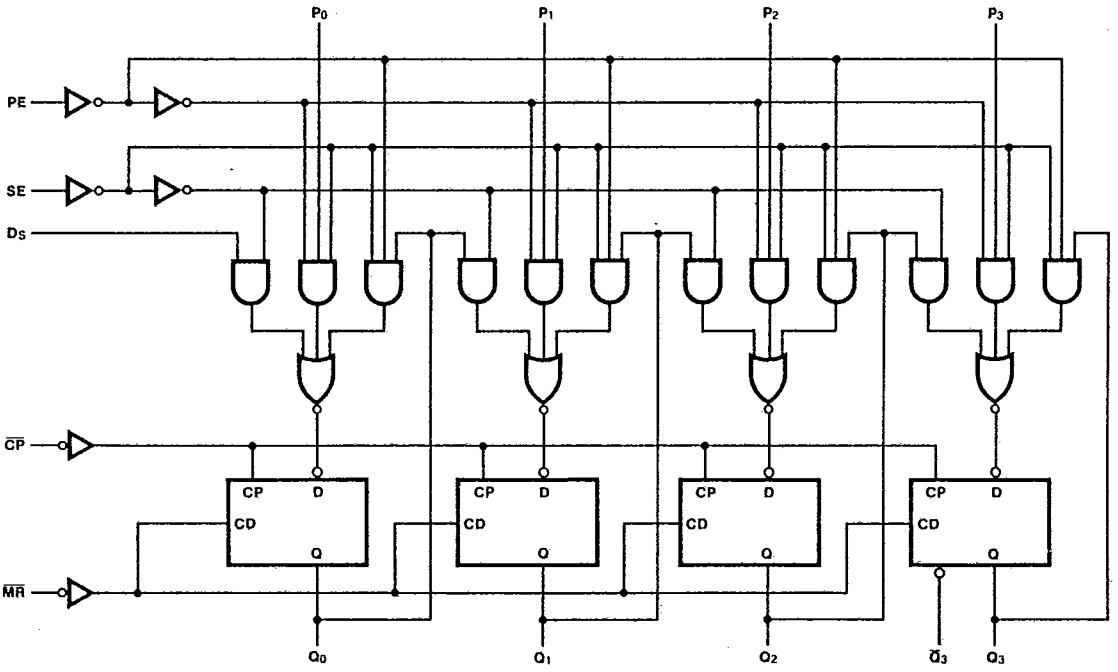
FUNCTIONAL DESCRIPTION — The '179 contains four D-type edge-triggered flip-flops and sufficient inter-stage logic to perform parallel load, shift right or hold operations. All state changes except reset are initiated by a HIGH-to-LOW transition of the clock. A LOW signal on $\overline{MR}$ overrides all other inputs and forces the Q outputs LOW and $\overline{Q}_3$ HIGH. With $\overline{MR}$ HIGH, a HIGH signal on SE prevents parallel loading and permits a right shift each time the clock makes a HIGH-to-LOW transition. When $\overline{MR}$ and SE are LOW, the signal applied to PE determines whether the circuit is in a parallel load or a hold mode, as shown in the Mode Select Table. The SE, PE, D_S and P_n inputs can change when the clock is in either state, provided only that the recommended setup and hold times are observed.

MODE SELECT TABLE

INPUTS				RESPONSE
$\overline{MR}$	SE	PE	$\overline{CP}$	
L	X	X	X	Asynchronous Reset; $Q_n \rightarrow$ LOW; $Q_3 \rightarrow$ HIGH
H	H	X	⌐	Right Shift. $D_S \rightarrow Q_0$; $Q_0 \rightarrow Q_1$, etc.
H	L	H	⌐	Parallel load. $P_n \rightarrow Q_n$
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		70	mA	V_{CC} = Max, P_n = Gnd $\overline{D_S}$, $\overline{PE}$, SE, $\overline{MR}$ = 4.5 V $\overline{CP}$ = ⊥
		XC		75		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 C_L = 15 pF, R_L = 400 Ω Max	UNITS	CONDITIONS
f_{max}	Maximum Clock Frequency	25		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q_n		26 35	ns	Figs. 3-1, 3-9
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_3		23	ns	Figs. 3-1, 3-17
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		36	ns	

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW D_S or P_n to $\overline{CP}$	30 30		ns	Fig. 3-7
t_h (H) t_h (L)	Hold Time HIGH or LOW D_S or P_n to $\overline{CP}$	5.0 5.0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW PE or SE to $\overline{CP}$	35 35		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW PE or SE to $\overline{CP}$	5.0 5.0		ns	
t_w (H)	$\overline{CP}$ Pulse Width HIGH	20		ns	Fig. 3-9
t_w (L)	$\overline{MR}$ Pulse Width LOW	20		ns	Fig. 3-17
t_{rec}	Recovery Time $\overline{MR}$ to $\overline{CP}$	15		ns	Fig. 3-17